

74ABT374A

Octal D-type flip-flop; positive-edge trigger; 3-state

Rev. 2 — 18 December 2012

Product data sheet

1. General description

The 74ABT374A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT374A is an 8-bit, edge triggered register coupled to eight 3-state output buffers. The two sections of the device are controlled independently by the clock input (CP) and output enable input ($\overline{OE}$) control gates.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The active LOW output enable ($\overline{OE}$) controls all eight 3-state buffers independent of the clock operation.

When $\overline{OE}$ is LOW, the stored data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance "OFF" state, which means they will neither drive nor load the bus.

2. Features and benefits

- 8-bit positive edge triggered register
- 3-state output buffers
- Power-on 3-state
- Power-on reset
- Output capability: +64 mA/–32 mA
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Live insertion/extraction permitted

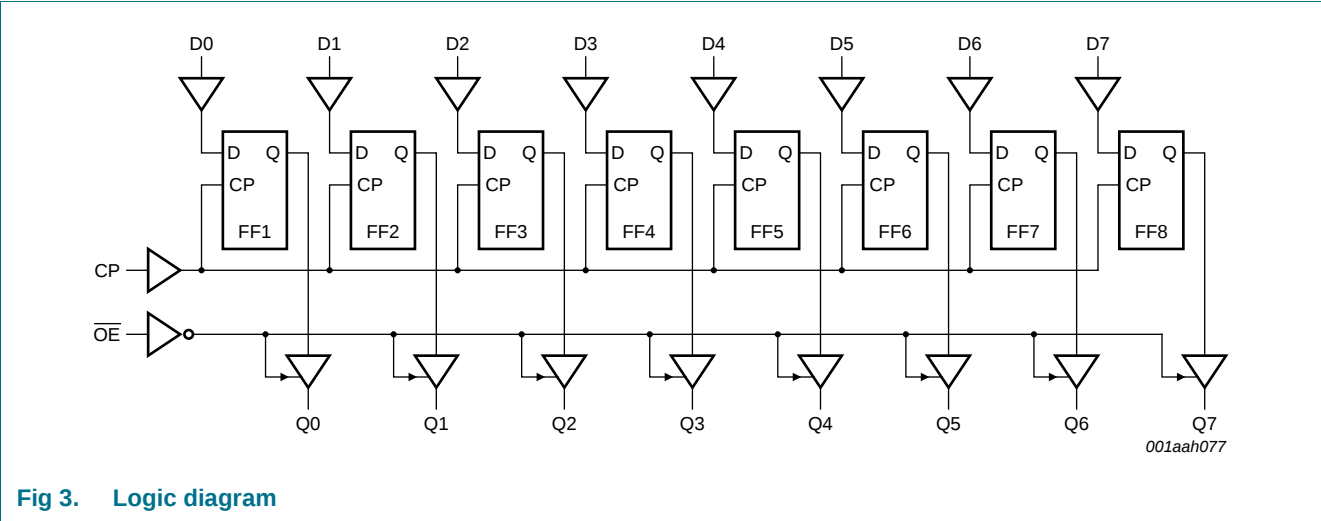
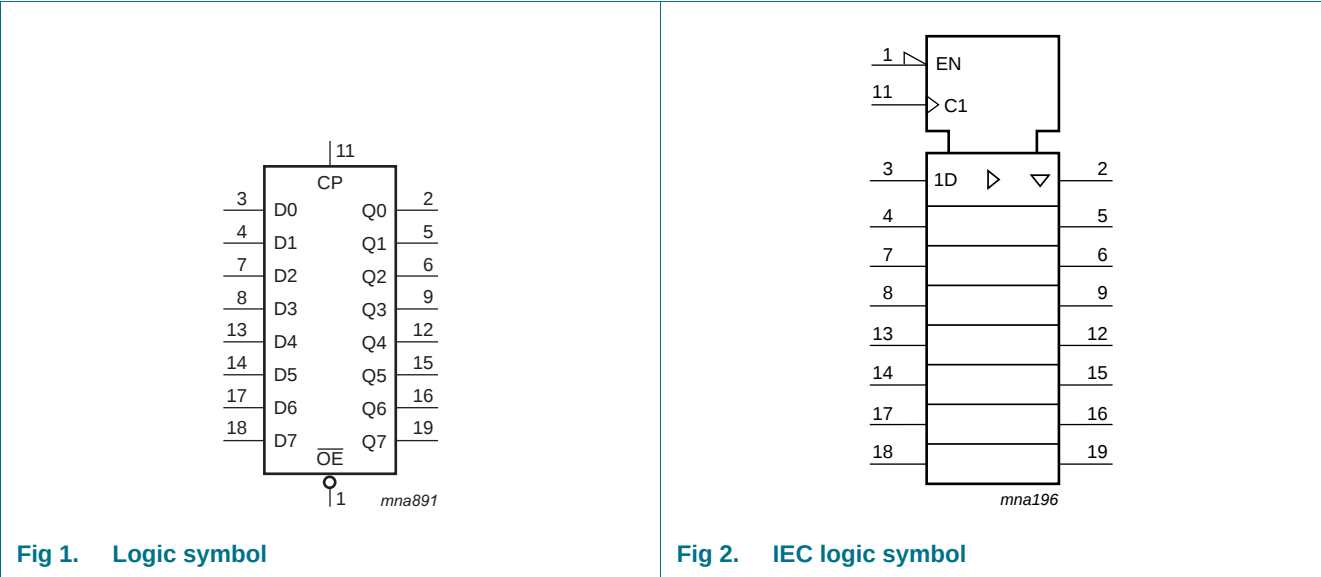


3. Ordering information

Table 1. Ordering information

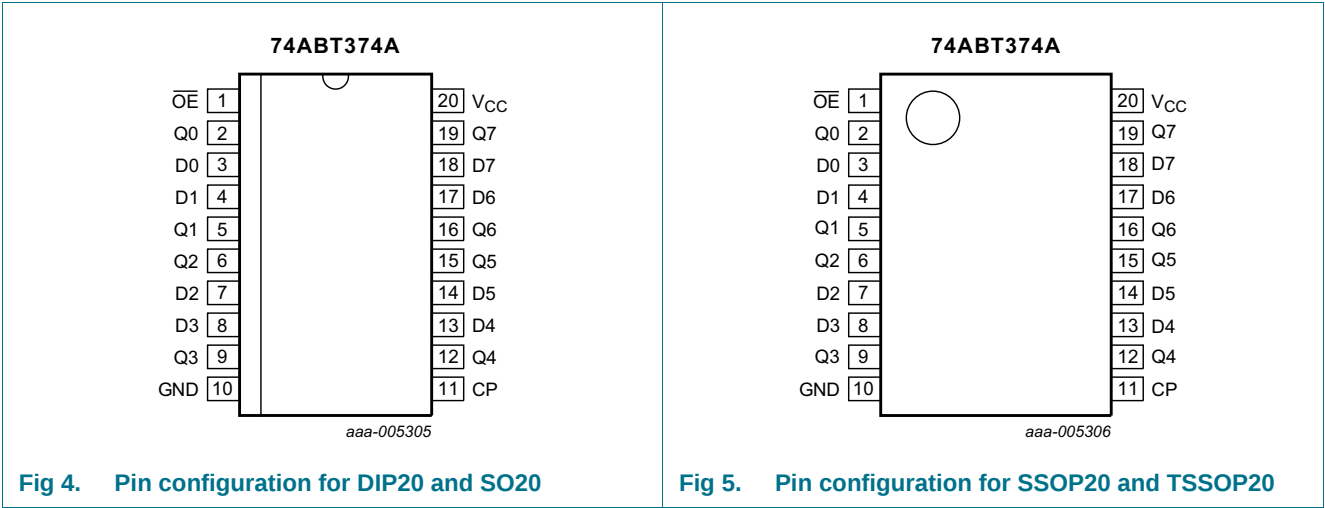
Type number	Package			
	Temperature range	Name	Description	Version
74ABT374AN	−40 °C to +85 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74ABT374AD	−40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ABT374ADB	−40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74ABT374APW	−40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
OE	1	3-state output enable input (active LOW)
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data input
GND	10	ground (0 V)
CP	11	clock pulse input (active rising edge)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	3-state flip-flop output
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table^[1]

Operating mode	Input			Internal flip-flop	Output Q _n
	OE	CP	D _n		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable output	H	↑	l	L	Z
	H	↑	h	H	Z

[1] H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH CP transition
Z = high-impedance OFF-state
↑ = LOW-to-HIGH clock transition

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		−0.5	+7.0	V
V _I	input voltage		^[1] −1.2	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	^[1] −0.5	+5.5	V
I _{IK}	input clamping current	V _I < 0 V	−18	-	mA
I _{OK}	output clamping current	V _O < 0 V	−50	-	mA
I _O	output current	output in LOW-state	-	128	mA
T _j	junction temperature		^[2] -	150	°C
T _{stg}	storage temperature		−65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		4.5	-	5.5	V
V _I	input voltage		0	-	V _{CC}	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
I _{OH}	HIGH-level output current		−32	-	-	mA
I _{OL}	LOW-level output current		-	-	64	mA
Δt/ΔV	input transition rise and fall rate		0	-	10	ns/V
T _{amb}	ambient temperature	in free air	−40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V _{IK}	input clamping voltage	V _{CC} = 4.5 V; I _{IK} = −18 mA	−1.2	−0.9	-	−1.2	-	V
V _{OH}	HIGH-level output voltage	V _I = V _{IL} or V _{IH}						
		V _{CC} = 4.5 V; I _{OH} = −3 mA	2.5	2.9	-	2.5	-	V
		V _{CC} = 5.0 V; I _{OH} = −3 mA	3.0	3.4	-	3.0	-	V
		V _{CC} = 4.5 V; I _{OH} = −32 mA	2.0	2.4	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; I _{OL} = 64 mA; V _I = V _{IL} or V _{IH}	-	0.42	0.55	-	0.55	V

Table 6. Static characteristics ...continued

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
$V_{OL(pu)}$	power-up LOW-level output voltage	$V_{CC} = 5.5 \text{ V}$; $I_O = 1 \text{ mA}$; $V_I = \text{GND or } V_{CC}$ [1]	-	0.13	0.55	-	0.55	V
I_I	input leakage current	$V_{CC} = 5.5 \text{ V}$; $V_I = V_{CC} \text{ or } \text{GND}$	-	± 0.01	± 1.0	-	± 1.0	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}$; $V_I \text{ or } V_O \leq 4.5 \text{ V}$	-	± 5.0	± 100	-	± 100	μA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} = 2.0 \text{ V}$; $V_O = 0.5 \text{ V}$; $V_I = \text{GND or } V_{CC}$; OE HIGH [2]	-	± 5.0	± 50	-	± 50	μA
I_{OZ}	OFF-state output current	$V_{CC} = 5.5 \text{ V}$; $V_I = V_{IL} \text{ or } V_{IH}$						
		$V_O = 2.7 \text{ V}$	-	5.0	50	-	50	μA
		$V_O = 0.5 \text{ V}$	-50	-5.0	-	-50	-	μA
I_{LO}	output leakage current	HIGH-state; $V_O = 5.5 \text{ V}$; $V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND or } V_{CC}$	-	5.0	50	-	50	μA
I_O	output current	$V_{CC} = 5.5 \text{ V}$; $V_O = 2.5 \text{ V}$ [3]	-180	-100	-50	-180	-50	mA
I_{CC}	supply current	$V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND or } V_{CC}$						
		outputs HIGH-state	-	110	250	-	250	μA
		outputs LOW-state	-	24	30	-	30	mA
		outputs disabled	-	110	250	-	250	μA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 5.5 \text{ V}$; one input at 3.4 V; other inputs at $V_{CC} \text{ or } \text{GND}$ [4]	-	0.5	1.5	-	1.5	mA
C_I	input capacitance	$V_I = 0 \text{ V or } V_{CC}$	-	4	-	-	-	pF
C_O	output capacitance	outputs disabled; $V_O = 0 \text{ V or } V_{CC}$	-	7	-	-	-	pF

[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

[2] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From $V_{CC} = 2.1 \text{ V}$ to $V_{CC} = 5 \text{ V} \pm 10 \%$ a transition time of up to 100 μs is permitted.

[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[4] This is the increase in supply current for each input at 3.4 V.

10. Dynamic characteristics

Table 7. Dynamic characteristics

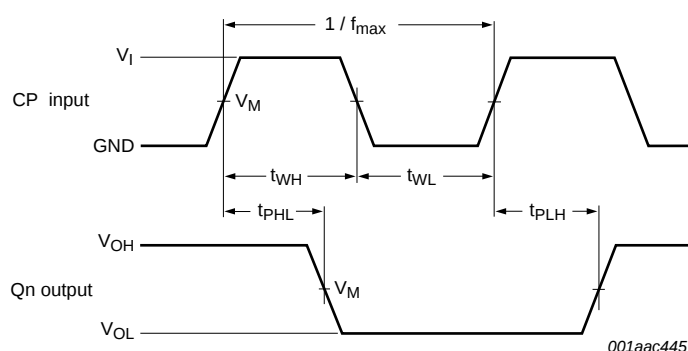
$\text{GND} = 0 \text{ V}$; for test circuit, see Figure 9.

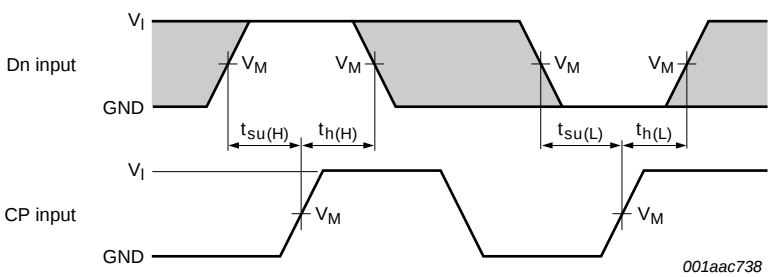
Symbol	Parameter	Conditions	25 °C; $V_{CC} = 5.0 \text{ V}$			–40 °C to +85 °C; $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$		Unit
			Min	Typ	Max	Min	Max	
$f_{\max}$	maximum frequency	see Figure 6	200	300	-	200	-	MHz
t_{PLH}	LOW to HIGH propagation delay	CP to Qn; see Figure 6	1.7	3.4	4.5	1.7	5.1	ns
t_{PHL}	HIGH to LOW propagation delay	CP to Qn; see Figure 6	2.0	3.8	4.9	2.0	5.2	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{\text{OE}}$ to Qn; see Figure 8	1.2	3.5	4.5	1.2	5.4	ns

Table 7. Dynamic characteristics ...continuedGND = 0 V; for test circuit, see [Figure 9](#).

Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			–40 °C to +85 °C; V _{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t _{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to Qn; see Figure 8	2.2	4.3	5.4	2.2	6.2	ns
t _{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to Qn; see Figure 8	1.8	3.6	4.7	1.8	5.2	ns
t _{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to Qn; see Figure 8	1.5	3.0	4.1	1.5	4.3	ns
t _{SU(H)}	set-up time HIGH	Dn to CP; see Figure 7	1.5	0.6	-	1.5	-	ns
t _{SU(L)}	set-up time LOW	Dn to CP; see Figure 7	1.2	0.3	-	1.2	-	ns
t _{H(H)}	hold time HIGH	CP to Dn; see Figure 7	1.0	–0.3	-	1.0	-	ns
t _{H(L)}	hold time LOW	CP to Dn; see Figure 7	1.0	–0.5	-	1.0	-	ns
t _{WH}	pulse width HIGH	CP; see Figure 6	2.0	0.8	-	2.0	-	ns
t _{WL}	pulse width LOW	CP; see Figure 6	2.8	1.0	-	2.8	-	ns

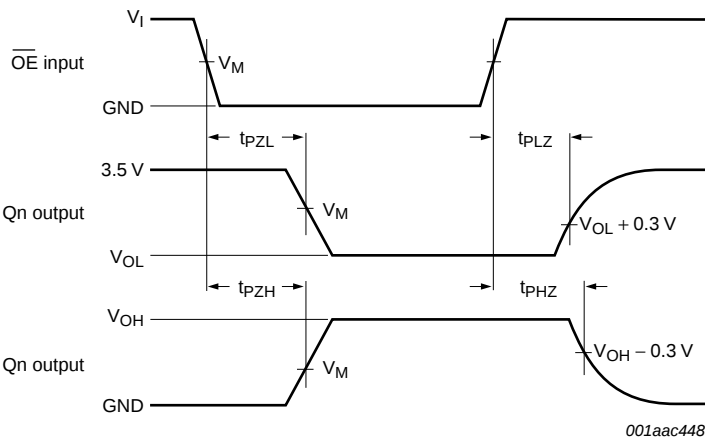
11. Waveforms

 $V_M = 1.5\text{ V}$ V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.**Fig 6.** Propagation delay clock input (CP) to output (Qn), clock pulse (CP) width and maximum clock (CP) frequency



$V_M = 1.5\text{ V}$
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 7. Set-up and hold times data output (Dn) to clock (CP)



$V_M = 1.5\text{ V}$
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load

Fig 8. 3-state output (Qn) enable and disable times

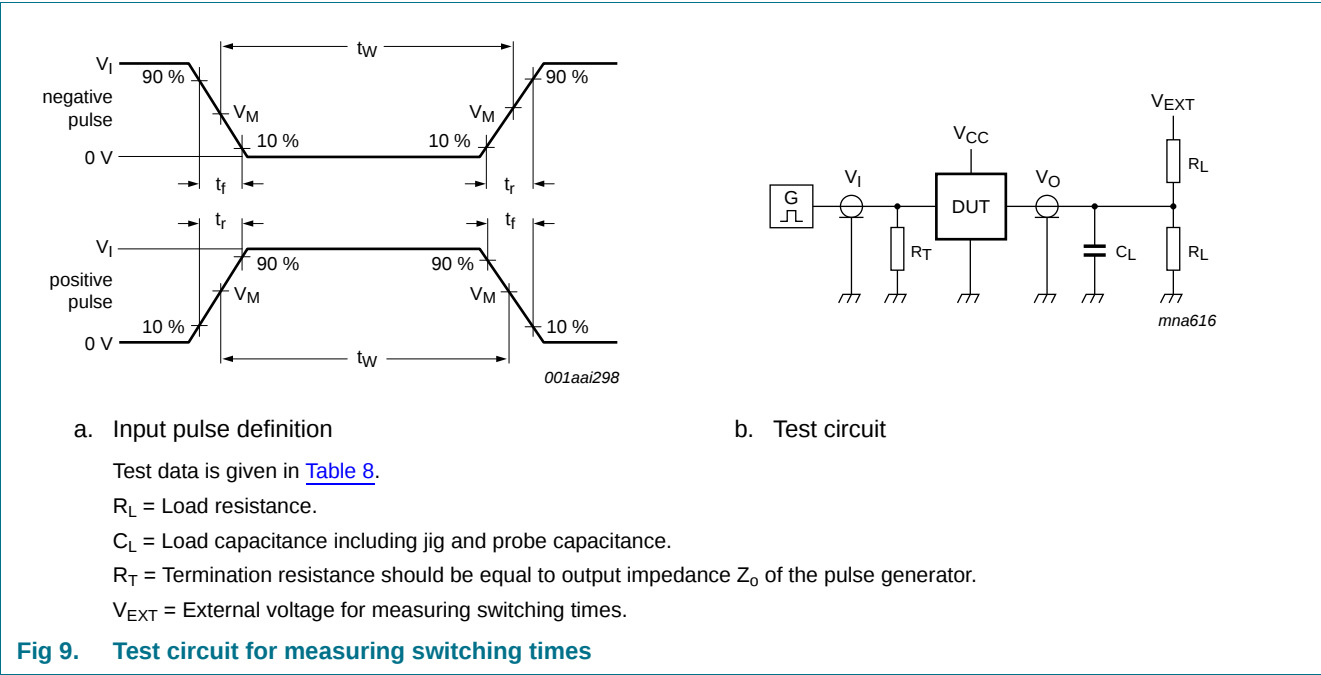


Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

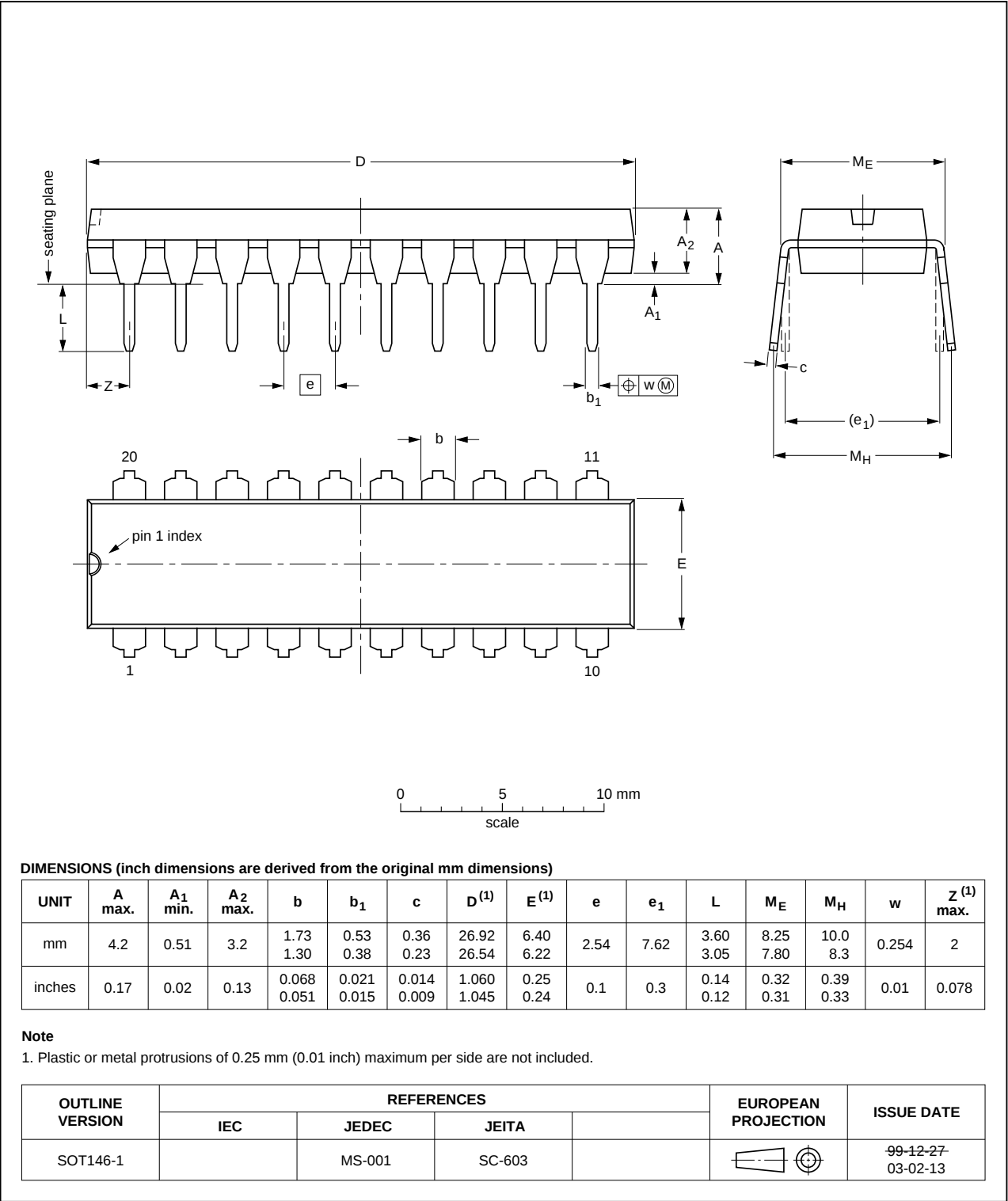
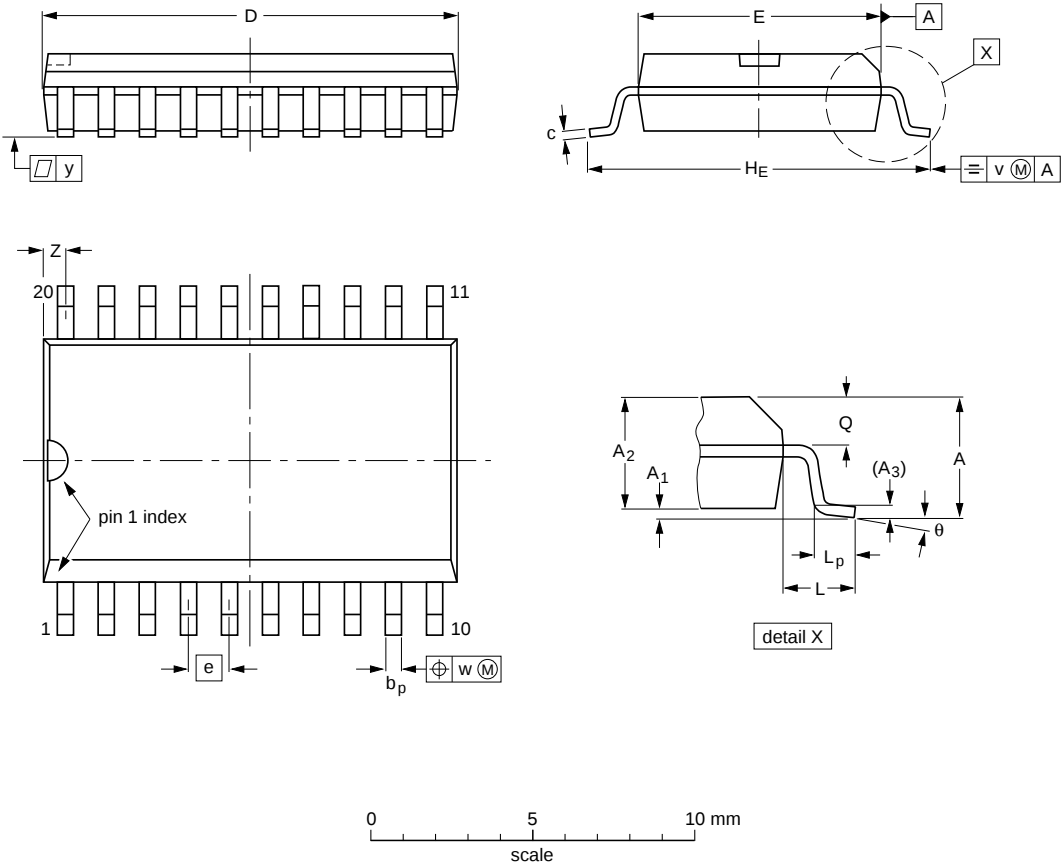


Fig 10. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

Fig 11. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

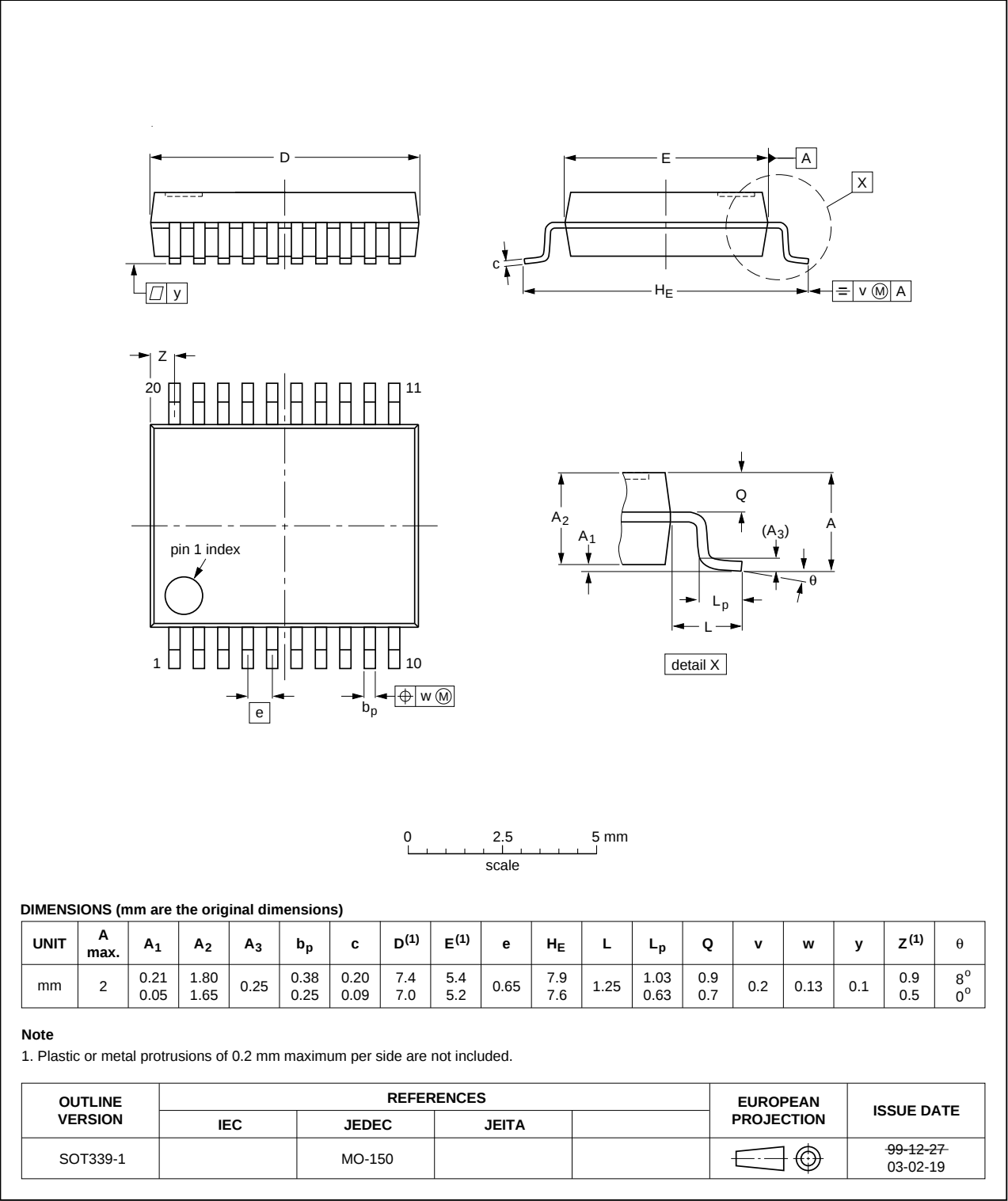


Fig 12. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

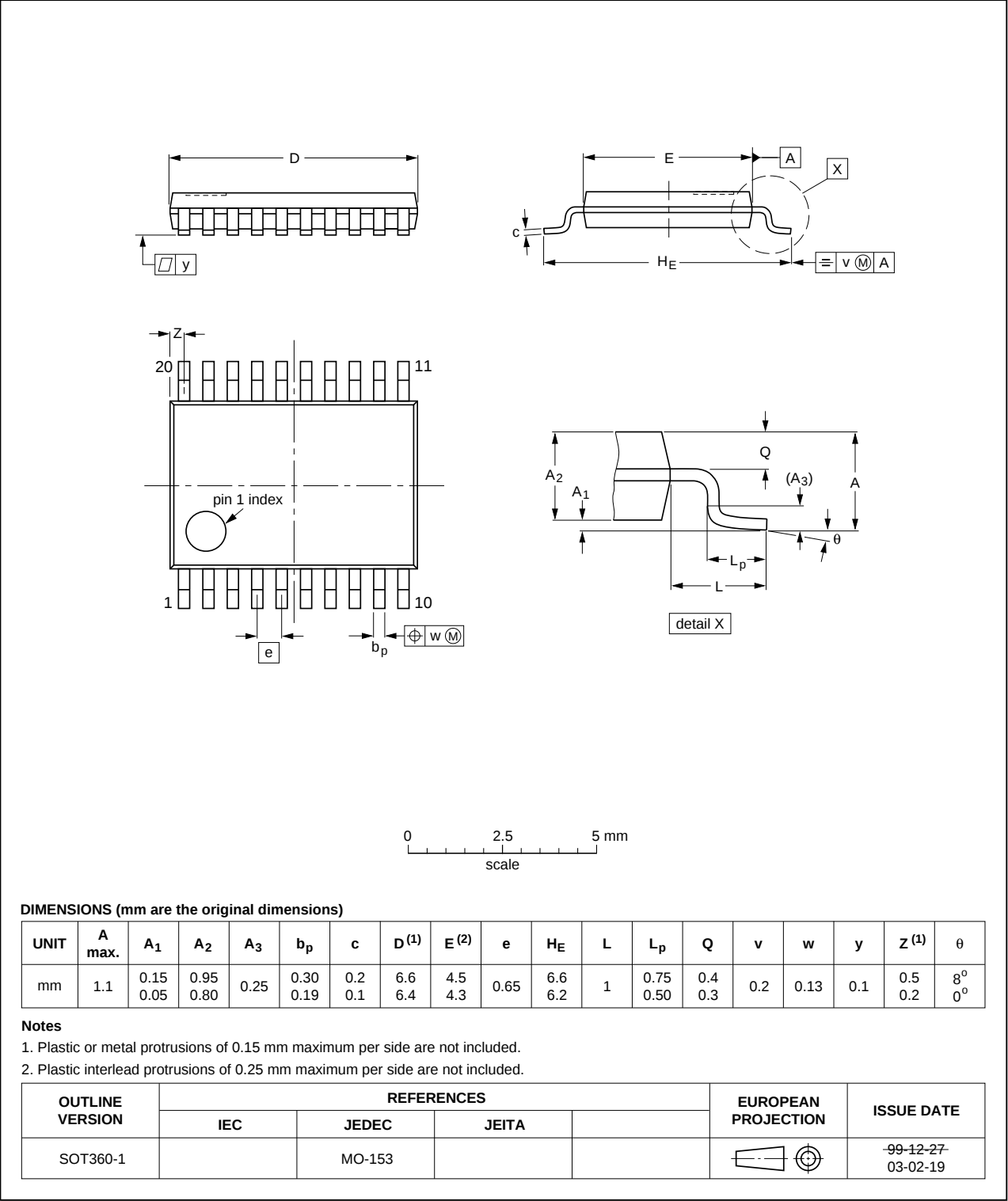


Fig 13. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BICMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT374A v.2	20121218	Product data sheet	-	74ABT374A v.1
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate.			
74ABT374A v.1	19950906	Product specification	-	-

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15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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