

## Xtrinsic MMA8491Q 3-Axis Multifunction Digital Accelerometer

The MMA8491Q is a low voltage, 3-axis low-g accelerometer housed in a 3 mm x 3 mm QFN package. The device can accommodate two accelerometer configurations, acting as either a 45° tilt sensor or a digital output accelerometer with I<sup>2</sup>C bus.

- As a 45° Tilt Sensor, the MMA8491Q device offers extreme ease of implementation by using a single line output per axis.
- As a digital output accelerometer, the 14-bit  $\pm 8g$  accelerometer data can be read from the device with a 1 mg/LSB sensitivity.

The extreme low power capabilities of the MMA8491Q will reduce the low data rate current consumption to less than 400 nA per Hz.

### Features

- Extreme low power, 400 nA per Hz
- Ultra-fast data output time,  $\sim 700 \mu s$
- 1.95V to 3.6V V<sub>DD</sub> supply range
- 3 mm x 3 mm, 0.65 mm pitch with visual solder joint inspection
- $\pm 8g$  full-scale range
- 14-bit digital output, 1 mg/LSB sensitivity
- Output Data Rate (ODR), implementation based from < 1 Hz to 800 Hz
- I<sup>2</sup>C digital interface
- 3-axis, 45° tilt outputs

### Typical Applications

- Smart grid: tamper detect
- Anti-theft
- White goods tilt
- Remote controls

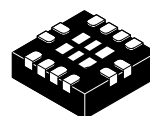
### Related Documentation

The MMA8491Q device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to the Freescale homepage at: <http://www.freescale.com/>
2. In the Keyword search box at the top of the page, enter the device number MMA8491Q. In the Refine Your Result pane on the left, click on the Documentation link.

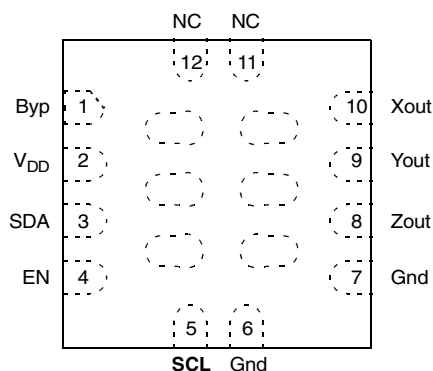
## MMA8491Q

### Bottom View



**12-Lead Industrial QFN**  
3 mm x 3 mm x 1.05 mm  
0.65 mm Pitch

### Pin Connections



### ORDERING INFORMATION

| Part Number | Temperature Range | Package | Shipping              |
|-------------|-------------------|---------|-----------------------|
| MMA8491QT   | -40 to +85°C      | QFN 12  | Tray                  |
| MMA8491QR1  | -40 to +85°C      | QFN 12  | 1000 pc / Tape & Reel |

# Contents

|          |                                                 |           |
|----------|-------------------------------------------------|-----------|
| <b>1</b> | <b>Block Diagram and Pin Descriptions</b>       | <b>3</b>  |
| 1.1      | Block diagram                                   | 3         |
| 1.2      | Definition of acceleration directions           | 3         |
| 1.3      | Tilt detection outputs                          | 4         |
| 1.4      | Pin descriptions                                | 5         |
| 1.5      | Recommended application diagram                 | 6         |
| <b>2</b> | <b>Mechanical and Electrical Specifications</b> | <b>7</b>  |
| 2.1      | Absolute maximum ratings                        | 7         |
| 2.2      | Mechanical characteristics                      | 8         |
| 2.3      | Electrical characteristics                      | 9         |
| 2.4      | I2C interface characteristics                   | 10        |
| <b>3</b> | <b>Modes of Operation</b>                       | <b>11</b> |
| 3.1      | ACTIVE mode                                     | 11        |
| 3.2      | STANDBY mode                                    | 11        |
| 3.3      | Next sample acquisition                         | 11        |
| 3.4      | Power-up timing sequences                       | 12        |
| 3.5      | 45° tilt detection                              | 12        |
| 3.6      | Tilt angle                                      | 13        |
| <b>4</b> | <b>Serial Interface (I<sup>2</sup>C)</b>        | <b>14</b> |
| 4.1      | I2C operation                                   | 14        |
| 4.2      | Single byte read                                | 14        |
| 4.3      | Multiple byte read                              | 15        |
| <b>5</b> | <b>Register Descriptions</b>                    | <b>16</b> |
| 5.1      | Register address map                            | 16        |
| 5.2      | Register bit map                                | 16        |
| 5.3      | Data registers                                  | 17        |
| 5.4      | Accelerometer output conversion                 | 18        |
| <b>6</b> | <b>Mounting Guidelines</b>                      | <b>19</b> |
| 6.1      | Overview of soldering considerations            | 19        |
| 6.2      | Halogen content                                 | 19        |
| 6.3      | PCB mounting recommendations                    | 19        |
| <b>7</b> | <b>Tape and Reel</b>                            | <b>21</b> |
| 7.1      | Tape dimensions                                 | 21        |
| 7.2      | Label and device orientation                    | 21        |
| <b>8</b> | <b>Package Dimensions</b>                       | <b>22</b> |
| <b>9</b> | <b>Revision History</b>                         | <b>25</b> |

# 1 Block Diagram and Pin Descriptions

## 1.1 Block diagram

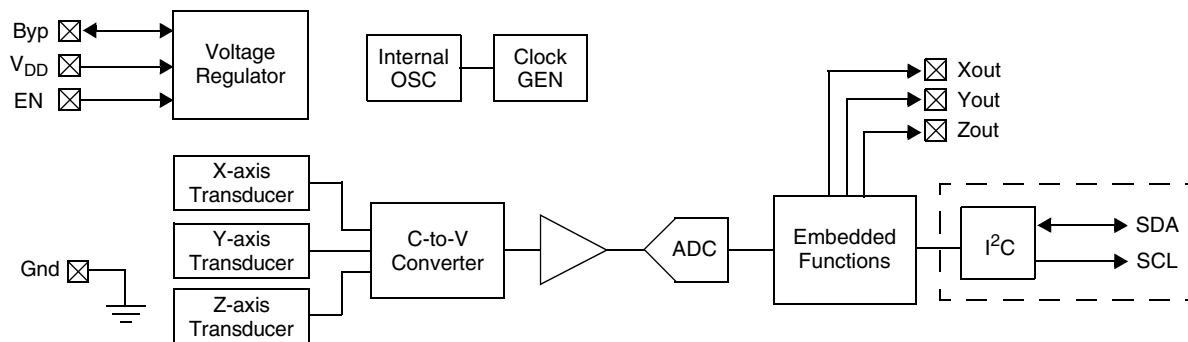


Figure 1. MMA8491Q block diagram

## 1.2 Definition of acceleration directions

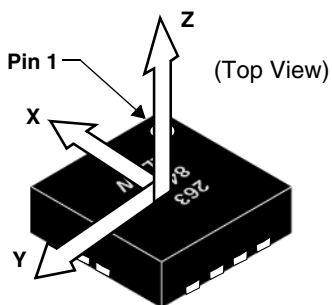


Figure 2. Acceleration direction definitions

### 1.3 Tilt detection outputs

The MMA8491Q has 3 tilt detection outputs: Xout, Yout, Zout. Figure 3 shows the output results at the 6 different orientation positions.

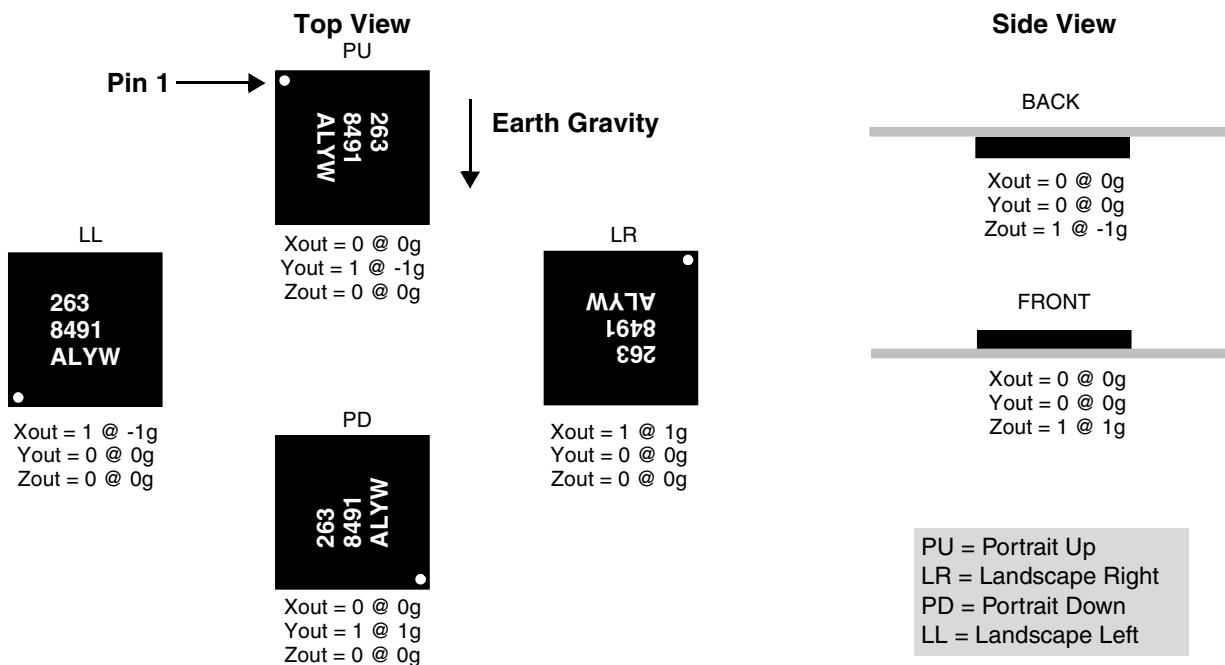
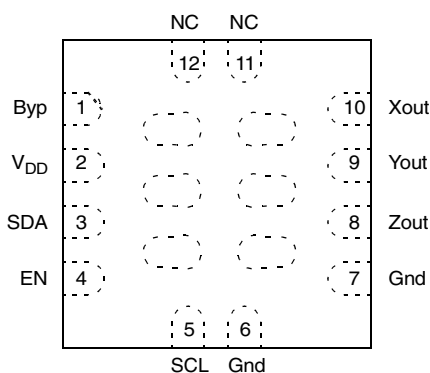


Figure 3. X, Y, Z output based on MMA8491Q orientation

## 1.4 Pin descriptions

MMA8491Q is hosted in a 12-pin 3 mm x 3 mm QFN package. Ten pins are used for functions; two pins are unconnected. Refer to [Table 1](#) for complete pin descriptions and functions.

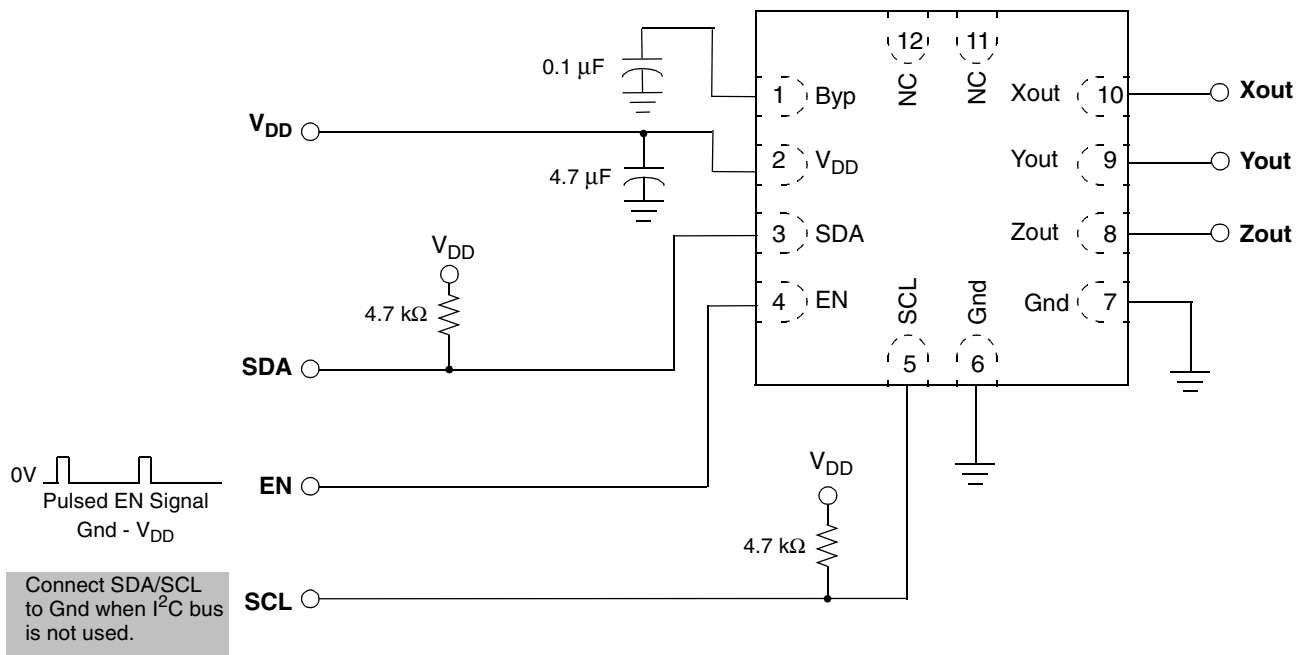


**Figure 4. Pin connections (top view)**

**Table 1. Pin descriptions**

| Pin # | Pin Name        | Function                                       | Description                                                                                                                                                                                                                                                                                | Pin Status   |
|-------|-----------------|------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|
| 1     | Byp             | Internal regulator output capacitor connection | The internal regulator voltage of 1.8V is present on this pin. Connect to external 0.1 $\mu$ F bypass capacitor.                                                                                                                                                                           | Output       |
| 2     | V <sub>DD</sub> | Power Supply                                   | Device power is supplied through the V <sub>DD</sub> line. Power supply decoupling capacitors should be placed as near as possible to pin 1 of the device.                                                                                                                                 | Input        |
| 3     | SDA             | I <sup>2</sup> C Data                          | I <sup>2</sup> C Slave Data Line <ul style="list-style-type: none"> <li>7-bit I<sup>2</sup>C device address is 0x55.</li> <li>The SDA and SCL I<sup>2</sup>C connections are open drain, and therefore usually require a pullup resistor</li> </ul>                                        | Input/Output |
| 4     | EN              | Enable Pin                                     | The Enable pin fully turns on the accelerometer system when it is pulled up to logic high. The accelerometer system is turned off when the Enable pin is logic low.                                                                                                                        | Input        |
| 5     | SCL             | I <sup>2</sup> C Clock                         | I <sup>2</sup> C Slave Clock Line                                                                                                                                                                                                                                                          | Input        |
| 6     | Gnd             | Ground                                         |                                                                                                                                                                                                                                                                                            | Ground       |
| 7     | Gnd             | Ground                                         |                                                                                                                                                                                                                                                                                            | Ground       |
| 8     | Zout            | Push-pull Z-Axis Tilt Detection Output         | <ul style="list-style-type: none"> <li>Output is high when acceleration is &gt; 0.688g (axis is <math> \phi  &gt; 45^\circ</math>).</li> <li>Output is low when acceleration is <math>\leq 0.688g</math> (axis is <math> \phi  \leq 45^\circ</math>).</li> </ul> These pins are push-pull. | Output       |
| 9     | Yout            | Push-pull Y-Axis Tilt Detection Output         |                                                                                                                                                                                                                                                                                            | Output       |
| 10    | Xout            | Push-pull X-Axis Tilt Detection Output         |                                                                                                                                                                                                                                                                                            | Output       |
| 11    | NC              | No internal connection                         |                                                                                                                                                                                                                                                                                            |              |
| 12    | NC              | No internal connection                         |                                                                                                                                                                                                                                                                                            |              |

## 1.5 Recommended application diagram



**Figure 5. V<sub>DD</sub> connects to power supply and EN is pulsed**

To ensure the accelerometer is fully functional, connect the MMA8491Q as suggested in [Figure 5](#).

- A capacitor must be connected to the Bypass pin (pin 1) to assist the internal voltage regulator. It is recommended to use a 0.1 µF capacitor. The capacitor should be placed as near as possible to the Bypass pin.
- The device power is supplied through the V<sub>DD</sub> line. The power supply decoupling capacitor should be placed as close as possible to the V<sub>DD</sub> pin.
  - Use a 1.0 or 4.7 µF capacitor when the V<sub>DD</sub> and EN are not tied together.
  - When V<sub>DD</sub> and EN are tied together, then use a 0.1 µF capacitor. The 0.1 µF capacitor value has been chosen to minimize the average current consumption while still maintaining an acceptable level of power supply high-frequency filtering.
- Both ground pins (pins 6 and 7) must be connected to ground.
- When the I<sup>2</sup>C communication line is used, use a pullup resistor to connect to line SDA and SCL. The SCL line can be driven by a push-pull driver, in which case, no pull-up resistor is necessary. If SDA and SCL pins are not used, then they should be tied to ground.

## 2 Mechanical and Electrical Specifications

### 2.1 Absolute maximum ratings

Table 2. Maximum ratings

| Rating                                       | Symbol     | Value        | Unit        |
|----------------------------------------------|------------|--------------|-------------|
| Maximum acceleration (all axes, 100 $\mu$ s) | $g_{max}$  | 10,000       | g           |
| Analog supply voltage                        | $V_{DD}$   | -0.3 to +3.6 | V           |
| Drop test                                    | $D_{drop}$ | 1.8          | m           |
| Operation temperature range                  | $T_{AGOC}$ | -40 to +85   | $^{\circ}C$ |
| Storage temperature range                    | $T_{stg}$  | -40 to +125  | $^{\circ}C$ |

Table 3. ESD and LATCHUP protection characteristics

| Rating                                 | Symbol | Value      | Unit |
|----------------------------------------|--------|------------|------|
| Human body model                       | HBM    | $\pm 2000$ | V    |
| Machine model                          | MM     | $\pm 200$  | V    |
| Charge device model                    | CDM    | $\pm 500$  | V    |
| Latchup current at $T_A = 85^{\circ}C$ |        | $\pm 100$  | mA   |

## 2.2 Mechanical characteristics

Mechanical characteristics are at  $V_{DD} = 2.8V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted <sup>(8)</sup> <sup>(10)</sup>.

**Table 4. Mechanical characteristics**

| Parameter                                                           | Symbol            | Conditions                                                                                               | Min            | Typ                 | Max   | Unit     |
|---------------------------------------------------------------------|-------------------|----------------------------------------------------------------------------------------------------------|----------------|---------------------|-------|----------|
| Full-scale measurement range <sup>(2)</sup>                         | FS                |                                                                                                          |                | ±8                  |       | g        |
| Sensitivity <sup>(1)</sup>                                          | So                |                                                                                                          | 973            | 1024                | 1075  | counts/g |
| Calibrated sensitivity error <sup>(1)</sup>                         | CSE               | All axes, all ranges                                                                                     | -5             |                     | 5     | %        |
| Cross-axis sensitivity <sup>(2)</sup>                               | CX <sub>SEN</sub> | Die rotation included                                                                                    | -4.2           |                     | 4.2   | %        |
| Sensitivity temperature variation <sup>(2)</sup>                    | TCS               | -40°C to +85°C                                                                                           | -0.014         |                     | 0.014 | %/°C     |
| Zero-g level temperature variation <sup>(2)</sup>                   | TCO               | -40°C to +85°C                                                                                           | -0.98          |                     | 0.98  | mg/°C    |
| Zero-g level offset accuracy <sup>(1)</sup> <sup>(3)</sup>          | TyOff             |                                                                                                          | -100           |                     | 100   | mg       |
| Zero-g level after board mount <sup>(2)</sup> <sup>(4)</sup>        | TyOffPBM          |                                                                                                          | -120           |                     | 120   | mg       |
| Noise <sup>(2)</sup>                                                | RMS               |                                                                                                          |                | 11.5 <sup>(9)</sup> | 18    | mg-rms   |
| Nonlinearity <sup>(2)</sup>                                         | NL                |                                                                                                          |                |                     | 1     | %FS      |
| Threshold / g-value <sup>(5)</sup>                                  | TDL               | Internal threshold of output level change (from 0g reference) , g values are calculated from trip angles | 25°C           | 0.583               | 0.688 | g        |
|                                                                     |                   |                                                                                                          | -40°C to +85°C | 0.577               | 0.688 |          |
| Threshold / Tilt angle <sup>(2)</sup> <sup>(4)</sup> <sup>(5)</sup> | TDL               | Internal threshold of output level change (from 0g reference)                                            | 25°C           | 35.6                | 43.5  | degrees  |
|                                                                     |                   |                                                                                                          | -40°C to +85°C | 35.2                | 43.5  |          |
| Temperature range <sup>(2)</sup>                                    | T <sub>AGOC</sub> |                                                                                                          | -40            | 25                  | 85    | °C       |

1. Parameters tested 100% at final test at room temperature.

2. Verified by characterization; not tested in production.

3. Before board mount.

4. Post-board mount offset specifications are based on a 4-layer PCB, relative to 25°C.

5. All angles are based on the trip angle from static 0g to 1g; the g-values are calculated from the trip angle.

6. Evaluation data: not tested in production.

7. Guaranteed by design.

8. Typical number is the target number, unless otherwise specified.

9. Typical number is mean data.

10. All numbers are based on  $V_{DD}$  cap = 4.7  $\mu F$ .

## 2.3 Electrical characteristics

Electrical characteristics are at  $V_{DD} = 2.8V$ ,  $T_A = +25^\circ C$ , unless otherwise noted. <sup>(8)</sup> <sup>(13)</sup>

**Table 5. Electrical characteristics**

| Parameter                                                    | Symbol                | Conditions                                                                          | Min             | Typ                                               | Max                                                | Unit       |
|--------------------------------------------------------------|-----------------------|-------------------------------------------------------------------------------------|-----------------|---------------------------------------------------|----------------------------------------------------|------------|
| Supply voltage <sup>(2)</sup>                                | $V_{DD}$              |                                                                                     | 1.95            | 2.8                                               | 3.6                                                | V          |
| Supply current in one-shot mode                              | $I_{dd}$              | $V_{DD} = 2.8V$ ,<br>EN is pulsed to $V_{DD}$ for 1 ms                              |                 | 400 <sup>(6)</sup> <sup>(9)</sup> <sup>(10)</sup> | 980 <sup>(2)</sup> <sup>(11)</sup> <sup>(12)</sup> | nA/Hz      |
| Supply current in shutdown mode                              | $I_{sd}$              | $V_{DD} = 2.8V$ , EN = 0                                                            |                 | 1.8 <sup>(6)</sup> <sup>(9)</sup>                 | 68 <sup>(2)</sup> <sup>(12)</sup>                  | nA         |
| Bypass capacitor at Byp pin <sup>(6)</sup>                   | $C_{byp}$             |                                                                                     | 70              | 100                                               | 470                                                | nF         |
| High level output voltage <sup>(2)</sup><br>Xout, Yout, Zout | $V_{oh}$              | $I_o = 500 \mu A$                                                                   | $0.85 * V_{DD}$ |                                                   |                                                    | V          |
| Low level output voltage <sup>(2)</sup><br>Xout, Yout, Zout  | $V_{ol}$              | $I_o = 500 \mu A$                                                                   |                 |                                                   | $0.15 * V_{DD}$                                    | V          |
| High level input voltage <sup>(2)</sup><br>EN                | $V_{ih}$              | $V_{DD} = 2.8V$                                                                     | $0.85 * V_{DD}$ |                                                   |                                                    | V          |
| Low level input voltage <sup>(2)</sup><br>EN                 | $V_{il}$              | $V_{DD} = 2.8V$                                                                     |                 |                                                   | $0.15 * V_{DD}$                                    | V          |
| Low level output voltage <sup>(7)</sup><br>SDA               | $V_{ols}$             | $I_o = 3 \text{ mA}$                                                                |                 |                                                   | 0.4                                                | V          |
| High level input voltage <sup>(7)</sup><br>SDA, SCL          | $V_{ih}$              | $V_{DD} = 2.8V$                                                                     | $0.7 * V_{DD}$  |                                                   |                                                    | V          |
| Low level input voltage <sup>(7)</sup><br>SDA, SCL           | $V_{il}$              | $V_{DD} = 2.8V$                                                                     |                 |                                                   | $0.3 * V_{DD}$                                     | V          |
| Output source current <sup>(2)</sup><br>Xout, Yout, Zout     | $I_{source}$          | Voltage high level $V_{out} = 0.85 * V_{DD}$ ,<br>$V_{DD} = 2.8V$                   |                 |                                                   | 7.3                                                | mA         |
| Output sink current <sup>(2)</sup><br>Xout, Yout, Zout       | $I_{sink}$            | Voltage low level $V_{out} = 0.15 * V_{DD}$ ,<br>$V_{DD} = 2.8V$                    |                 |                                                   | 8.9                                                | mA         |
| Turn-on time <sup>(14)</sup>                                 | $T_{on} / T_{active}$ | Measured from the time EN = 1.95V<br>to valid outputs                               |                 | 720 <sup>(6)</sup> <sup>(9)</sup> <sup>(10)</sup> | 900 <sup>(2)</sup> <sup>(11)</sup> <sup>(12)</sup> | $\mu s$    |
| Reset Time <sup>(7)</sup>                                    | $T_{rst}$             | $V_{DD} = 2.8V$ , the time between falling<br>edge of EN and next rising edge of EN | 1000            |                                                   |                                                    | $\mu s$    |
| Temperature range <sup>(2)</sup>                             | $T_{AGOC}$            |                                                                                     | -40             | 25                                                | 85                                                 | $^\circ C$ |

- Parameters tested 100% at final test at room temperature.
- Verified by characterization; not tested in production.
- Before board mount.
- Post-board mount offset specifications are based on a 4-layer PCB, relative to  $25^\circ C$ .
- All angles are based on the trip angle from static 0g to 1g; the g-values are calculated from the trip angle.
- Evaluation data: not tested in production.
- Guaranteed by design.
- Typical number is the target number unless otherwise specified.
- Typical number is mean data.
- Data is based on typical bypass cap = 100 nF.
- Data is based on max bypass cap = 470 nF.
- Over temperature  $-40^\circ C$  to  $85^\circ C$ .
- All numbers are based on  $V_{DD}$  cap = 4.7  $\mu F$ .
- For application connection, see [Figure 5 on page 6](#).

## 2.4

### Table 6. I<sup>2</sup>C slave timing values<sup>(1)</sup>

| Parameter                                                                             | Symbol              | I <sup>2</sup> C Fast Mode             |                    | Unit |
|---------------------------------------------------------------------------------------|---------------------|----------------------------------------|--------------------|------|
|                                                                                       |                     | Min                                    | Max                |      |
| SCL clock frequency                                                                   | f <sub>SCL</sub>    | 0                                      | 400                | kHz  |
| Bus-free time between STOP and START condition                                        | t <sub>BUF</sub>    | 1.3                                    |                    | μs   |
| (Repeated) START hold time                                                            | t <sub>HD;STA</sub> | 0.6                                    |                    | μs   |
| Repeated START setup time                                                             | t <sub>SU;STA</sub> | 0.6                                    |                    | μs   |
| STOP condition setup time                                                             | t <sub>SU;STO</sub> | 0.6                                    |                    | μs   |
| SDA data hold time                                                                    | t <sub>HD;DAT</sub> | 0.05                                   | 0.9 <sup>(2)</sup> | μs   |
| SDA setup time                                                                        | t <sub>SU;DAT</sub> | 100                                    |                    | ns   |
| SCL clock low time                                                                    | t <sub>LOW</sub>    | 1.3                                    |                    | μs   |
| SCL clock high time                                                                   | t <sub>HIGH</sub>   | 0.6                                    |                    | μs   |
| SDA and SCL rise time                                                                 | t <sub>r</sub>      | 20 + 0.1 C <sub>b</sub> <sup>(3)</sup> | 300                | ns   |
| SDA and SCL fall time                                                                 | t <sub>f</sub>      | 20 + 0.1 C <sub>b</sub> <sup>(3)</sup> | 300                | ns   |
| SDA valid time <sup>(4)</sup>                                                         | t <sub>VD;DAT</sub> |                                        | 0.9 <sup>(2)</sup> | μs   |
| SDA valid acknowledge time <sup>(5)</sup>                                             | t <sub>VD;ACK</sub> |                                        | 0.9 <sup>(2)</sup> | μs   |
| Pulse width of spikes on SDA and SCL that must be suppressed by internal input filter | t <sub>SP</sub>     | 0                                      | 50                 | ns   |
| Capacitive load for each bus line                                                     | C <sub>b</sub>      |                                        | 400                | pF   |

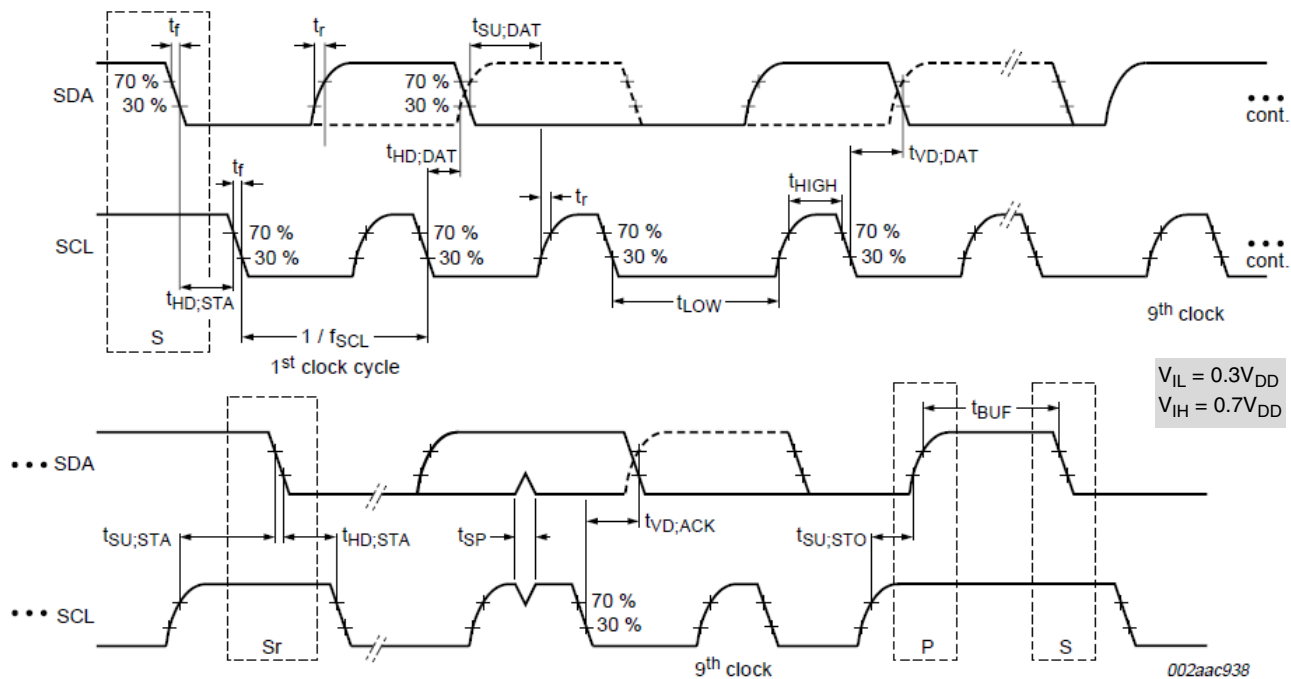
1.All values referred to  $V_{IH(min)}$  ( $0.3V_{DD}$ ) and  $V_{IL(max)}$  ( $0.7V_{DD}$ ) levels.

2. This device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal.

3.  $C_b$  = total capacitance of one bus line in pF.

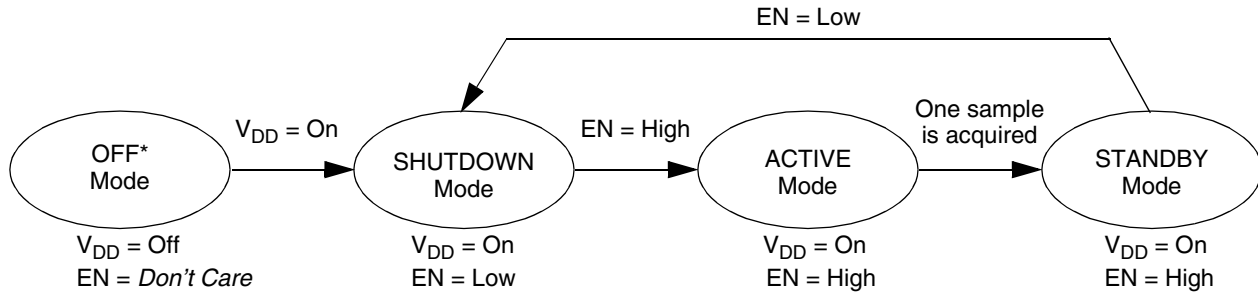
4.  $t_{\text{VP-DAT}}$  = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

5.  $t_{\text{YD\_ACK}}$  = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).



### Figure 6. I<sup>2</sup>C slave timing diagram

### 3 Modes of Operation



\*OFF mode can be entered from any state by removing the power.

Figure 7. MMA8491Q operating modes

Table 7. Operating modes

| Mode     | Conditions                                        | Function Description                                                                         | Digital Output State                                      |
|----------|---------------------------------------------------|----------------------------------------------------------------------------------------------|-----------------------------------------------------------|
| OFF      | $V_{DD} = \text{OFF}$<br>$EN = \text{Don't Care}$ | Device is powered off.                                                                       | Hi-Z                                                      |
| SHUTDOWN | $V_{DD} = \text{ON}$<br>$EN = \text{Low}$         | All blocks are shut down.                                                                    | Hi-Z                                                      |
| ACTIVE   | $V_{DD} = \text{ON}$<br>$EN = \text{High}$        | All blocks are enabled.<br>Device enters Standby mode automatically after data conversion.   | Deasserted, $X_{out} = 0$ , $Y_{out} = 0$ , $Z_{out} = 0$ |
| STANDBY  | $V_{DD} = \text{ON}$<br>$EN = \text{High}$        | Only digital output subsystem is enabled.<br>Data is valid and available only in this stage. | Active, I <sup>2</sup> C outputs become valid             |

#### 3.1 ACTIVE mode

The accelerometer subsystem is turned on at the rising edge of the EN pin, and acquires one sample for each of the three axes. Note that EN should not be asserted before  $V_{DD}$  reaches 1.95V. Samples are acquired, converted, and compensated for zero-g offset and gain errors, and then compared to an internal threshold value of 0.688g and stored.

- If any of the X, Y, Z axes sample's **absolute value** > **this threshold**, then the corresponding outputs on these axes drive logic highs.
- If any of the X, Y, Z axes sample's **absolute value** ≤ **this threshold**, then the corresponding outputs on these axes drive logic lows.

Read register 0x00 in this stage to determine whether the sample data is ready to be read.

#### 3.2 STANDBY mode

The device enter STANDBY mode automatically after the previously described function (powers into SHUTDOWN mode, ACTIVE mode) is accomplished. The digital output system outputs valid data, which can also be read via the I<sup>2</sup>C communication bus. This is the appropriate phase to read the measured data, either from the 3 push-pull logic outputs or through the I<sup>2</sup>C transaction. All other subsystems are turned off.

These outputs are held until the MMA8491Q operation mode changes. For lower power consumption, deassert the EN pin as soon as data is read (to enter SHUTDOWN mode).

#### 3.3 Next sample acquisition

The MMA8491Q needs to be brought back to the ACTIVE mode again by pulling EN pin up to a Logic 1. Another option is to power down the device and start from OFF mode as illustrated in Figure 7.

For applications where sampling intervals are greater than 30 seconds, the host can shut off the tilt sensor power after acquisition of tilt sensor output data to conserve energy and prolong battery life.

### 3.4 Power-up timing sequences

The power-up timing sequence for MMA84591Q is shown in Figure 8, where  $V_{DD}$  is powered and the EN pin is activated to acquire a single sample. Additional samples can be acquired by repeating the EN pulse.

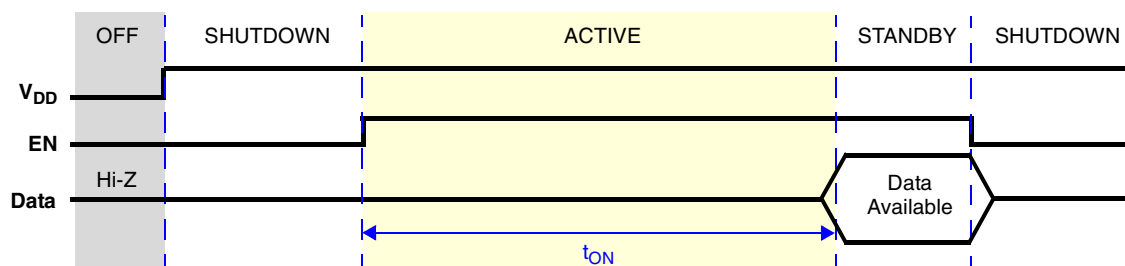


Figure 8. MMA8491Q timing sequence

$t_{ON}$  is the time between EN to the end of ACTIVE stage, after which the newly acquired sample data is available.

### 3.5 45° tilt detection

The output value changes according to the **absolute value** of the acceleration of the MMA8491Q compared to the threshold:

- When the acceleration's **absolute value** > the threshold 0.688g, the output = '1'.
- When the acceleration's **absolute value** ≤ the threshold, the output = '0'.

$$Output = \begin{cases} 1, & \text{when } (|g\text{-value}| > 0.688g) \\ 0, & \text{when } (|g\text{-value}| \leq 0.688g) \end{cases}$$

For example,

- When the MMA8491Q is set on a table, it senses 1g acceleration on Z-axis and senses 0g on X and Y axes.
- When the MMA8491Q is flipped upside down on the table, it senses -1g acceleration on Z-axis and senses 0g on X and Y axes.

In both cases  $X_{out} = 0$ ,  $Y_{out} = 0$ , and  $Z_{out} = 1$ .

### 3.6 Tilt angle

Tilt angles can be calculated from the g-value threshold using the equation below. The tilt threshold is 0.688g, which corresponds to 43.5°. [Figure 9](#) illustrates the tilt angle threshold.

$$\text{Tilt Angle} = \text{asin}\left(\frac{\text{g-value}}{1g}\right)$$

- When 0g acceleration is present on an axis, the tilt angle = 0°; when 1g acceleration is present on an axis, the tilt angle = 90°.
- When the tilt angle > the tilt threshold, the output for the axis is HIGH; when the tilt angle ≤ the tilt threshold, the output for the axis is LOW.

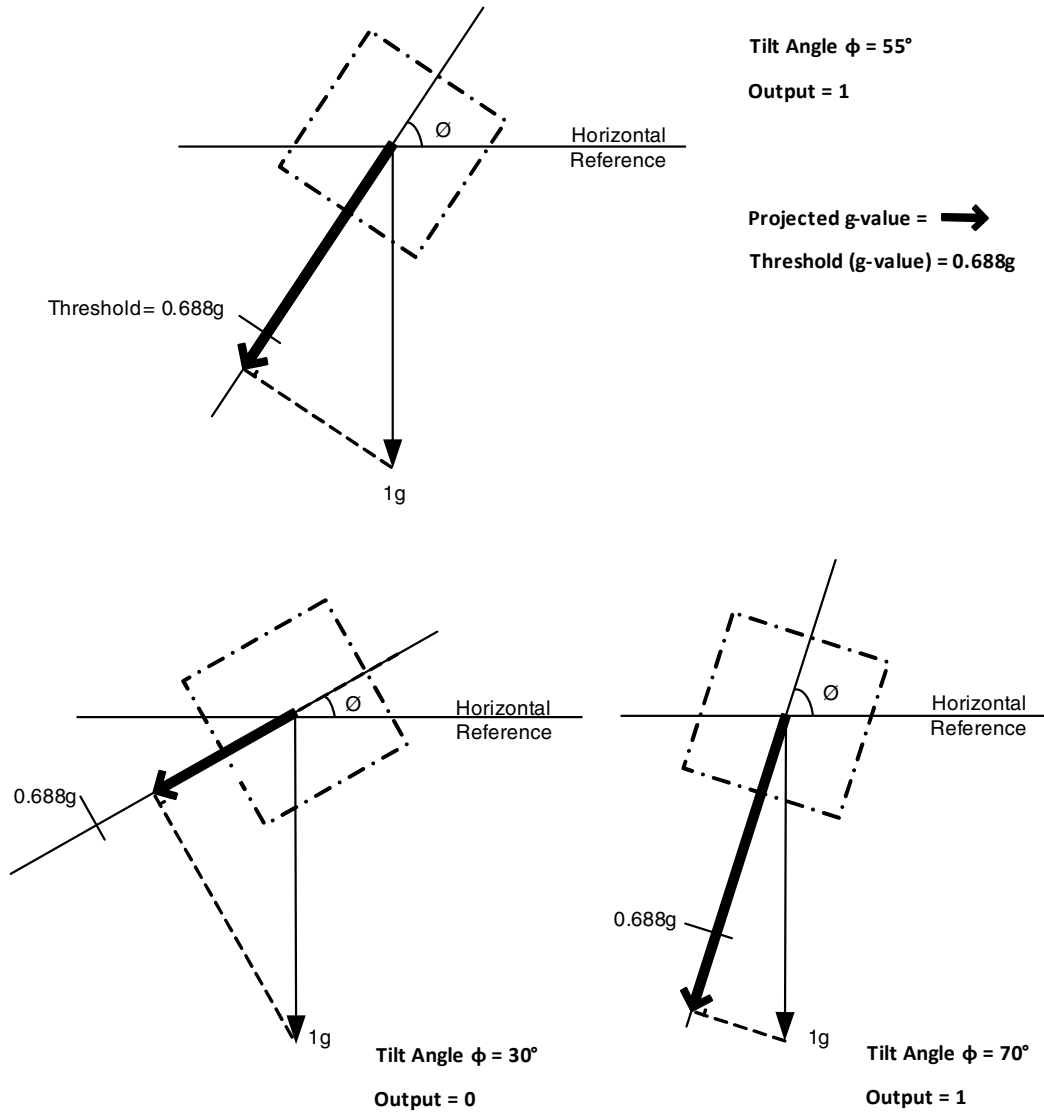


Figure 9. MMA8491Q output is based on tilt angle and sensor g-value

## 4 Serial Interface (I<sup>2</sup>C)

Acceleration data may be accessed through an I<sup>2</sup>C interface thus making the device particularly suitable for direct interfacing with a microcontroller. The MMA8491Q features three interrupt signals which indicate the tilt-sensing results on X, Y, Z axis respectively. The raw accelerometer data are readable via I<sup>2</sup>C at the same time when interrupt signal is available.

The registers embedded inside the MMA8491Q are accessible through the I<sup>2</sup>C serial interface (Table 8). To enable the I<sup>2</sup>C interface, the EN pin must be HIGH. If either EN or V<sub>DD</sub> are absent, the MMA8491Q I<sup>2</sup>C interface reads invalid data. The I<sup>2</sup>C interface may be used for communications along with other I<sup>2</sup>C devices. Removing power from the V<sub>DD</sub> pin of the MMA8491Q does not affect the I<sup>2</sup>C bus.

**Table 8. Serial interface pins**

| Pin | Description                   |
|-----|-------------------------------|
| SCL | I <sup>2</sup> C Serial Clock |
| SDA | I <sup>2</sup> C Serial Data  |

There are two signals associated with the I<sup>2</sup>C bus; the Serial Clock Line (SCL) and the Serial Data Line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. External pullup resistors connected to V<sub>DD</sub> are expected for SDA and SCL. When the bus is free both the lines are HIGH. The I<sup>2</sup>C interface is compliant with Fast mode (400 kHz, Table 6).

### 4.1 I<sup>2</sup>C operation

The transaction on the bus is started through a start condition (START) signal. A START condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH.

After START has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after START contains the slave address in the first 7 bits, and the 8th bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first 7 bits after a start condition with its address. If they match, then the device considers itself addressed by the Master.

The 9th clock pulse, following the slave address byte (and each subsequent byte), is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line LOW so that it remains stable low during the high period of the acknowledge clock period.

A LOW-to-HIGH transition on SDA while SCL is HIGH is defined as a stop condition (STOP). A data transfer is always terminated by a STOP.

A Master may also issue a repeated START during a data transfer. The MMA8491Q expects repeated STARTs to be used to randomly read from specific registers.

The MMA8491Q accelerometer standard 7-bit slave address is 01010101(0x55).

**Table 9. I<sup>2</sup>C device address sequence**

| Command | [7:1]<br>Device Address | [7:1]<br>Device Address | [0]<br>R/W | [7:0]<br>8-bit Final Value |
|---------|-------------------------|-------------------------|------------|----------------------------|
| Read    | 01010101                | 0x55                    | 1          | 0xAB                       |
| Write   | 01010101                | 0x55                    | 0          | 0xAA                       |

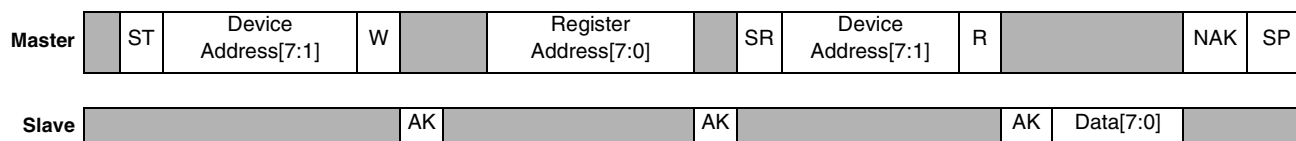
### 4.2 Single byte read

The transmission of an 8-bit command begins on the falling edge of SCL. After the 8 clock cycles are used to send the command, note that the data returned is sent with the MSB first after the data is received. Figure 10 shows the timing diagram for the accelerometer 8-bit I<sup>2</sup>C read operation.

1. The Master (or MCU) transmits a start condition (ST) to the MMA8491Q, slave address (0x55), with the R/W bit set to "0" for a write, and the MMA8491Q sends an acknowledgement.
2. Then the Master (or MCU) transmits the address of the register to read and the MMA8491Q sends an acknowledgement.
3. The Master (or MCU) transmits a repeated start condition (SR) and then addresses the MMA8491Q (0x1D) with the R/W bit set to "1" for a read from the previously selected register.
4. The Slave then acknowledges and transmits the data from the requested register.
5. The Master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer.

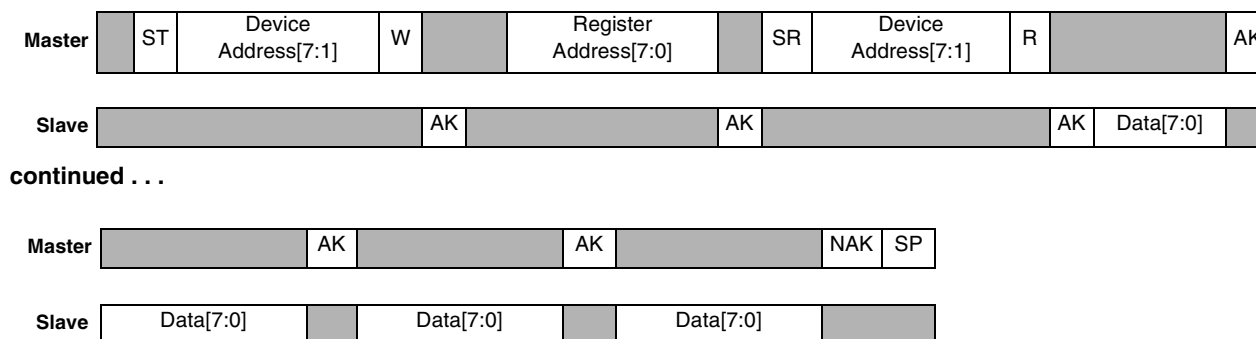
**Legend**

|                              |                    |                     |              |
|------------------------------|--------------------|---------------------|--------------|
| ST: Start Condition          | SP: Stop Condition | NAK: No Acknowledge | W: Write = 0 |
| SR: Repeated Start Condition | AK: Acknowledge    | R: Read = 1         |              |

**Figure 10. Single byte read**

### 4.3 Multiple byte read

When performing a multibyte read or “burst read”, the MMA8491Q automatically increments the received register address commands after a read command is received. Therefore, after following the steps of a single byte read, multiple bytes of data can be read from sequential registers after each MMA8491Q acknowledgment (AK) is received, until a no acknowledge (NAK) occurs from the Master, followed by a stop condition (SP) signaling an end of transmission.

**Figure 11. Multiple byte read**

## 5 Register Descriptions

### 5.1 Register address map

Table 10. Register address map<sup>(1)(2)</sup>

| Name      | Type | Register Address | Auto-Increment Address <sup>(3)</sup> | Default | Comment                               |
|-----------|------|------------------|---------------------------------------|---------|---------------------------------------|
| STATUS    | R    | 0x00             | 0x01                                  | 0x00    | Read time status                      |
| OUT_X_MSB | R    | 0x01             | 0x02                                  | Output  | [7:0] are 8 MSBs of the 14-bit sample |
| OUT_X_LSB | R    | 0x02             | 0x03                                  | Output  | [7:2] are the 6 LSB of 14-bit sample  |
| OUT_Y_MSB | R    | 0x03             | 0x04                                  | Output  | [7:0] are 8 MSBs of the 14-bit sample |
| OUT_Y_LSB | R    | 0x04             | 0x05                                  | Output  | [7:2] are the 6 LSB of 14-bit sample  |
| OUT_Z_MSB | R    | 0x05             | 0x06                                  | Output  | [7:0] are 8 MSBs of the 14-bit sample |
| OUT_Z_LSB | R    | 0x06             | <b>0x00</b>                           | Output  | [7:2] are the 6 LSB of 14-bit sample  |

1. Register contents are preserved when EN pin is set high after sampling.
2. Register contents are reset when EN pin is set low.
3. Auto-increment is the I<sup>2</sup>C feature that the I<sup>2</sup>C read address is automatically updated after each read. Auto-increment addresses which are not a simple increment are highlighted in **bold**. The auto-increment addressing is only enabled when device registers are read using I<sup>2</sup>C burst read mode. Therefore the internal storage of the auto-increment address is cleared whenever a stop-bit is detected.

### 5.2 Register bit map

Table 11. Register bit map

| Address Offset | Name      |   | 7        | 6 | 5 | 4 | 3     | 2   | 1   | 0   |
|----------------|-----------|---|----------|---|---|---|-------|-----|-----|-----|
| 0x00           | STATUS    | R | 0        | 0 | 0 | 0 | ZYXDR | ZDR | YDR | XDR |
| 0x01           | OUT_X_MSB | R | XD[13:6] |   |   |   |       |     |     |     |
| 0x02           | OUT_X_LSB | R | XD[5:0]  |   |   |   |       |     | 0   | 0   |
| 0x03           | OUT_Y_MSB | R | YD[13:6] |   |   |   |       |     |     |     |
| 0x04           | OUT_Y_LSB | R | YD[5:0]  |   |   |   |       |     | 0   | 0   |
| 0x05           | OUT_Z_MSB | R | ZD[13:6] |   |   |   |       |     |     |     |
| 0x06           | OUT_Z_LSB | R | ZD[5:0]  |   |   |   |       |     | 0   | 0   |

## 5.3 Data registers

### 5.3.1 0x00 Status register

Register 0x00 reflects the real-time status information of the X, Y, and Z sample data. The data read bits (ZYXDR, ZDR, YDR, XDR) are set when samples are taken and ready to be read.

**Table 12. STATUS register**

| Field | Description                                                                                                                                                                                                                                                                                                                                                                          |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ZYXDR | <b>X, Y, Z-axis new Data Ready</b> (and available) <ul style="list-style-type: none"><li>• ZYXDR signals that a new sample for all channels is available.</li><li>• ZYXDR is cleared when the high-bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all channels are read.</li></ul> 0: No new set of data ready (default value)<br>1: A new set of data is ready |
| ZDR   | <b>Z-axis new Data Ready</b> (and available) <ul style="list-style-type: none"><li>• ZDR is set whenever a new acceleration sample related to the Z-axis is generated.</li><li>• ZDR is cleared anytime OUT_Z_MSB register is read.</li></ul> 0: No new Z-axis data is ready (default value)<br>1: A new Z-axis data is ready                                                        |
| YDR   | <b>Y-axis new Data Ready</b> (and available) <ul style="list-style-type: none"><li>• YDR is set whenever a new acceleration sample related to the Y-axis is generated.</li><li>• YDR is cleared anytime OUT_Y_MSB register is read.</li></ul> 0: No new Y-axis data ready (default value)<br>1: A new Y-axis data is ready                                                           |
| XDR   | <b>X-axis new Data Ready</b> (and available) <ul style="list-style-type: none"><li>• XDR is set whenever a new acceleration sample related to the X-axis is generated.</li><li>• XDR is cleared anytime OUT_X_MSB register is read.</li></ul> 0: No new X-axis data ready (default value)<br>1: A new X-axis data is ready                                                           |

### 5.3.2 Accelerometer data registers (0x01–0x06)

These registers contain the X-axis, Y-axis, and Z-axis 14-bit output sample data (expressed as 2's complement numbers).

- OUT\_X\_MSB, OUT\_X\_LSB, OUT\_Y\_MSB, OUT\_Y\_LSB, OUT\_Z\_MSB, and OUT\_Z\_LSB are stored in the auto-incrementing address range of 0x01 – 0x06.
- The LSB registers can only be read immediately following the read access of the corresponding MSB register. A random read access to the LSB registers is not possible.
- Reading the MSB register and then the LSB register in sequence ensures that both bytes (LSB and MSB) belong to the same data sample, even if a new data sample arrives between reading the MSB and the LSB byte.
- The accelerometer data registers should be read only after the status register has confirmed that new data on all axes is available.

**Table 13. OUT\_X\_MSB: X\_MSB register (0x01, Read-only)**

| Bit 7    | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------|-------|-------|-------|-------|-------|-------|
| XD[13:7] |       |       |       |       |       |       |       |

**Table 14. OUT\_X\_LSB: X\_LSB register (0x02, Read-only)**

| Bit 7   | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|
| XD[5:0] |       |       |       |       |       | 0     | 0     |

**Table 15. OUT\_Y\_MSB: Y\_MSB register (0x03, Read-only)**

| Bit 7    | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------|-------|-------|-------|-------|-------|-------|
| YD[13:6] |       |       |       |       |       |       |       |

**Table 16. OUT\_Y\_LSB: Y\_LSB register (0x04, Read-only)**

| Bit 7   | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|
| YD[5:0] |       |       |       |       |       | 0     | 0     |

**Table 17. OUT\_Z\_MSB: Z\_MSB register (0x05, Read-only)**

| Bit 7    | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------|-------|-------|-------|-------|-------|-------|
| ZD[13:6] |       |       |       |       |       |       |       |

**Table 18. OUT\_Z\_LSB: Z\_LSB register (0x06, Read-only)**

| Bit 7   | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|
| ZD[5:0] |       |       |       |       |       | 0     | 0     |

## 5.4 Accelerometer output conversion

**Table 19. Accelerometer output data**

| 14-bit Data       | Range $\pm 8g$<br>(1 mg/count) |
|-------------------|--------------------------------|
| 01 1111 1111 1111 | +8.000g                        |
| 01 1111 1111 1110 | +7.998g                        |
| ...               | ...                            |
| 00 0000 0000 0000 | 0.000g                         |
| 11 1111 1111 1111 | -0.001g                        |
| ...               | ...                            |
| 10 0000 0000 0001 | -7.998g                        |
| 10 0000 0000 0000 | -8.000g                        |

## 6 Mounting Guidelines

Surface mount printed circuit board (PCB) layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the PCB and the package. With the correct footprint, the packages will self-align when subjected to a solder reflow process. The purpose is to minimize the stress on the package after board mounting. The MMA8491Q accelerometers use the QFN package. This section describes suggested methods of soldering and mounting these devices to the PCB for consumer applications.

### 6.1 Overview of soldering considerations

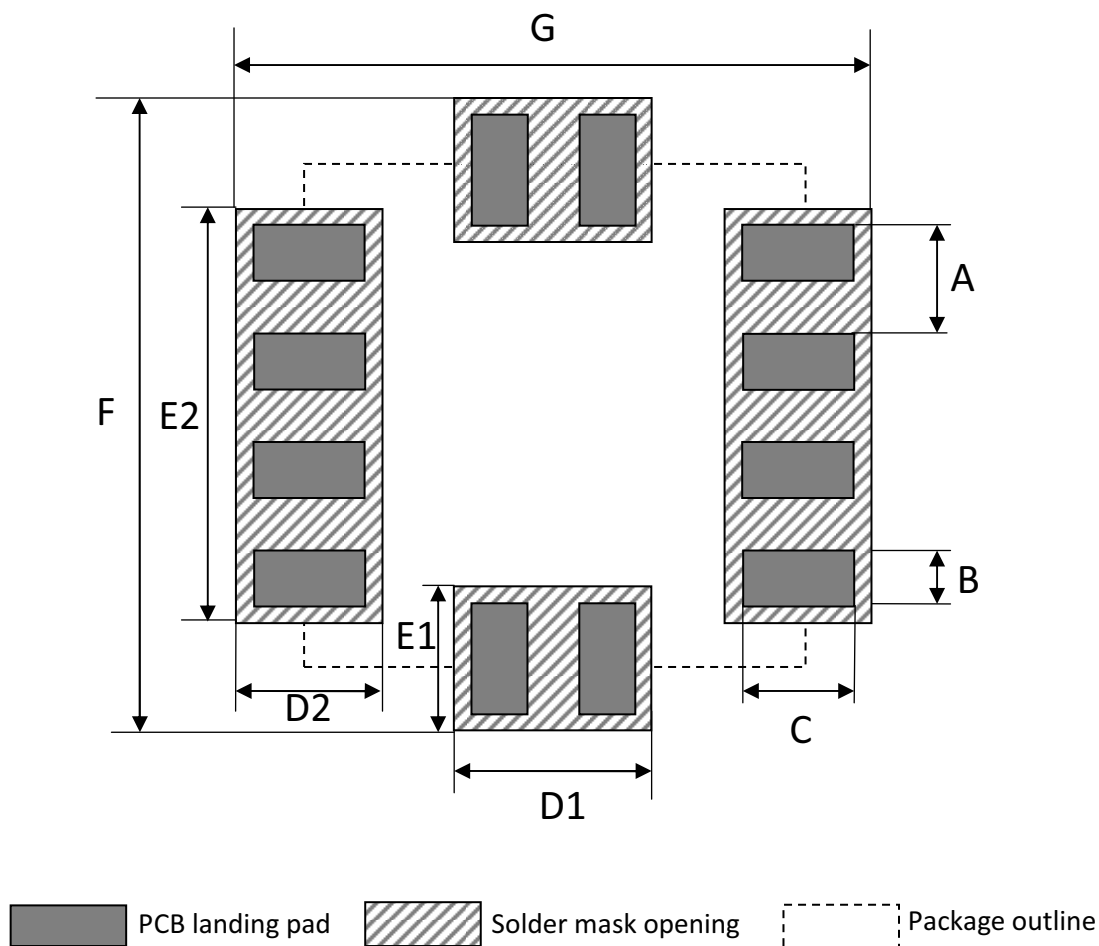
The information provided here is based on experiments executed on QFN devices. They do not represent exact conditions present at a customer site. Hence, information herein should be used as guidance only and process and design optimizations are recommended to develop an application specific solution. It should be noted that with the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

### 6.2 Halogen content

This package is designed to be Halogen Free, exceeding most industry and customer standards. Halogen Free means that no homogeneous material within the assembly package shall contain chlorine (Cl) in excess of 700 ppm or 0.07% weight/weight or bromine (Br) in excess of 900 ppm or 0.09% weight/weight.

### 6.3 PCB mounting recommendations

1. Do not solder down Exposed Pad (EP) under the package to minimize board mounting stress impact to product performance.
2. PCB landing pad is 0.675 mm x 0.325 mm as shown in [Figure 12](#).
3. Solder mask opening = PCB land pad edge + 0.2 mm larger all around.
4. Stencil opening size is 0.625 mm x 0.3 mm.
5. Stencil thickness is 100 or 125  $\mu$ m.
6. The solder mask should not cover any of the PCB landing pads, as shown in [Figure 12](#).
7. No additional via nor metal pattern underneath package on the top of the PCB layer.
8. Do not place any components or vias within 2 mm of the package land area. This may cause additional package stress if it is too close to the package land area.
9. Signal traces connected to pads should be as symmetric as possible. Put dummy traces on NC pads, to have same length of exposed trace for all pads.
10. Use a standard pick and place process and equipment. Do not use a hand soldering process.
11. Customers are advised to be cautious about the proximity of screw down holes to the sensor, and the location of any press fit to the assembled PCB when in an enclosure. It is important that the assembled PCB remain flat after assembly to keep electronic operation of the device optimal.
12. The PCB should be rated for the multiple lead-free reflow condition with max 260°C temperature.
13. Freescale sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide free molding compound (green) and lead-free terminations. These terminations are compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

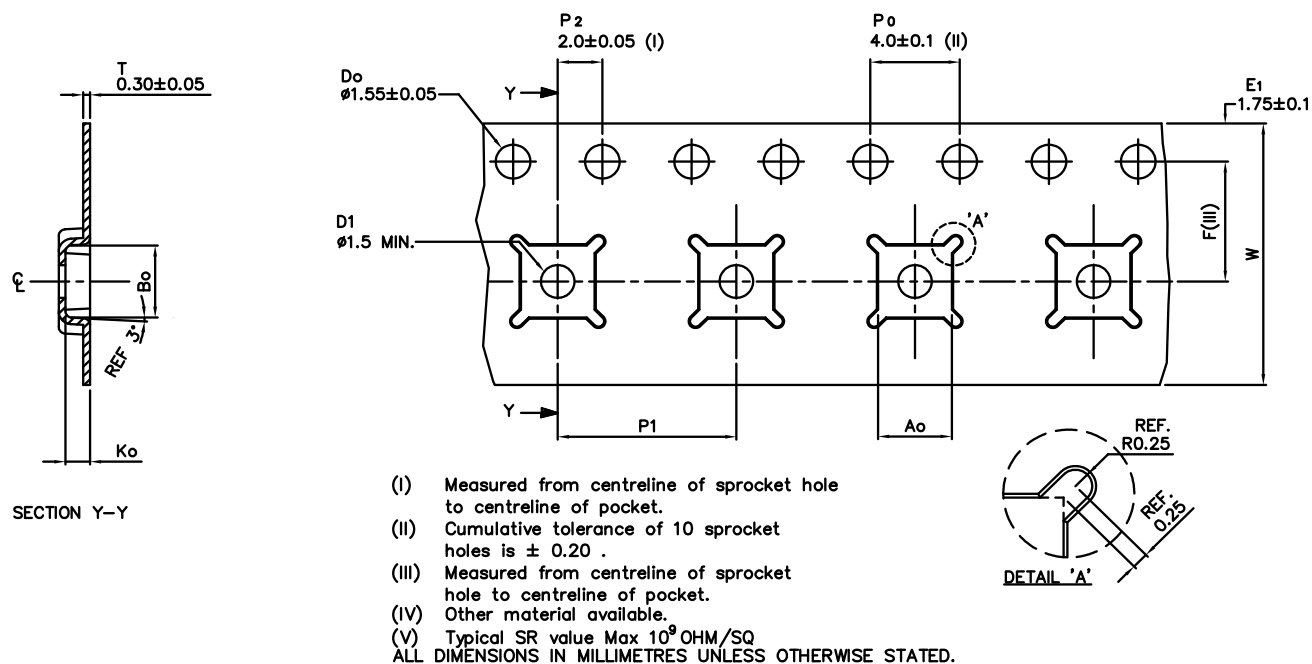


| Symbol | Description                | Value (mm) |
|--------|----------------------------|------------|
| A      | Pitch                      | 0.650      |
| B      | Landing Pad Width          | 0.325      |
| C      | Landing Pad Length         | 0.675      |
| D1     | Solder Mask Pattern Width  | 1.175      |
| D2     | Solder Mask Pattern Length | 0.875      |
| E1     | Solder Mask Pattern Width  | 0.875      |
| E2     | Solder Mask Pattern Length | 2.475      |
| F      | I/O Pads Extended Length   | 3.8        |
| G      | I/O Pads Extended Length   | 3.8        |

**Figure 12. PCB footprint guidelines**

## 7 Tape and Reel

### 7.1 Tape dimensions



|    |               |
|----|---------------|
| Ao | 3.30 +/– 0.1  |
| Bo | 3.30 +/– 0.1  |
| Ko | 1.10 +/– 0.1  |
| F  | 5.50 +/– 0.05 |
| P1 | 8.00 +/– 0.1  |
| W  | 12.00 +/– 0.3 |

Measurements are in millimeters.

Figure 13. Mechanical dimensions

### 7.2 Label and device orientation

MMA8491Q is oriented on the tape as illustrated in Figure 14. The front side dot marked on the device indicates pin 1.

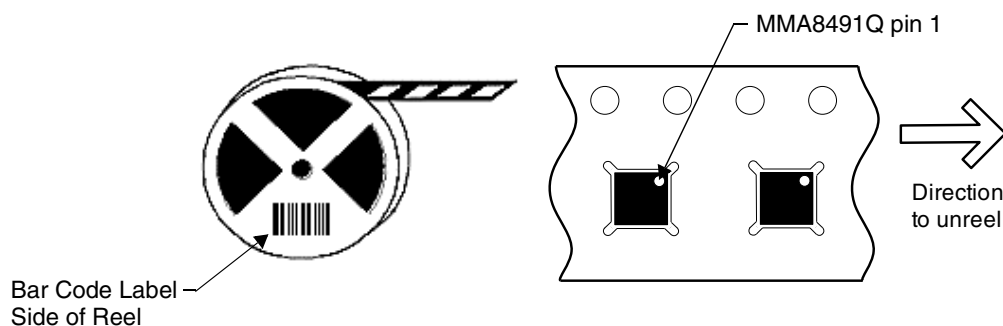


Figure 14. Tape and reel orientation

## 8 Package Dimensions

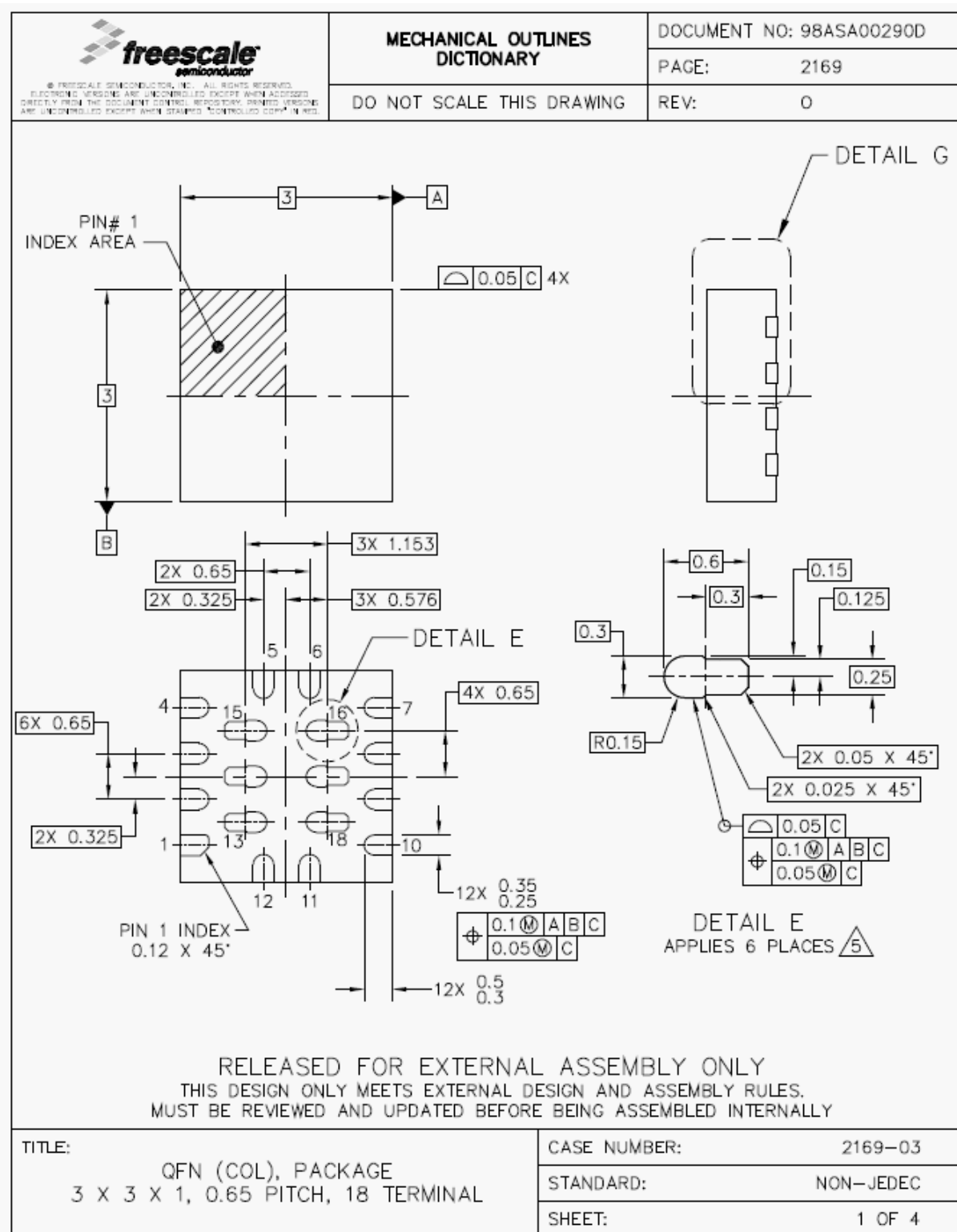
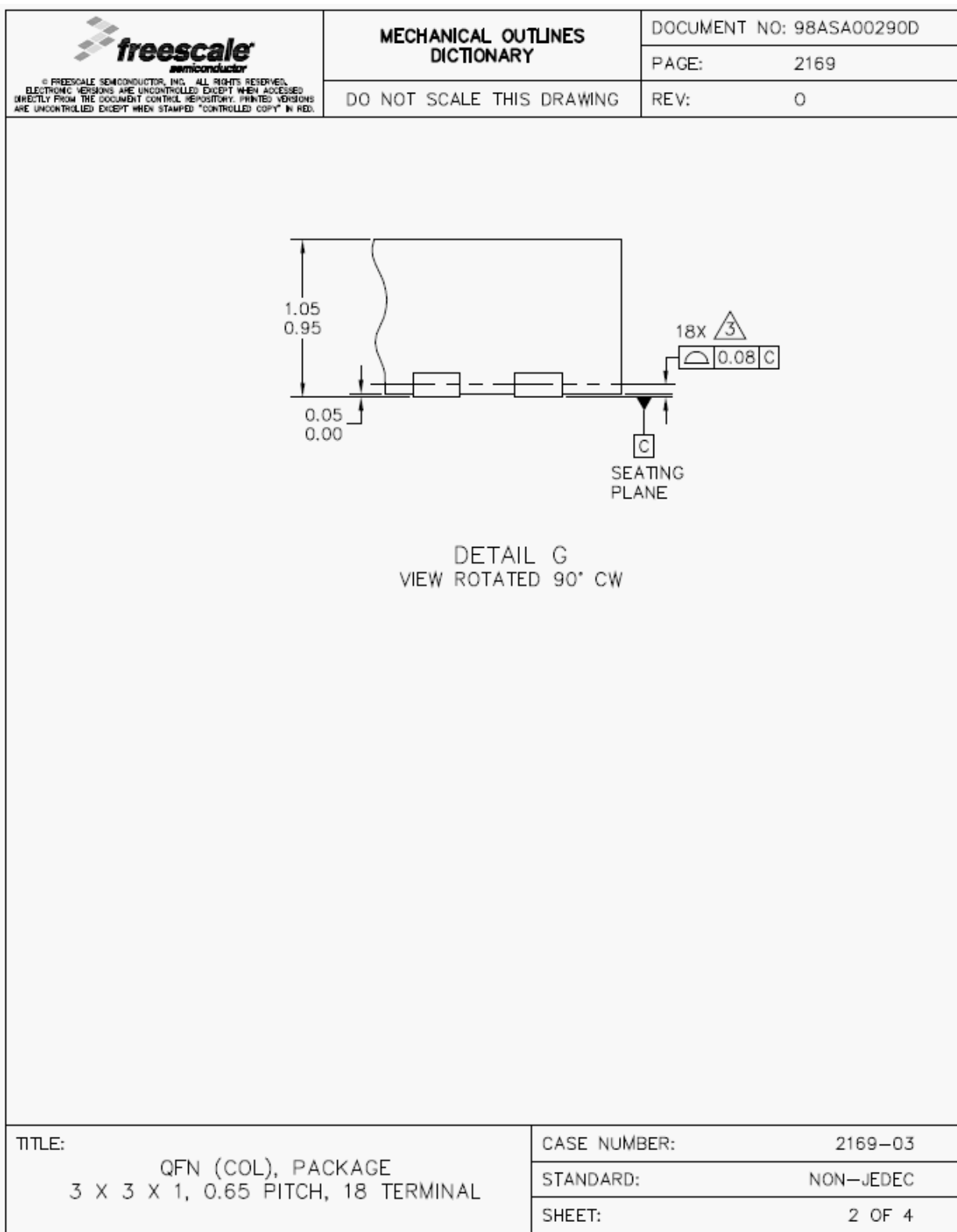


Figure 15. Case 2169-02, Issue X1, 12-Lead QFN—page 1



**Figure 16. Case 2169-02, Issue X1, 12-Lead QFN—page 2**

|                                                                                                                                                                                                                                                                                                                                                                |                                           |                      |                          |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|----------------------|--------------------------|
| <br><small>© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.<br/>ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSSED<br/>DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED VERSIONS<br/>ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.</small> | <b>MECHANICAL OUTLINES<br/>DICTIONARY</b> |                      | DOCUMENT NO: 98ASA00290D |
|                                                                                                                                                                                                                                                                                                                                                                | DO NOT SCALE THIS DRAWING                 |                      | PAGE: 2169               |
|                                                                                                                                                                                                                                                                                                                                                                |                                           |                      | REV: 0                   |
| <p>NOTES:</p> <p>1. ALL DIMENSIONS ARE IN MILLIMETERS.</p> <p>2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.</p> <p>3. COPLANARITY APPLIES TO LEADS.</p> <p>4. MIN. METAL GAP SHOULD BE 0.2 MM.</p> <p>5. LEADS 13 TO 18 ARE NOT SOLDERABLE.</p>                                                                                                        |                                           |                      |                          |
| TITLE:<br>QFN (COL), PACKAGE<br>3 X 3 X 1, 0.65 PITCH, 18 TERMINAL                                                                                                                                                                                                                                                                                             |                                           | CASE NUMBER: 2169-03 |                          |
|                                                                                                                                                                                                                                                                                                                                                                |                                           | STANDARD: NON-JEDEC  |                          |
|                                                                                                                                                                                                                                                                                                                                                                |                                           | SHEET: 3 OF 4        |                          |

Figure 17. Case 2169-02, Issue X1, 12-Lead QFN—page 3

## 9 Revision History

Table 20. Revision history

| Revision number | Revision date | Description of changes                                    |
|-----------------|---------------|-----------------------------------------------------------|
| 1               | 10/2012       | • Initial release                                         |
| 2               | 11/2012       | • Characterization data verified to be complete and final |

---

***How to Reach Us:*****Home Page:**

freescale.com

**Web Support:**

freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [freescale.com/SalesTermsandConditions](http://freescale.com/SalesTermsandConditions).

Freescale, the Freescale logo, Altivec, C-5, CodeTest, CodeWarrior, ColdFire, C-Ware, Energy Efficient Solutions logo, Kinetis, mobileGT, PowerQUICC, Processor Expert, QorIQ, Qorivva, StarCore, Symphony, and VortiQa are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Airfast, BeeKit, BeeStack, ColdFire+, CoreNet, Flexis, MagniV, MXC, Platform in a Package, QorIQ Qonverge, QUICC Engine, Ready Play, SafeAssure, SMARTMOS, TurboLink, Vybrid, and Xtrinsic are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2012 Freescale Semiconductor, Inc.

Document Number: MMA8491Q

Rev 2.0

11/2012

