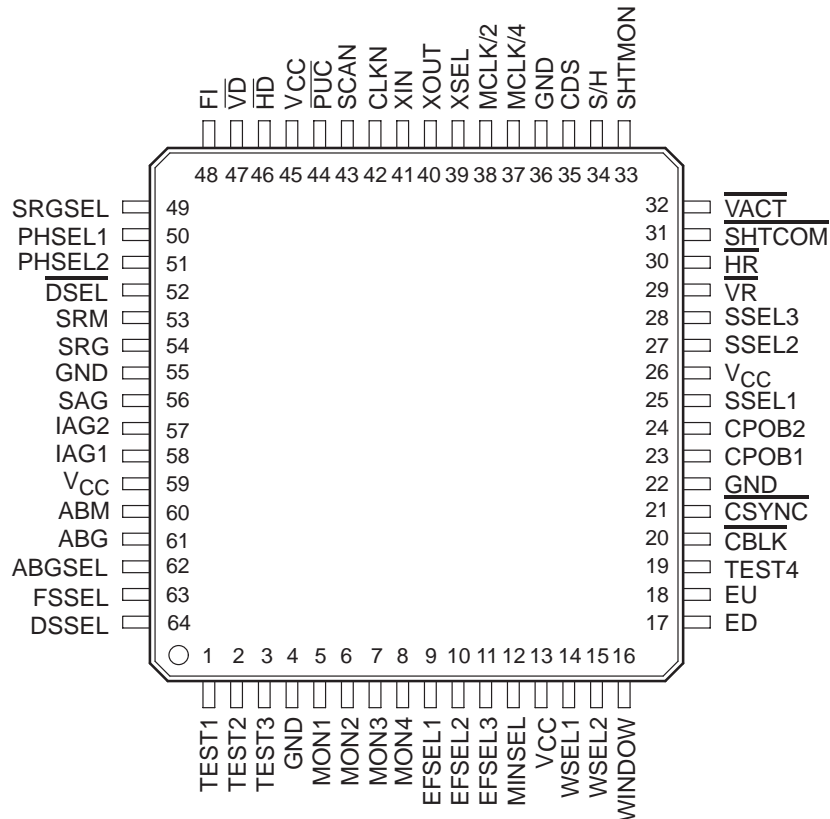


- EIA-170 Timing Operation
- Solid-State Reliability
- Fixed Electronic-Shutter Options
- Random Shutter-Mode
- Flicker-Compensation Mode
- Auto-Iris Capability
- Electronic-Windowing Options
- Horizontal and Vertical Resets for External Synchronization
- Double-Speed Readout Option



description

The TMC57750 is a monolithic integrated circuit designed to supply timing signals for the Texas Instruments (TI™) 4-mm TC255 monochrome CCD image sensor. The TMC57750 supplies both CCD drive signals and EIA-170 television-synchronization signals at standard video rates. It requires a single 5-V supply voltage and a 25-MHz timing crystal or crystal oscillator. The TMC57750 provides the user with several options including antiblooming-frequency selection, external synchronization, fixed electronic-shutter selection, electronic auto-iris, and window selection.

The TMC57750 is designed to drive the TC255 CCD image sensor through an intermediary level-shifting device such as the TI TMC57253 serial and parallel driver. It supplies sampling, clamping, and synchronizing signals for the TI SN76121OFR video processor. The TMC57750 EIA-170 synchronization signals include composite sync, composite blank, and field indicator.

The TMC57750 is supplied in a 64-pin plastic flat package and is characterized for operation from –20°C to 45°C.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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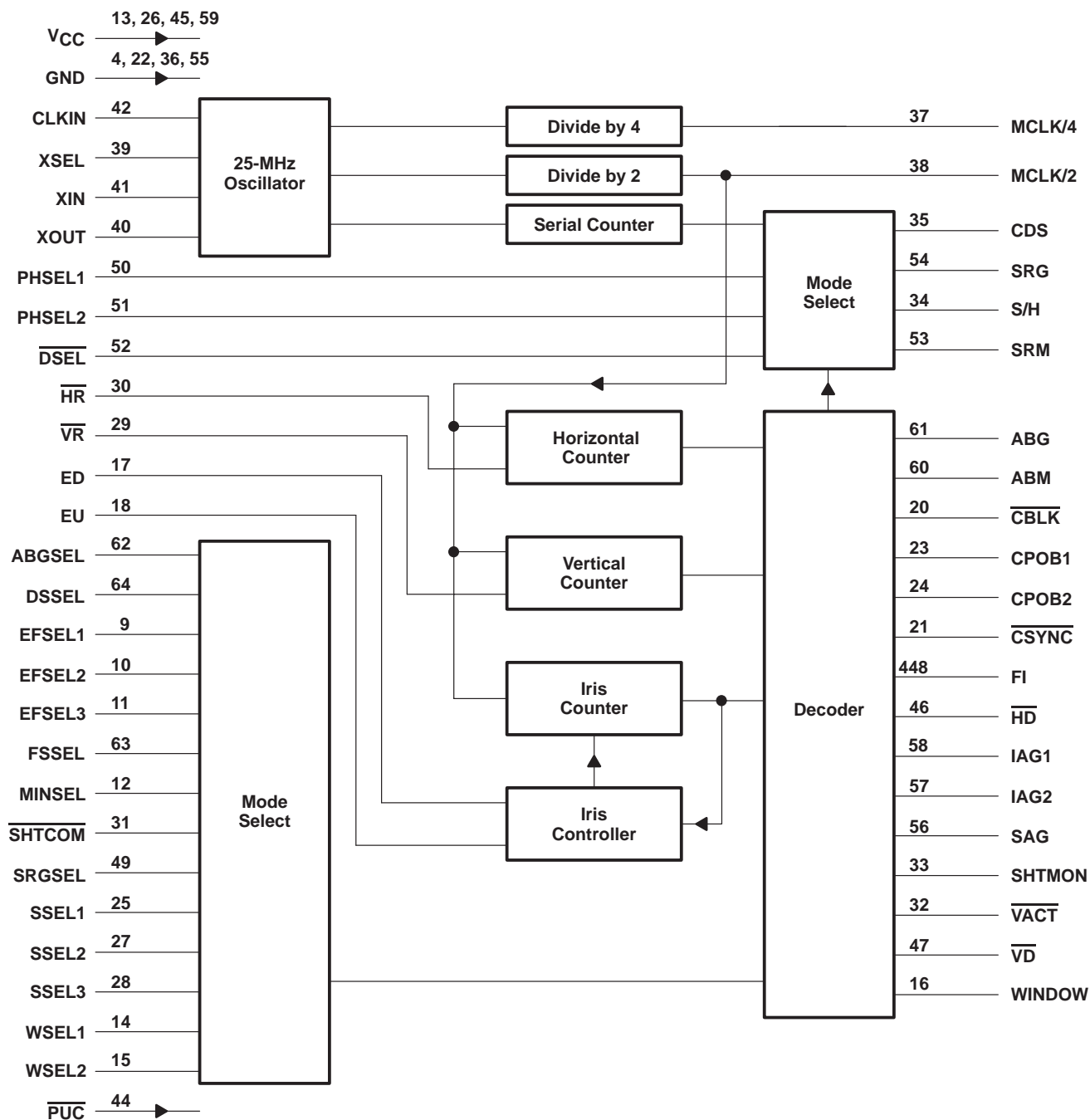
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TMC57750

1/4-INCH RS-170 TIMER

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functional block diagram



Terminal Functions

TERMINAL NAME		NO.	I/O	DESCRIPTION															
ABG		61	O	Antiblooming gate															
ABM		60	O	Antiblooming gate mid-level															
ABGSEL		62	I	Antiblooming-gate select. ABGSEL selects the frequency of the antiblooming gate. When ABGSEL is high, the standard frequency of 6.25 MHz is selected. When low, the double frequency of 12.5 MHz is selected.															
CLKIN		42	I	Clock in															
CBLK		20	O	Composite blank															
CPOB1		23	O	Optical black clamp one															
CPOB2		24	O	Optical black clamp two															
CSYNC		21	O	Composite sync															
CDS		35	O	Co9rrelated double sampling															
DSEL		52	I	Delay select. DSEL selects the delay of CDS and S/H with respect to SRG. When DSEL is high, a standard delay is selected. When low, an additional delay of 5 ns is selected.															
DSSEL		64	I	Display-scan select. DSSEL selects the display-scanning mode. When DSSEL is high, the interlace mode is selected. When low, the noninterlace mode is selected. In the interlace mode, one field is 262.5 horizontal lines and one frame is 525 horizontal lines. In the noninterlace mode, one field is 262 horizontal lines and one frame is 524 horizontal lines.															
ED		17	I	Exposure down. ED decreases the integration of the CCD sensor.															
EU		18	I	Exposure up. EU increases the integration of the CCD sensor.															
EFSEL1, EFSEL2, EFSEL3		9, 10, 11	I	Electronic-function select. EFSEL1, EFSEL2, and EFSEL3 selects the operational modes (see Table 1 and Figure 4).															
FI		49	O	Field index															
FSSEL		63	I	Frame-shift select. FSSEL selects the parallel-transfer frequency. When FSSEL is high, the standard frequency of 12.5 MHz is selected. When low, the double frequency of 25 MHz is selected.															
GND		4, 22, 36, 55		Ground															
HD		46	O	Horizontal drive															
HR		30	I	Horizontal reset															
IAG1		58	O	Image-area gate 1															
IAG2		57	O	Image-area gate 2															
MCLK/4		37	O	Master clock divided by 4															
MCLK/2		38	O	Master clock divided by 2															
MINSEL		12	I	Minimum exposure-time select. MINSEL selects the minimum exposure time for the auto-iris mode. When high, the exposure time of 1/50000 second is selected. When low, the exposure time of 1/8000 second is selected.															
MON1, MON2, MON3, MON4		5, 6, 7, 8	O	MON1, MON2, MON3, and MON4 are test-monitoring terminals and are not used in normal operation.															
PHSEL1, PHSEL2		50, 51	I	<div>Phase select. PHSEL1 and PHSEL2 determine the timing relation of S/H and CDS with respect to SRG.</div> <table><thead><tr><th>PHSEL1</th><th>PHSEL2</th><th>OPERATION</th></tr></thead><tbody><tr><td>H</td><td>H</td><td>MODE1</td></tr><tr><td>L</td><td>H</td><td>MODE2</td></tr><tr><td>H</td><td>L</td><td>MODE3</td></tr><tr><td>L</td><td>L</td><td>MODE4</td></tr></tbody></table> <div>MODES1, 2, 3, and 4 are shown in Figure 3.</div>	PHSEL1	PHSEL2	OPERATION	H	H	MODE1	L	H	MODE2	H	L	MODE3	L	L	MODE4
PHSEL1	PHSEL2	OPERATION																	
H	H	MODE1																	
L	H	MODE2																	
H	L	MODE3																	
L	L	MODE4																	

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Terminal Functions (Continued)

TERMINAL NAME NO.		I/O	DESCRIPTION															
PUC	44	I	Power-up clear															
SAG	56	O	Storage-area gate															
SCAN	43		SCAN is a test point and is not used in normal operation.															
SHTCOM	31	I	Shutter command															
SRG	54	O	Serial-register gate															
SRM	53	O	Serial-register gate mid-level															
SRGSEL	49	I	Serial-register gate select. SRGSEL selects the readout frequency. When SRGSEL is high, the standard frequency of 6.25 MHz is selected. When low, the double frequency of 12.5 MHz is selected.															
SHTMON	33	O	Shutter monitor															
S/H	34	O	Sample and hold															
SEL1, SEL2, SEL3	25, 27, 28	I	Shutter-speed select. SEL1, SEL2, and SEL3 selects the fixed shutter times in horizontal TV lines. This selection sets the exposure times if either the manual-shutter or random-shutter modes are selected (see Table 2).															
TEST1, TEST2, TEST3, TEST4	1, 2, 3, 19		TEST1, TEST2, TEST3, and TEST4 are test points and are not used in normal operation.															
VACT	32	O	Video active															
VCC	13, 26, 45, 59		Supply voltage															
VD	47	O	Vertical drive															
VR	29	I	Vertical reset															
WINDOW	16	O	Window. WINDOW is high as defined by WSEL1 and WSEL2 at the times in TV lines and horizontal pixels (see Table 3).															
WSEL1, WSEL2	14, 15	I	Window select. WSEL1 and WSEL2 selects the output mode of WINDOW. These inputs are normally used with the auto-iris mode in selecting the desired region to optimize the exposure of the best image (see Table 3). <table><thead><tr><th>WSEL1</th><th>WSEL2</th><th>OPERATION</th></tr></thead><tbody><tr><td>H</td><td>H</td><td>MODE1</td></tr><tr><td>L</td><td>H</td><td>MODE2</td></tr><tr><td>H</td><td>L</td><td>MODE3</td></tr><tr><td>L</td><td>L</td><td>MODE4</td></tr></tbody></table>	WSEL1	WSEL2	OPERATION	H	H	MODE1	L	H	MODE2	H	L	MODE3	L	L	MODE4
WSEL1	WSEL2	OPERATION																
H	H	MODE1																
L	H	MODE2																
H	L	MODE3																
L	L	MODE4																
XSEL	39	I	Crystal-oscillator select. XSEL selects the inputs used as the master clock. When XSEL is high, a 25-MHz crystal is connected between XIN and XOUT. When XSEL is low, a 25-MHz crystal oscillator is required and its output connected to CLKIN.															
XIN	41		Crystal in															
XOUT	40		Crystal out															

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC}	–0.5 V to 6 V
Input voltage range, V_{I}	–0.5 V to $\text{V}_{\text{CC}} + 0.5 \text{ V}$
Output voltage range, V_{O}	–0.5 V to $\text{V}_{\text{CC}} + 0.5 \text{ V}$
Operating free-air temperature range, T_{A}	–20°C to 45°C
Storage temperature range, T_{STG}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C



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recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	TTL	2		V_{CC}	V
		CMOS	$0.7V_{CC}$		V_{CC}	
V_{IL}	Low-level input voltage	TTL	GND		0.8	V
		CMOS	GND		$0.2V_{CC}$	
t_r, t_f	Input rise and fall times	TTL	0		25	ns
		CMOS	0		25	
T_A	Operating free-air temperature		–20		45	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = Rated current	$V_{CC}-0.8$		V
V_{OL}	Low-level output voltage	I_{OL} = Rated current		0.5	V
V_{T+}	Schmitt-trigger input hysteresis, TTL	$V_{CC} = 5\text{ V}$	0.3		V
V_{T-}	Schmitt-trigger input hysteresis, CMOS		$0.2V_{CC}$		
I_{IH}	High-level input current	$V_I = V_{CC}$		1	μA
I_{IL}	Low-level input current	$V_I = \text{GND}$		–1	μA
I_O	Output current	$V_O = V_{CC}$ or GND		± 10	μA
I_{CCQ}	Quiescent current	$V_I = V_{CC}$		60	μA

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Table 1. Electronic-Function Select

EFSEL1	EFSEL2	EFSEL3	MODE
L	L	L	261H [†]
H	L	L	Auto-iris [‡]
L	H	L	Random shutter
H	H	L	Flickerless [§]
L	L	H	Manual shutter
H	L	H	STD
L	H	H	STD
H	H	H	STD

[†] For the 261H mode, see Figure 4.


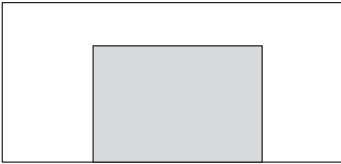
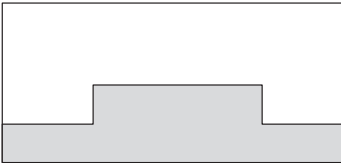

[‡] The maximum range of the auto-iris integration times is 1/50000 second to 1/60 second.

[§] The flickerless mode has a fixed shutter of 1/100 second. It has an effect only when 50-Hz power systems are in use.

Table 2. Shutter-Speed Select

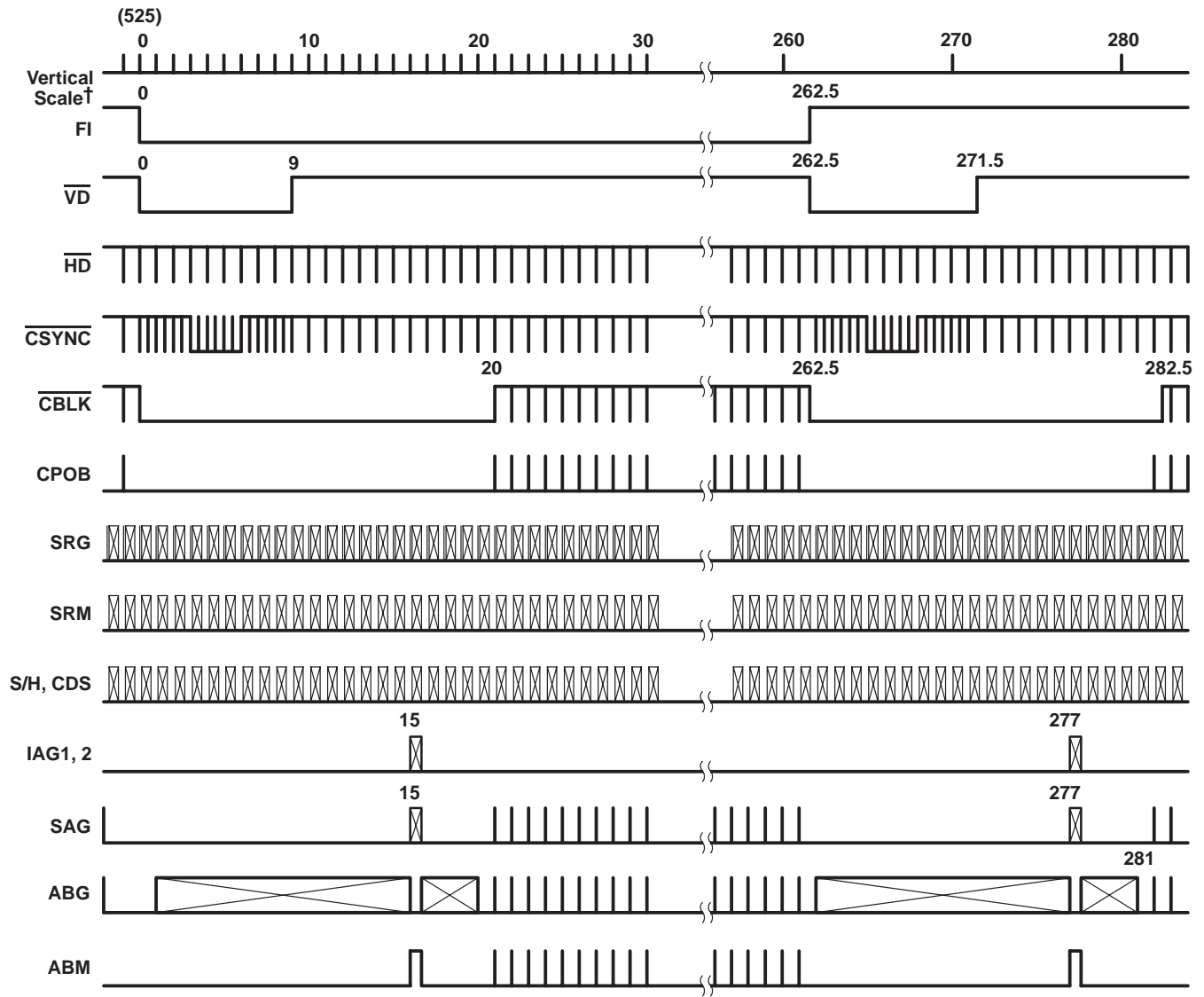
SEL1	SEL2	SEL3	FIXED SHUTTER TIMES
L	L	L	1H
H	L	L	2H
L	H	L	4H
H	H	L	8H
L	L	H	16H
H	L	H	32H
L	H	H	64H
H	H	H	128H

Table 3. WINDOW Modes

MODE	PIXEL			
	130–294	295–624	625–789	
MODE1				
Lines 22–81, 285–344	H	H	H	
Lines 82–141, 345–404	H	H	H	
Lines 142–201, 405–464	H	H	H	
Lines 202–261, 465–525	H	H	H	
MODE2				
Lines 22–81, 285–344	L	L	L	
Lines 82–141, 345–404	L	H	L	
Lines 142–201, 405–464	L	H	L	
Lines 202–261 465–525	L	H	L	
MODE3				
Lines 22–81, 285–344	L	L	L	
Lines 82–141, 345–404	L	L	L	
Lines 142–201, 405–464	L	H	L	
Lines 202–261 465–525	H	H	H	
MODE4				
Lines 22–81, 285–344	L	L	L	
Lines 82–141, 345–404	L	L	L	
Lines 142–201, 405–464	L	L	L	
Lines 202–261, 465–525	H	H	H	

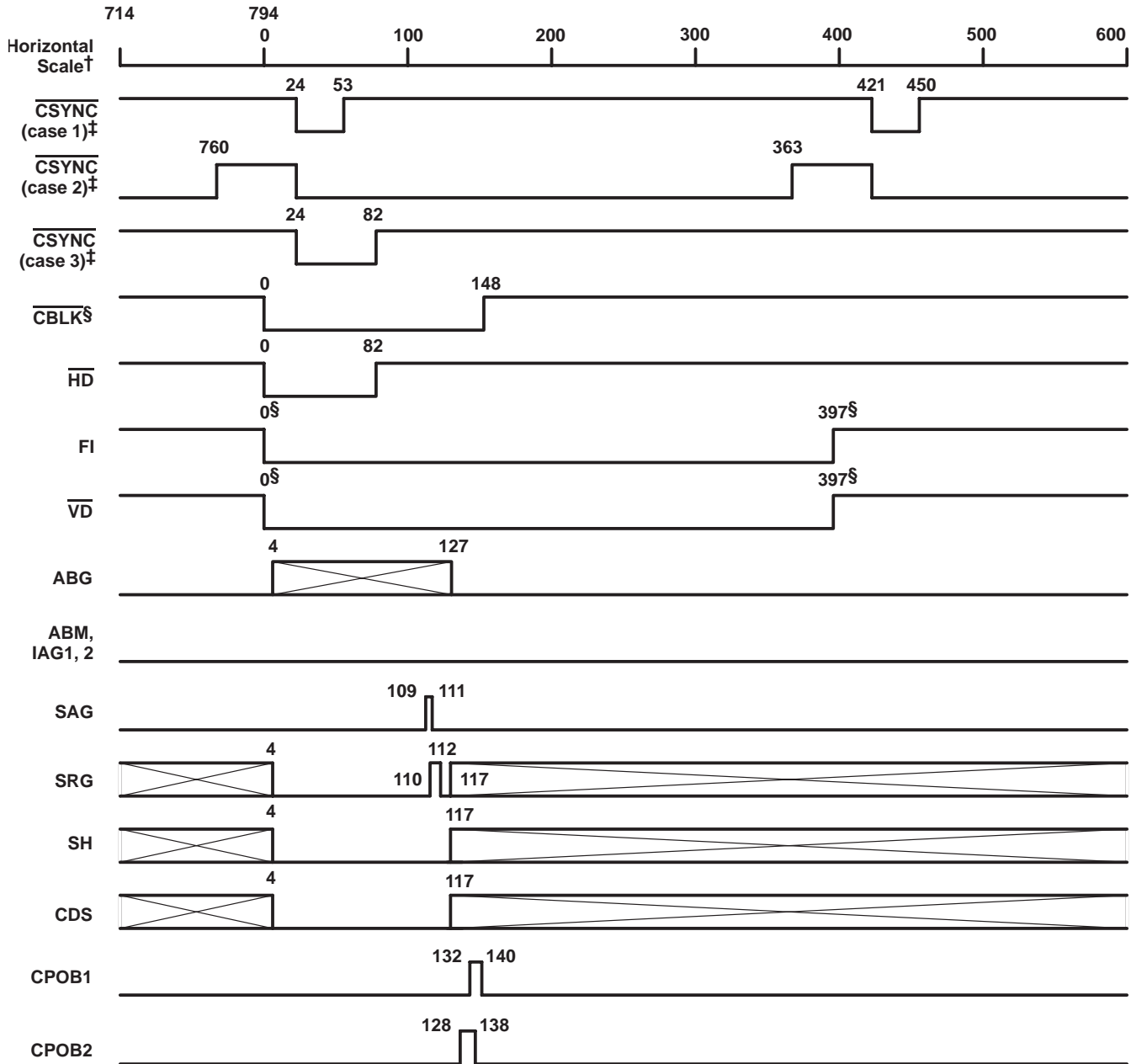
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† One TV frame = 33.3 ms = 525 intervals

Figure 1. Vertical Timing



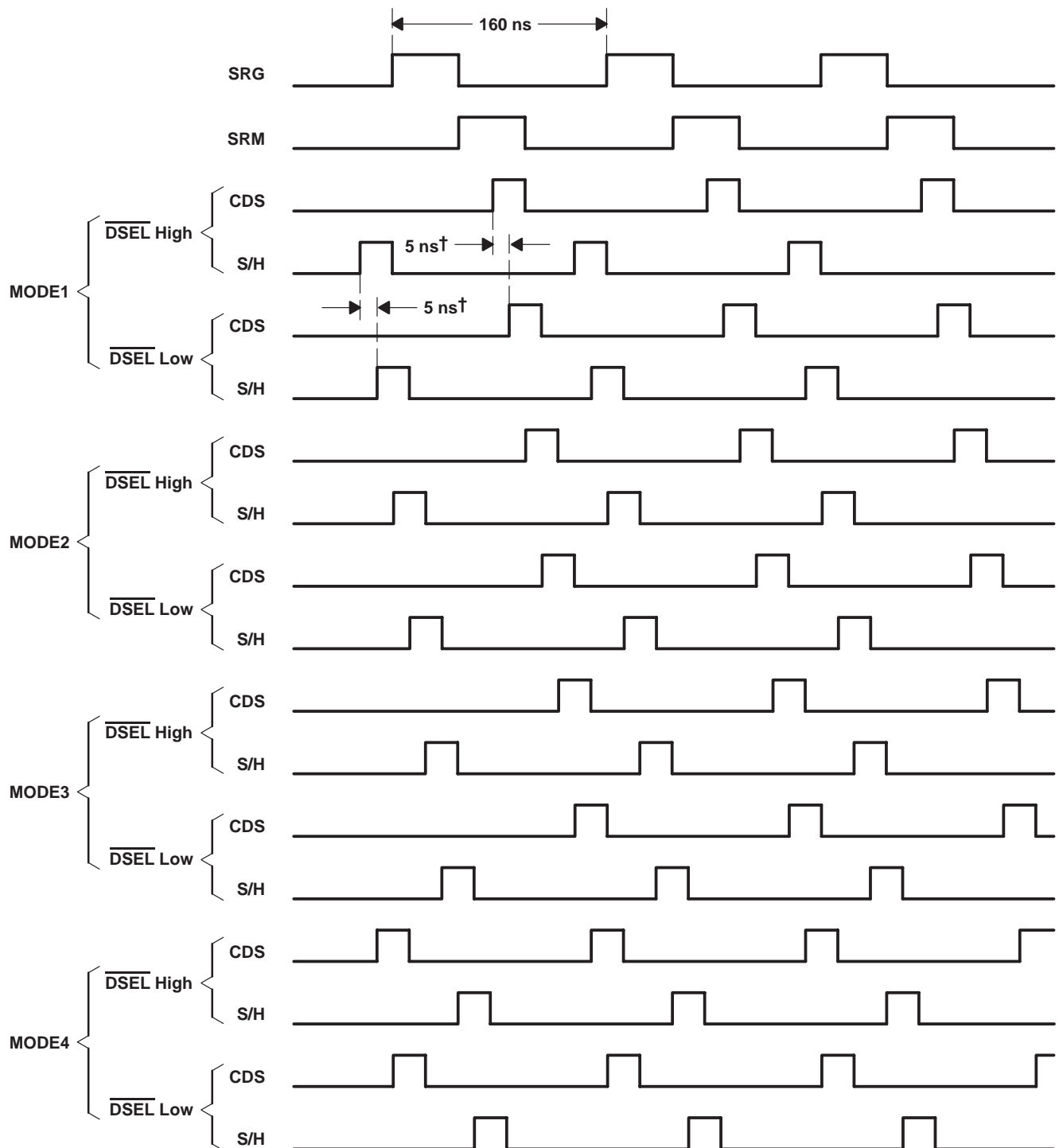
† One horizontal-scan line = $63.52 \mu\text{s}$ = 794 intervals

‡ CSYNC varies depending on which horizontal-scan line of a 262.5-line TV field is being examined.

- Case 1 depicts the equalization pulses that occur during horizontal-scan lines 1, 2, 3, 7, 8, and 9.
- Case 2 depicts the vertical serration pulses that occur during horizontal-scan lines 4, 5, and 6.
- Case 3 applies to all remaining horizontal-scan lines.

§ CBLK makes 1/2 line transitions only on lines 262.5 and 268.5. FI makes a high-to-low transition only on line 525 and a low-to-high transition only on line 262.5. VD makes high to low transitions only on lines 525 and 262.5. It makes low-to-high transitions only on lines 9 and 271.5.

Figure 2. Horizontal Timing



† In all four modes, the selection of $\overline{\text{DSEL}}$ low results in an additional 5-ns delay of CDS and S/H with respect to SRG.

Figure 3. Phase-Select-Mode Timing

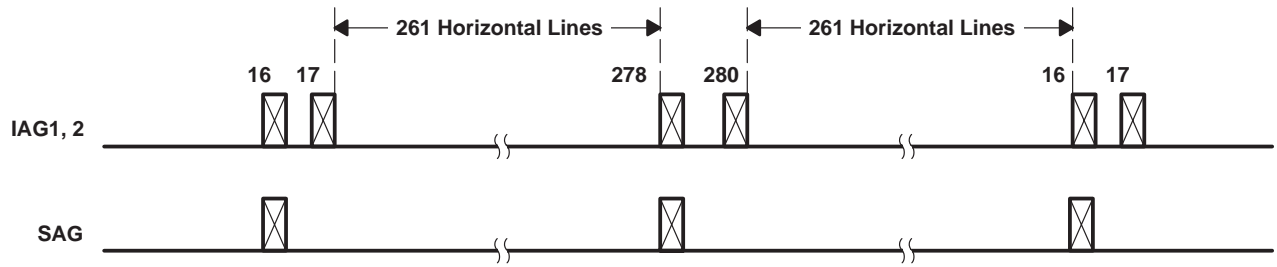


Figure 4. 261H Mode

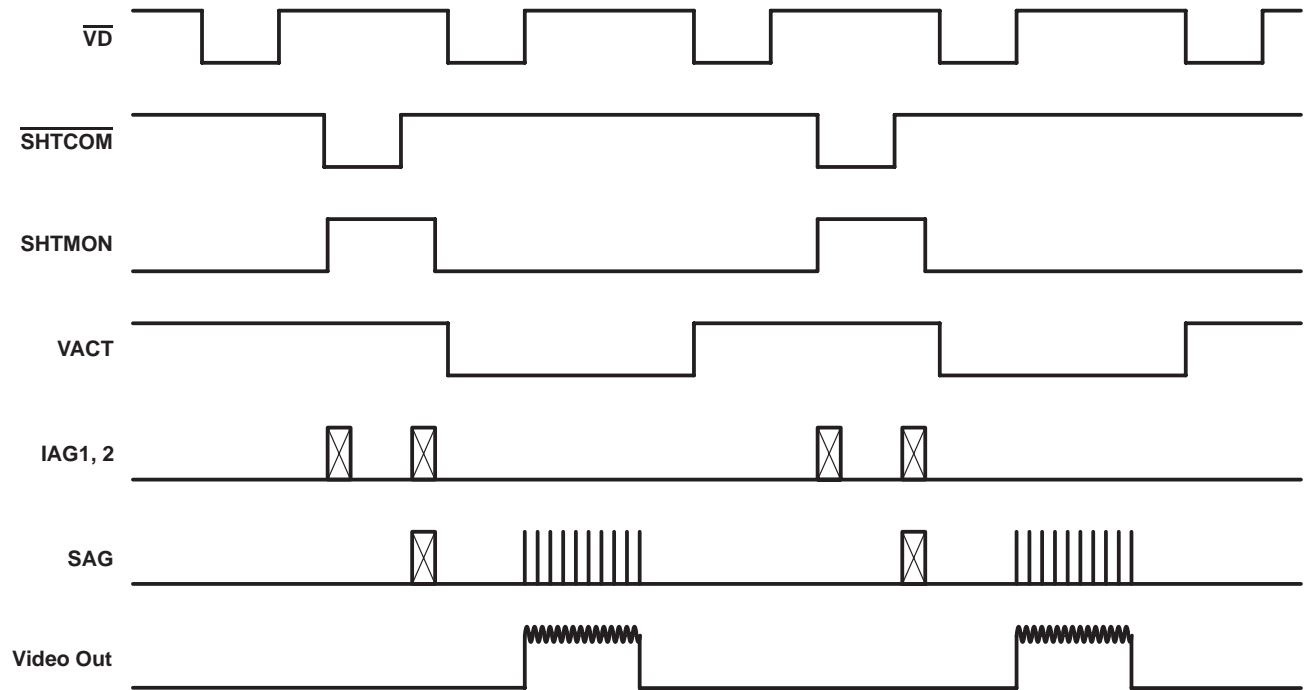
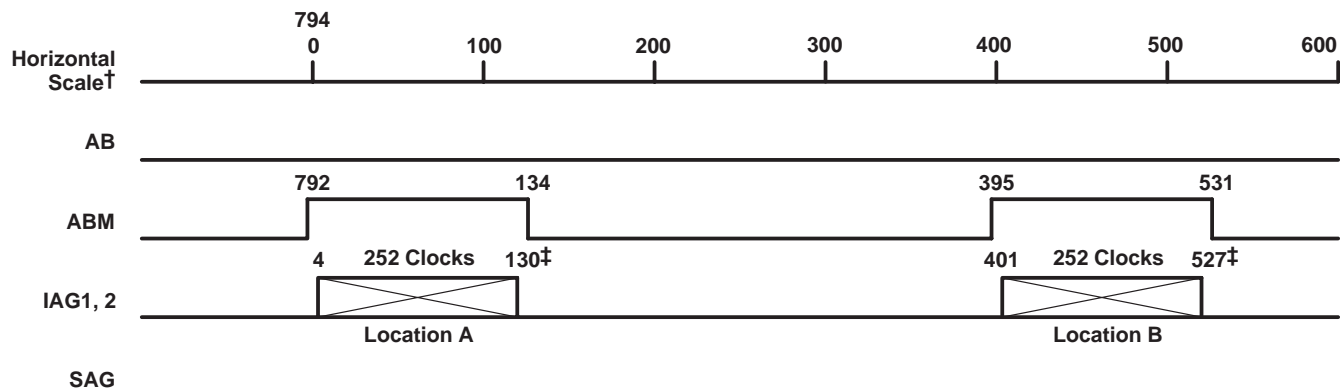


Figure 5. Random-Shutter-Mode Timing

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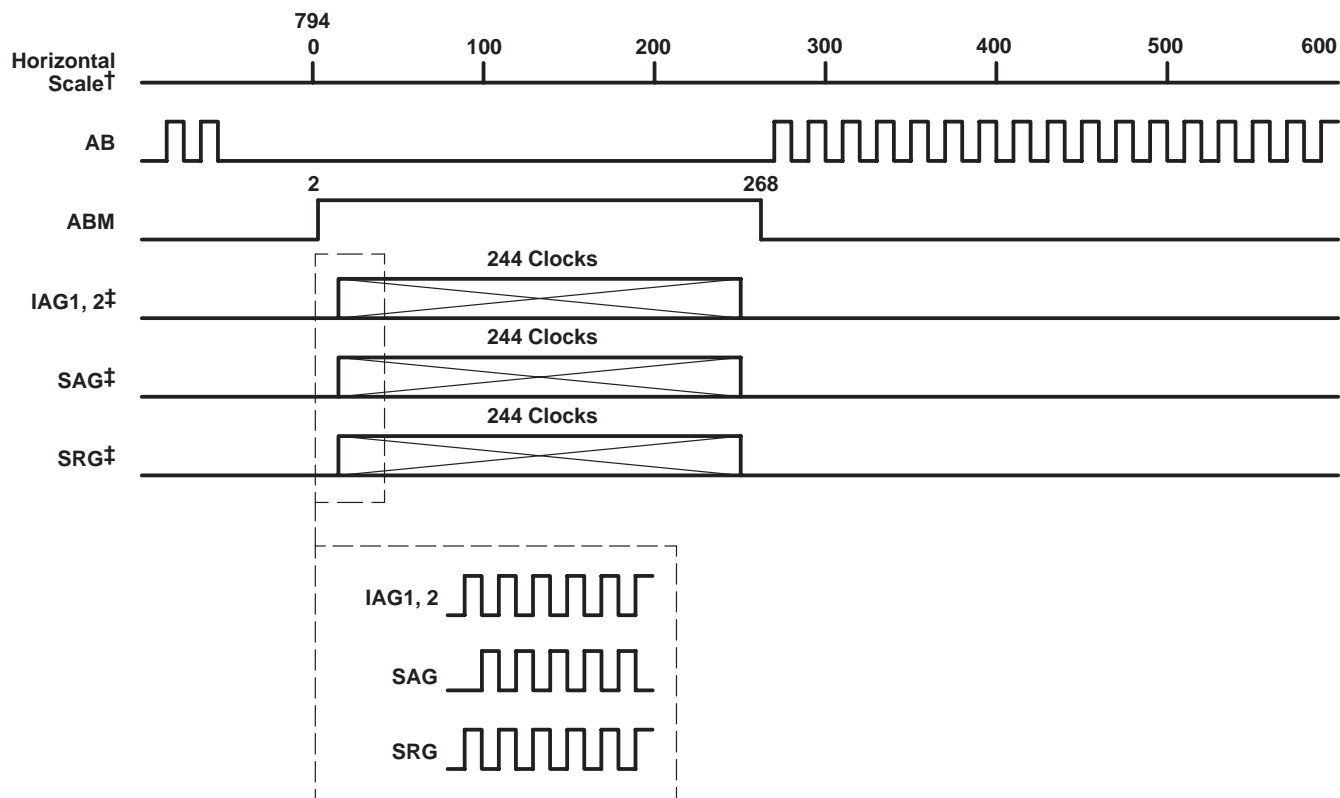
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† One horizontal-scan line = $63.52 \mu s = 794$ intervals

‡ The clear sequence must take place at Location A if the iris controller determines that it is to be executed on any of the lines 21–262 of TV field 1 or lines 284–525 of TV field 2. The clear sequence can take place at either Location A or Location B if the iris controller determines that it is to be executed on any of the lines 1–20 (excluding line 16) of TV field 1 or lines 263–283 (excluding line 278) of TV field 2. The frequency of the clear sequence is 25 MHz.

Figure 6. Clear Timing



† One horizontal-scan line = $63.52 \mu s = 794$ intervals

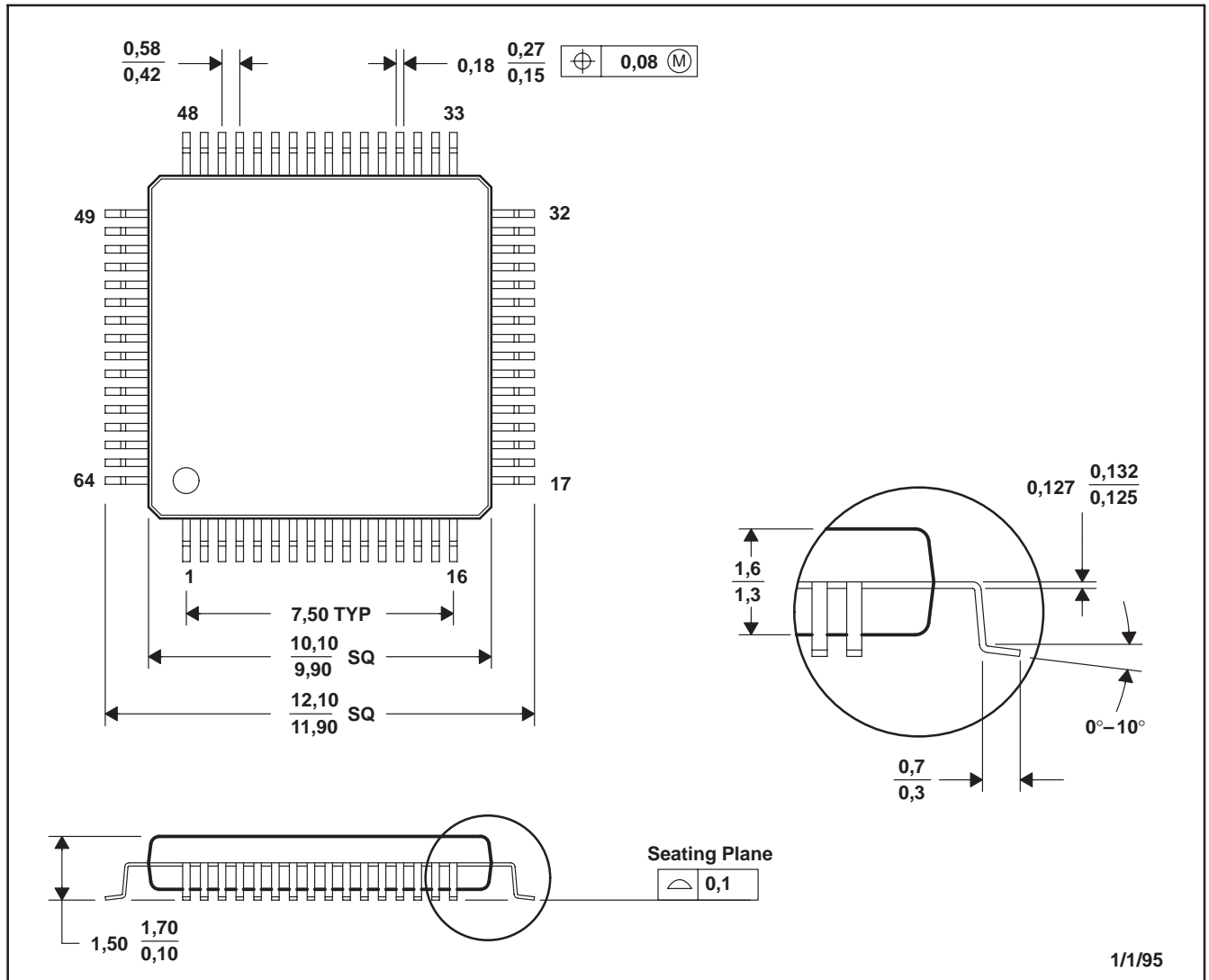
‡ The frequency of the parallel transfer is 12.5 MHz.

Figure 7. Parallel-Transfer Timing

MECHANICAL DATA

LQFP

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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