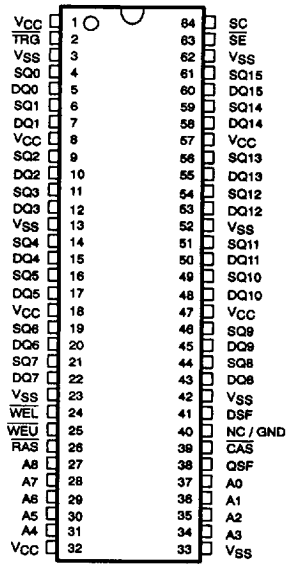
TMS55165
262 144 BY 16-BIT MULTIPORT VIDEO RAM

SMVS165B–AUGUST 1992–REVISED JANUARY 1993

- **DRAM : 262 144 Words × 16 Bits SAM: 256 Words × 16 Bits**
- **Dual Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Data Transfer Function From the DRAM to the Serial Data Register**
- **(4 × 4) × 4 Block Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From the 16-Bit On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O. Two Write-Per-Bit Modes to Simplify System Design**
- **Byte Write Control ($\overline{WEL}$, $\overline{WEU}$) Provides Flexibility**
- **Enhanced Page Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ and Hidden Refresh Modes**
- **Long Refresh Period: Every 8 ms (Max)**
- **DRAM Port Is Compatible With the TMS45165**
- **Up to 45-MHz Uninterrupted Serial Data Streams**
- **256 Selectable Serial Register Starting Locations**
- **$\overline{SE}$ Controlled Register Status QSF**
- **Split Serial-Data Register for Simplified Realtime Register Reload**
- **3-State Serial Outputs Allow Easy Multiplexing of Video Data Streams**
- **All Inputs/Outputs and Clocks TTL Compatible**
- **Compatible With JEDEC Standards**
- **Texas Instruments EPIC™ CMOS Process**
- **Designed to Work With the Industry-Leading Texas Instruments Graphics Family**
- **Performance Ranges:**

DGH PACKAGE†
(TOP VIEW)



† Package is shown for pinout rererence only.

PIN NOMENCLATURE

A0–A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ15	DRAM Data I/O, Write Mask Data
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row-Address Strobe
SC	Serial Clock
SQ0–SQ15	Serial Data Output
$\overline{TRG}$	Output Enable, Transfer Select
$\overline{WEL}$, $\overline{WEU}$	DRAM Byte Write Enable Selects
DSF	Special Function Select
QSF	Special Function Output
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
NC/GND	No Connect/Ground (Important: Not Connected Internally to V_{SS})

	ACCESS TIME ROW ENABLE $t_{a(R)}$ (MAX)	ACCESS TIME SERIAL DATA $t_{a(SQ)}$ (MAX)	DRAM CYCLE TIME $t_{c(rd\ W)}$ (MIN)	DRAM PAGE MODE $t_{c(P)}$ (MIN)	SERIAL CYCLE TIME $t_{c(SC)}$ (MIN)	OPERATING CURRENT SERIAL PORT STANDBY I_{CC1} (MAX)	OPERATING CURRENT SERIAL PORT ACTIVE I_{CC1A} (MAX)
TMS55165-70	70 ns	20 ns	130 ns	45 ns	22 ns	165 mA	205 mA
TMS55165-80	80 ns	25 ns	150 ns	50 ns	30 ns	160 mA	195 mA

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description

The TMS55165 Multiport Video RAM is a high-speed dual ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 16 bits each, interfaced to a serial data register [Serial Access Memory (SAM)], organized as 256 words of 16 bits each. The TMS55165 supports three basic types of operation: random access to and from the DRAM, serial access from the serial register, and transfer of data from any row in the DRAM to the serial register. Except during transfer operations, the TMS55165 can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

The TMS55165 is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's (4 × 4) × 4 block write feature. The block write mode allows sixteen bits of data (present in an on-chip color data register) to be written to any combination of four adjacent column address locations. As many as 64 bits of data can be written to memory during each $\overline{CAS}$ cycle time. Also on the DRAM port, a write mask or a write-per-bit allows masking any combination of the 16 inputs/outputs on any write cycle. The persistent write-per-bit feature uses a mask register which, once loaded, can be used on subsequent write cycles without reloading. The TMS55165 also offers byte write capability. Byte write control can be applied in write cycles, block write cycles, load mask register cycles, and load color register cycles.

The TMS55165 offers a split-register transfer read (DRAM to SAM) feature for the serial register (SAM port). This feature enables real-time register reload implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. This real-time register reload implementation allows truly continuous serial data. For applications not requiring real-time register reload (for example, reloads done during CRT retrace periods), the single-register mode of operation is retained to simplify system design.

The SAM port is designed for maximum performance. Data can be accessed from the SAM at serial rates up to 45 MHz. During the split register transfer reads, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, designated QSF, is included to indicate which half of the serial register is active at any given time in split register mode.

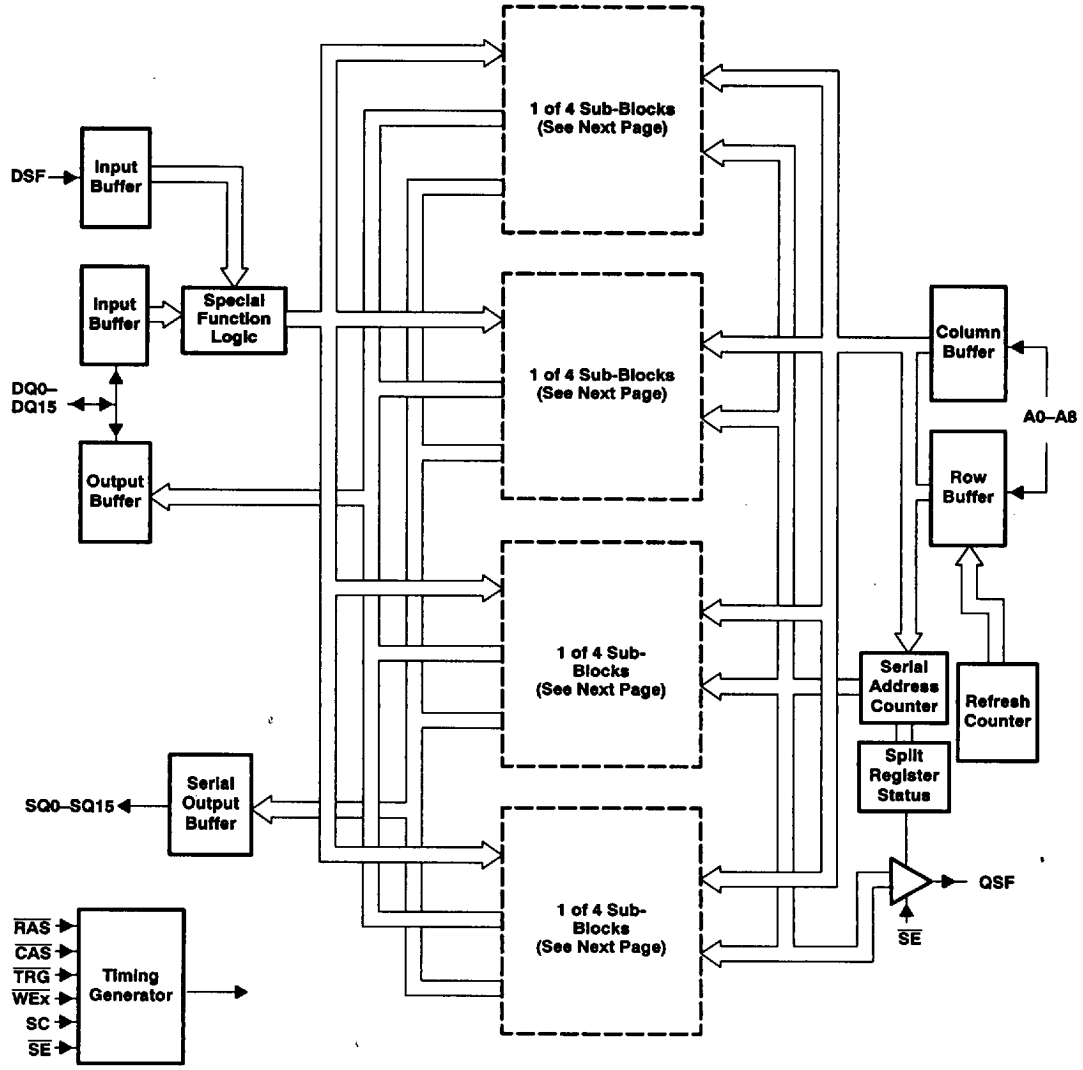
All inputs, outputs, and clock signals on the TMS55165 are compatible with Series 74 TTL. All address lines and data-in are latched on chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The TMS55165 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The TMS55165 is offered in a 64-pin super-small-outline gull-wing leaded package for direct surface mounting.

The TMS55165 and other TI multiport video RAMs are supported by a broad line of graphics processors and control devices from Texas Instruments.

functional block diagram



functional block diagram (continued)

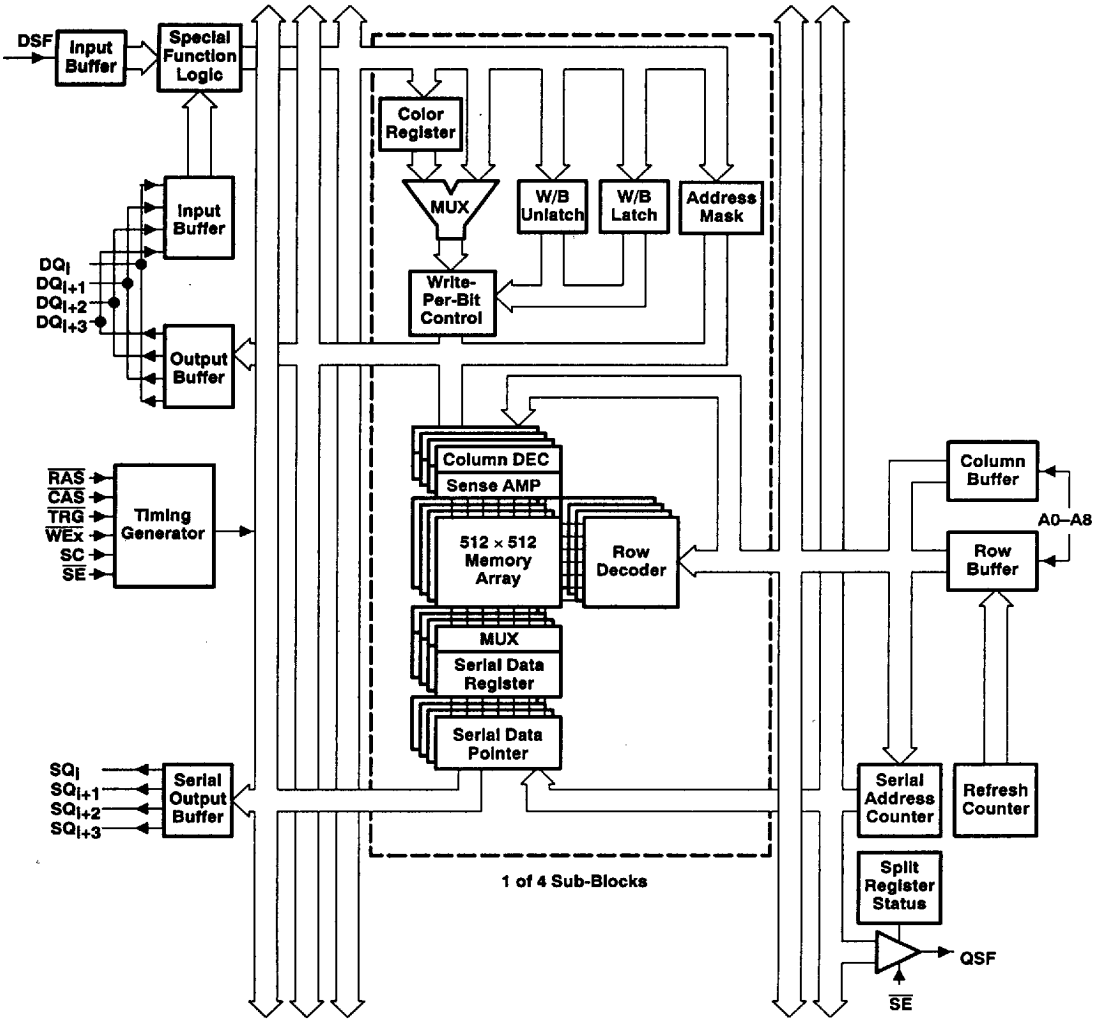


Table 1. Function Table

FUNCTION	RAS FALL				CAS FALL	ADDRESS		DQ0–DQ15‡		MNE CODE
	CAS	TRG	WEx†	DSF	DSF	RAS	CAS	RAS	CAS WEL WEU	
Reserved (do not use)	0	0	0	0	X	X	X	X	X	—
CAS-before-RAS refresh (option reset)§	0	X	1	0	X	X	X	X	X	CBR
CAS-before-RAS refresh (no reset)¶	0	X	1	1	X	X	X	X	X	CBRN
Read transfer	1	0	1	0	X	Row Addr	Tap Point	X	X	RT
Split-register read transfer	1	0	1	1	X	Row Addr	Tap Point	X	X	SRT
DRAM write (non-persistent write-per-bit)	1	1	0	0	0	Row Addr	Col Add	Write Mask	Valid Data	RWM
DRAM block write (non-persistent write-per-bit)	1	1	0	0	1	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM write (persistent write-per-bit)	1	1	0	0	0	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	1	1	0	0	1	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
DRAM write (non-masked)	1	1	1	0	0	Row Addr	Col Addr	X	Valid Data	RW
DRAM block write (non-masked)	1	1	1	0	1	Row Addr	Block Addr A2–A8	X	Col Mask	BW
Load write mask register #	1	1	1	1	0	Refresh Addr	X	X	Write Mask	LMR
Load color register	1	1	1	1	1	Refresh Addr	X	X	Color Data	LCR

† Logic 0 is selected when either or both WEL and WEU are low.
‡ DQ0–DQ15 are latched on either the first WEx falling edge or the falling edge of CAS, whichever occurs later.
§ CAS-before-RAS refresh (option reset) mode will end persistent write-per-bit mode. Hidden refresh will also end the persistent write-per-bit mode regardless of the state of DSF at RAS.
¶ CAS-before-RAS refresh (no reset) mode will not end persistent write-per-bit mode.
# Load Write Mask Register cycle will set the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CAS-before-RAS (option reset) cycle.
X: = Don't care.
Column Mask: 1 = Write to address/column location enabled.
Write Mask: 1 = Write to I/O enabled.

Table 2. Pin Description vs Operational Mode

PIN	DRAM	TRANSFER	SAM
A0–A8	Row, column address	Row-address, Tap point	
$\overline{CAS}$	Column-address strobe, DQ output enable	Tap address strobe	
DQ	DRAM data I/O, Write mask		
DSF	Block write enable, Write mask register load enable, Color register load enable $\overline{CAS}$-before-$\overline{RAS}$ (option reset)	Split register transfer enable	
$\overline{RAS}$	Row-address strobe	Row-address strobe	
$\overline{SE}$			SQ output enable, QSF output enable
SC			Serial clock
SQ			Serial data output
$\overline{TRG}$	DQ output enable	Transfer enable	
$\overline{WEL}$ / $\overline{WEU}$	Byte write enable, Write-per-bit enable		
QSF			Serial register status
NC/GND	Make no external connection or tie to system GND		
V_{CC}†	5-V Supply		
V_{SS}†	Ground		

† For proper device operation, all V_{CC} pins must be connected to a 5-V supply, and all V_{SS} pins must be tied to ground.

pin definitions

address (A0–A8)

Eighteen address bits are required to decode one of 262 144 storage locations. Nine row address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Nine column address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$.

During the read transfer operation, the states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of the 512 rows where the transfer will occur. At the falling edge of $\overline{CAS}$, the column address bits A0–A8 are latched. The most significant column address bit (A8) selects which half of the row will be transferred to the SAM. The appropriate 8-bit column address (A0–A7) selects one of 256 tap points (starting positions) for the serial data output.

During split register read transfer operation, address bit A7 is ignored at the falling edge of $\overline{CAS}$. An internal counter will select which half of the register will be used. If the high half of the SAM is currently in use, the low half of the SAM will be loaded with the low half of the DRAM half row, and vice versa. The remaining seven address bits (A0–A6) are used to select 1 of 127 possible starting locations within the SAM. Locations 127 and 255 are not valid tap points.

row-address strobe ($\overline{RAS}$)

$\overline{RAS}$ is similar to a chip enable, so that all DRAM cycles and transfer cycles are initiated by the falling edge of $\overline{RAS}$. $\overline{RAS}$ is a control input that latches the states of the row address, $\overline{WEL}$, $\overline{WEU}$, $\overline{TRG}$, $\overline{CAS}$, and DSF onto the chip to invoke DRAM and read transfer functions of the TMS55165.

column-address strobe ($\overline{CAS}$)

$\overline{CAS}$ is a control input that latches the states of the column address and DSF to control DRAM and read transfer functions of the TMS55165. When $\overline{CAS}$ is brought low during a transfer cycle, the address bits A0–A8 will be latched at the start position (tap) for the serial data output. $\overline{CAS}$ also acts as an output enable for the DRAM output pins, DQ0–DQ15.

output enable/transfer select ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either DRAM or transfer operation as $\overline{RAS}$ falls. For DRAM operation, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. During DRAM operation, $\overline{TRG}$ functions as an output enable for the DRAM output pins, DQ0–DQ15.

For transfer operation, $\overline{TRG}$ must be brought low before $\overline{RAS}$ falls.

write mask select, write enable ($\overline{WEU}$, $\overline{WEL}$)

In DRAM operation, $\overline{WEL}$ enables data to be written to the lower byte (DQ0–DQ7), and $\overline{WEU}$ enables data to be written to the upper byte (DQ8–DQ15). Both $\overline{WEL}$ and $\overline{WEU}$ have to be held high together to select the read mode. Bringing either or both $\overline{WEL}$ and $\overline{WEU}$ low will select the write mode.

$\overline{WEL}$ and $\overline{WEU}$ are also used to select the DRAM write-per-bit mode of operation. If either or both $\overline{WEL}$ and $\overline{WEU}$ are brought low as $\overline{RAS}$ falls during a DRAM write cycle, the write-per-bit operation is invoked. The TMS55165 supports both the non-persistent write-per-bit mode and the persistent write-per-bit mode.

special function select (DSF)

The DSF input is latched on the falling edge of $\overline{RAS}$ and $\overline{CAS}$, similarly to an address. DSF determines which of the following functions below are invoked on a particular cycle:

- CBR refresh with reset (CBR)
- CBR refresh with no reset (CBRN)
- Block write
- Loading mask register for the persistent write-per-bit mode
- Loading color register for the block write mode
- Split-register read transfer

DRAM data I/O, write mask data (DQ0–DQ15)

DRAM data is written or read through the common I/O DQ pins. The three-state DQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance (floating) state as long as either $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. Either $\overline{CAS}$ or $\overline{TRG}$ going high returns the outputs to a high-impedance state. In a read transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

The write-per-bit mask is latched into the device via the random DQ pins by the falling edge of $\overline{RAS}$.

serial data output (SQ0–SQ15)

Serial data is read from the SQ pins. The SQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. Data-out is the same polarity as data-in. The serial outputs are in the high-impedance (floating) state as long as serial enable pin, $\overline{SE}$, is high. The serial outputs are enabled when $\overline{SE}$ is brought low.

serial clock (SC)

Serial data is accessed out of the data register from the rising edge of SC. The TMS55165 is designed to work with a wide range of clock duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC clock operating frequency.

serial enable ($\overline{SE}$)

During serial access operations, $\overline{SE}$ is used as an enable/disable for the SQ outputs. $\overline{SE}$ low will enable the serial data output. $\overline{SE}$ high will disable the serial data output. $\overline{SE}$ is also used as an enable/disable for output pin QSF.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is not disabled. Thus, external SC pulses will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

special function output (QSF)

QSF is an output pin that indicates which half of the SAM is being accessed. When QSF is low, the serial address pointer is accessing the lower (least significant) 128 bits of the serial register (SAM). When QSF is high, then the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon crossing a boundary between the two SAM halves.

During the read transfer operation (non-split register), QSF may change state upon completing the cycle. This state is determined by the tap point being loaded during the transfer cycle. During the split-register read transfer operation, QSF may change state upon crossing a boundary between the two SAM halves.

QSF output is enabled by $\overline{SE}$. If $\overline{SE}$ is high, then QSF output will be in the high-impedance state.

no connect/ground (NC/GND)

The NC/GND pin should be tied to system ground or left floating for proper device operation.

functional operation description

random access operation

Table 3. DRAM Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CAS}$ FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	$\overline{CAS}$	$\overline{TRG}$	$\overline{WEx}$‡	DSF	DSF	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$ $\overline{WEL}$ $\overline{WEU}$	
Reserved (do not use)	0	0	0	0	X	X	X	X	X	—
$\overline{CAS}$-before-$\overline{RAS}$ refresh (option reset)§	0	X	1	0	X	X	X	X	X	CBR
$\overline{CAS}$-before-$\overline{RAS}$ refresh (no reset)¶	0	X	1	1	X	X	X	X	X	CBRN
DRAM write (non-persistent write-per-bit)	1	1	0	0	0	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM block write (non-persistent write-per-bit)	1	1	0	0	1	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM write (persistent write-per-bit)	1	1	0	0	0	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	1	1	0	0	1	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
DRAM write (non-masked)	1	1	1	0	0	Row Addr	Col Addr	X	Valid Data	RW
DRAM block write (non-masked)	1	1	1	0	1	Row Addr	Block Addr A2–A8	X	Col Mask	BW
Load write mask register#	1	1	1	1	0	Refresh Address	X	X	Write Mask	LMR
Load color register	1	1	1	1	1	Refresh Address	X	X	Color Data	LCR

† DQ0–DQ15 are latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later.
‡ Logic 0 is selected when either or both $\overline{WEL}$ and $\overline{WEU}$ are low.
§ $\overline{CAS}$-before-$\overline{RAS}$ refresh (option reset) mode will end persistent write-per-bit mode. Hidden refresh will also end the persistent write-per-bit mode regardless of the state of DSF at $\overline{RAS}$.
¶ $\overline{CAS}$-before-$\overline{RAS}$ refresh (no reset) mode will not end persistent write-per-bit mode.
# Load Write Mask Register cycle will set the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the $\overline{CAS}$-before-$\overline{RAS}$ (option reset) cycle.
X: = Don't care.
Column Mask: 1 = Write to address/column location enabled.
Write Mask: 1 = Write to I/O enabled.

refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refreshes are accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored and the refresh address is generated internally. Two types of CBR refresh cycles are available. The CBR refresh (option reset) will end the persistent write-per-bit mode. The CBRN refresh (no reset) will not end the persistent write-per-bit mode. The 512 rows of the DRAM do not necessarily need to be refreshed consecutively, as long as the entire refresh is completed within the required time period $t_{rf(MA)}$. Other cycles may be performed in between $\overline{CAS}$-before-$\overline{RAS}$ cycles without disturbing the internal address generation. The output buffers remain in the high-impedance state during the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, regardless of the state of $\overline{TRG}$.

hidden refresh

A hidden refresh is accomplished by holding $\overline{CAS}$ low in the DRAM read cycle and cycling $\overline{RAS}$. The output data of the DRAM read cycle remains valid while the refresh is being carried out. Like the $\overline{CAS}$-before-$\overline{RAS}$ refresh, the refreshed row addresses are generated internally during the hidden refresh. Hidden refresh will also end the peristent write-per-bit mode, regardless of the state of $\overline{TRG}$.

$\overline{RAS}$ only refresh

A $\overline{RAS}$-only refresh is accomplished by cycling $\overline{RAS}$ at every row address. Unless $\overline{CAS}$ and $\overline{TRG}$ are low, the output buffers remain in the high-impedance state to conserve power. Externally generated addresses must be supplied during $\overline{RAS}$-only refresh. Strobing each of 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed.

enhanced page mode

Enhanced page mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row address setup, row address hold, and address multiplex. The maximum $\overline{RAS}$ low time and $\overline{CAS}$ page cycle time used determines the number of columns that may be accessed.

Unlike conventional page mode operations, the enhanced page mode allows the TMS55165 to operate at a higher data bandwidth. Data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied.

byte write operation

Byte write operations can be applied in DRAM write cycles, block write cycles, load mask register cycles, and load color register cycles.

Holding either or both $\overline{WEL}$ and $\overline{WEU}$ low will select the write mode. In normal write cycles, $\overline{WEL}$ enables data to be written to the lower byte (DQ0–DQ7), and $\overline{WEU}$ enables data to be written to the upper byte (DQ8–DQ15). For early write cycles, one of $\overline{WEx}$ is brought low before $\overline{CAS}$ falls. The other $\overline{WEx}$ can be brought low before $\overline{CAS}$ falls or after $\overline{CAS}$ falls. The data is strobed in with data setup and hold times for DQ0–DQ15 referenced to $\overline{CAS}$ (see Figure 1).

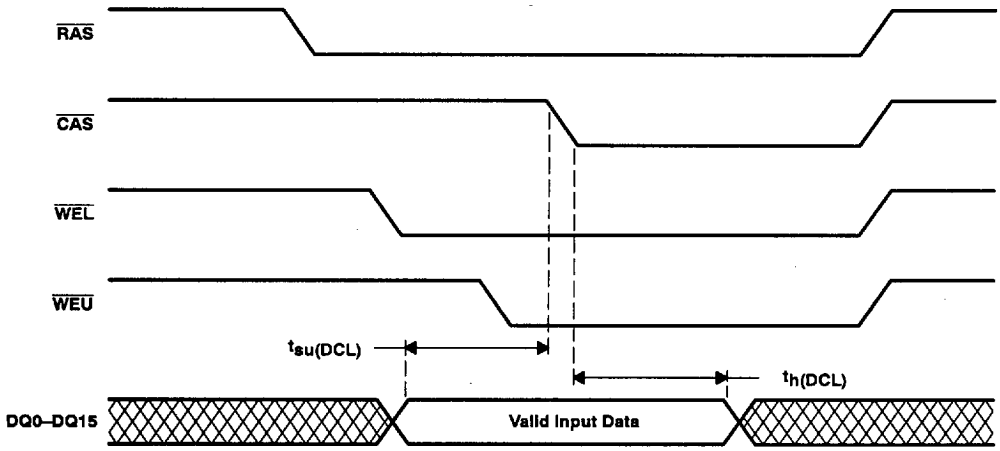


Figure 1. Example of an Early Write

For late write or read-modify-write cycles, $\overline{WEL}$ and $\overline{WEU}$ are both held high before $\overline{CAS}$ falls. After $\overline{CAS}$ falls, either or both $\overline{WEL}$ and $\overline{WEU}$ are brought low to select the corresponding byte or bytes to be written. Data will be strobed in by $\overline{WEL}$ and/or $\overline{WEU}$ with data setup and hold times for DQ0–DQ15 referenced to whichever $\overline{WEx}$ falls earlier (Figure 2).

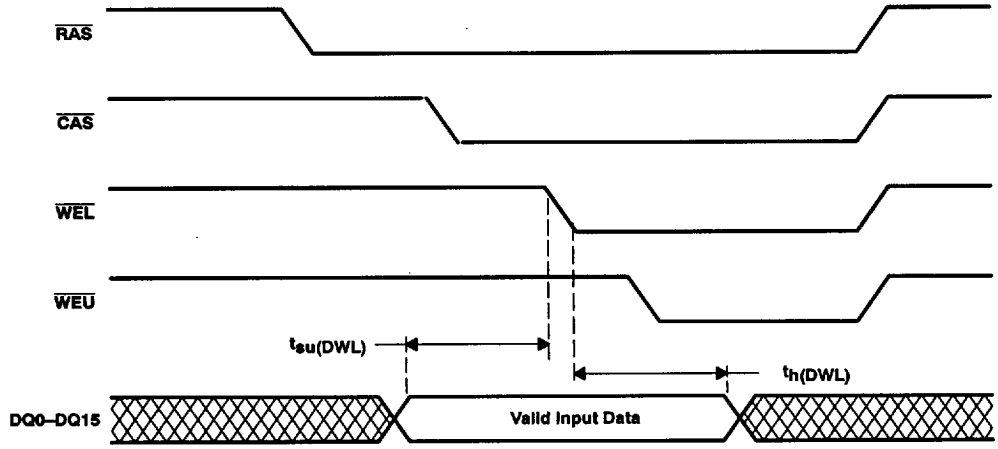


Figure 2. Example of a Late Write

write-per-bit

The write-per-bit feature allows masking any combination of the 16 DQs on any write cycles. The write-per-bit operation is invoked when either or both $\overline{WEL}$ and $\overline{WEU}$ are held low on the falling edge of $\overline{RAS}$. Either individual $\overline{WEx}$ will allow entry of the entire 16-bit mask on DQ0–DQ15. Byte control of the mask input is not allowed.

If both $\overline{WEL}$ and $\overline{WEU}$ are held high on the falling edge of $\overline{RAS}$, the write operation will be performed without any masking. The TMS55165 offers two write-per-bit modes: the non-persistent write-per-bit and the persistent write-per-bit.

non-persistent write-per-bit

When either or both $\overline{WEL}$ and $\overline{WEU}$ are low on the falling edge of $\overline{RAS}$, the write mask is reloaded. A 16-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the sixteen random I/Os are written and which are not. After $\overline{RAS}$ has latched the on-chip write-per-bit mask, input data is driven onto the DQ pins and is latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later. $\overline{WEL}$ enables the lower byte (DQ0–DQ7) to be written, and $\overline{WEU}$ enables the upper byte (DQ8–DQ15) to be written per the mask. If a data low (write mask = 0) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a data high (write mask = 1) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O (Figure 3).

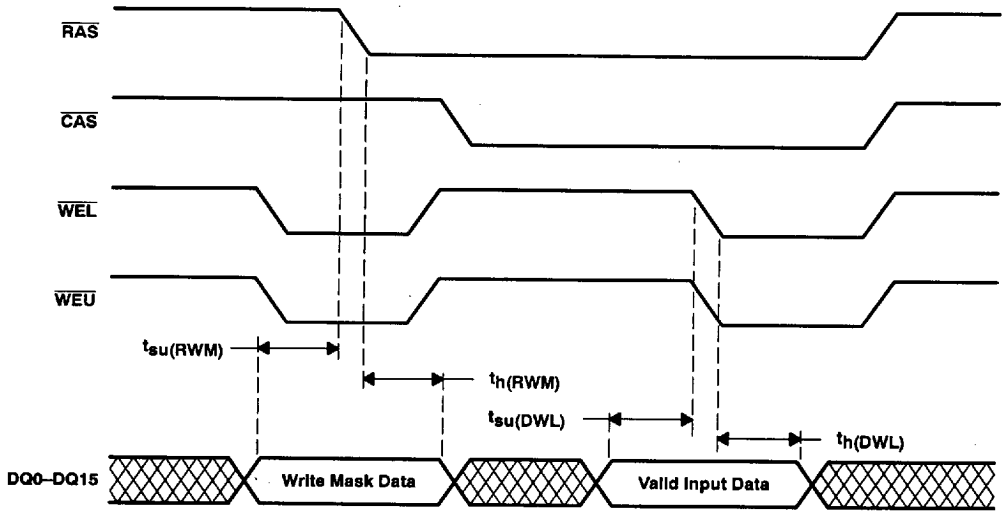


Figure 3. Example of Non-Persistent Write-Per-Bit (Late Write)

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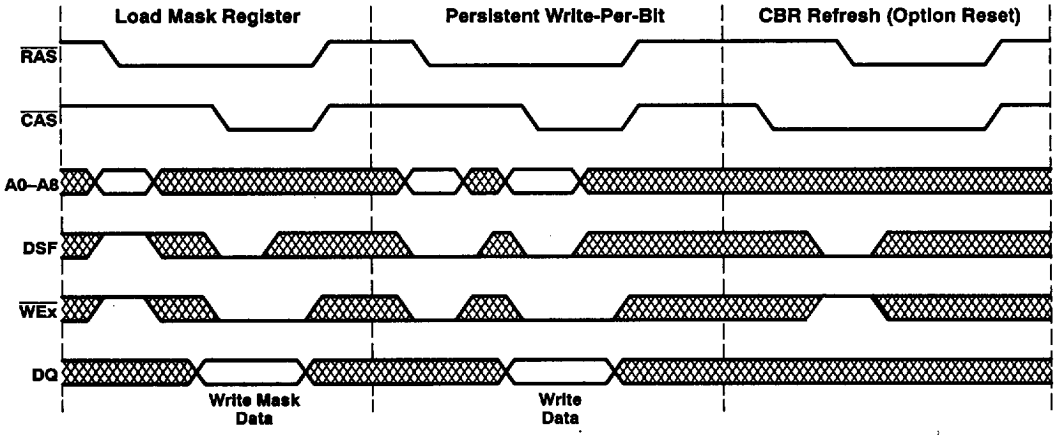
persistent write-per-bit

The persistent write-per-bit mode is initiated only by performing a load mask register cycle first. In the persistent write-per-bit mode, the write-per-bit mask will not be overwritten but will remain valid over an arbitrary number of write cycles until another LMR cycle is performed or power is removed.

The load write mask register cycle is performed using DRAM write cycle timing, except DSF is held high on the falling edge of $\overline{RAS}$ and held low on the falling edge of $\overline{CAS}$. A binary code is input to the write mask register via the random I/O pins and latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later. Byte write control can be applied to the write mask during load the write mask register cycle. The persistent write-per-bit mode can then be used in exactly the same way as the non-persistent write-per-bit mode, except the input data on the falling edge of $\overline{RAS}$ is ignored. When the device is set to the persistent write-per-bit mode, it will remain in this mode and will be reset only by a $\overline{CAS}$-before-$\overline{RAS}$ refresh with option reset cycle (Figure 4). A hidden refresh cycle will also end the persistent write-per-bit mode, regardless of the state of DSF.



Mask Data = 1 : Write to I/O Enabled
= 0 : Write to I/O Disabled

Figure 4. Example of Persistent Write-Per-Bit

block write

The block write feature allows up to 64 bits of data to be written simultaneously to one row of the memory array. This function is implemented as (4 columns × 4 DQs) repeated in four quadrants. In this manner, each of the four one-megabit quadrants may have up to 4 consecutive columns written at a time with up to 4 DQs per column (see Figure 5).

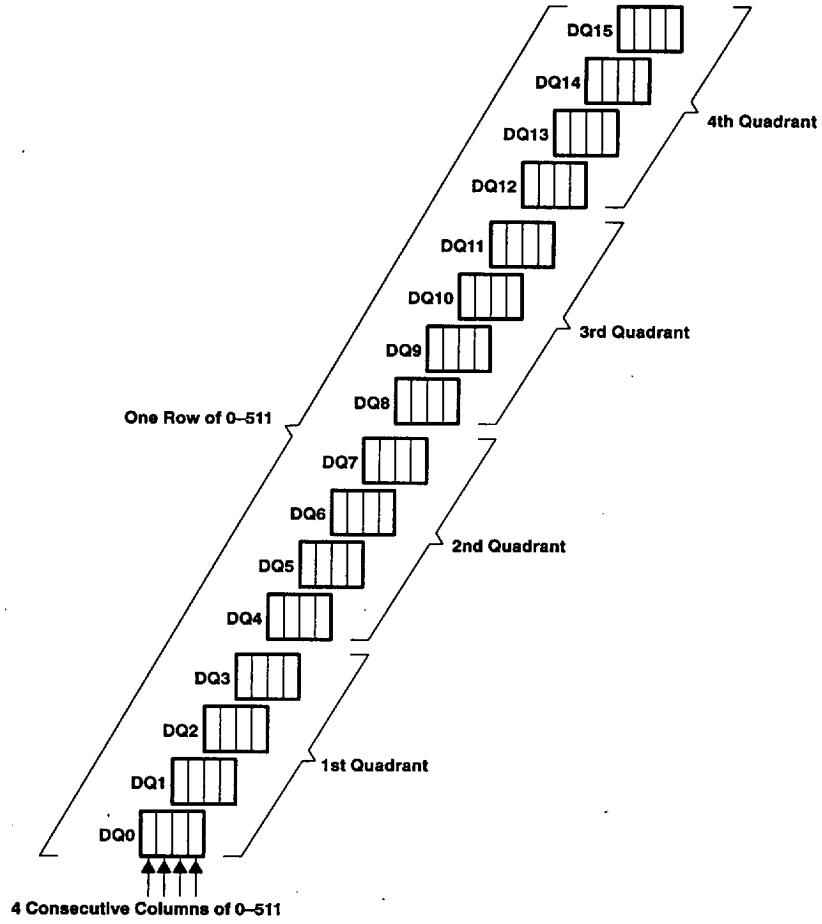


Figure 5. Block Write

Each one-megabit quadrant has a 4-bit column mask to mask off any or all of the four columns from being written with data. Non-persistent write-per-bit or persistent write-per-bit functions can be applied to the block write operation to provide write masking options. The DQ data is provided by 4 bits from the on-chip color register. Bits 0–3 from the 16-bit write mask, bits 0–3 from the 16-bit column mask and bits 0–3 from the 16-bit color data register configure the block write for the 1st quadrant, while bits 4–7, 8–11, 12–15, control the other quadrants in a similar fashion.

TEXAS INSTRUMENTS
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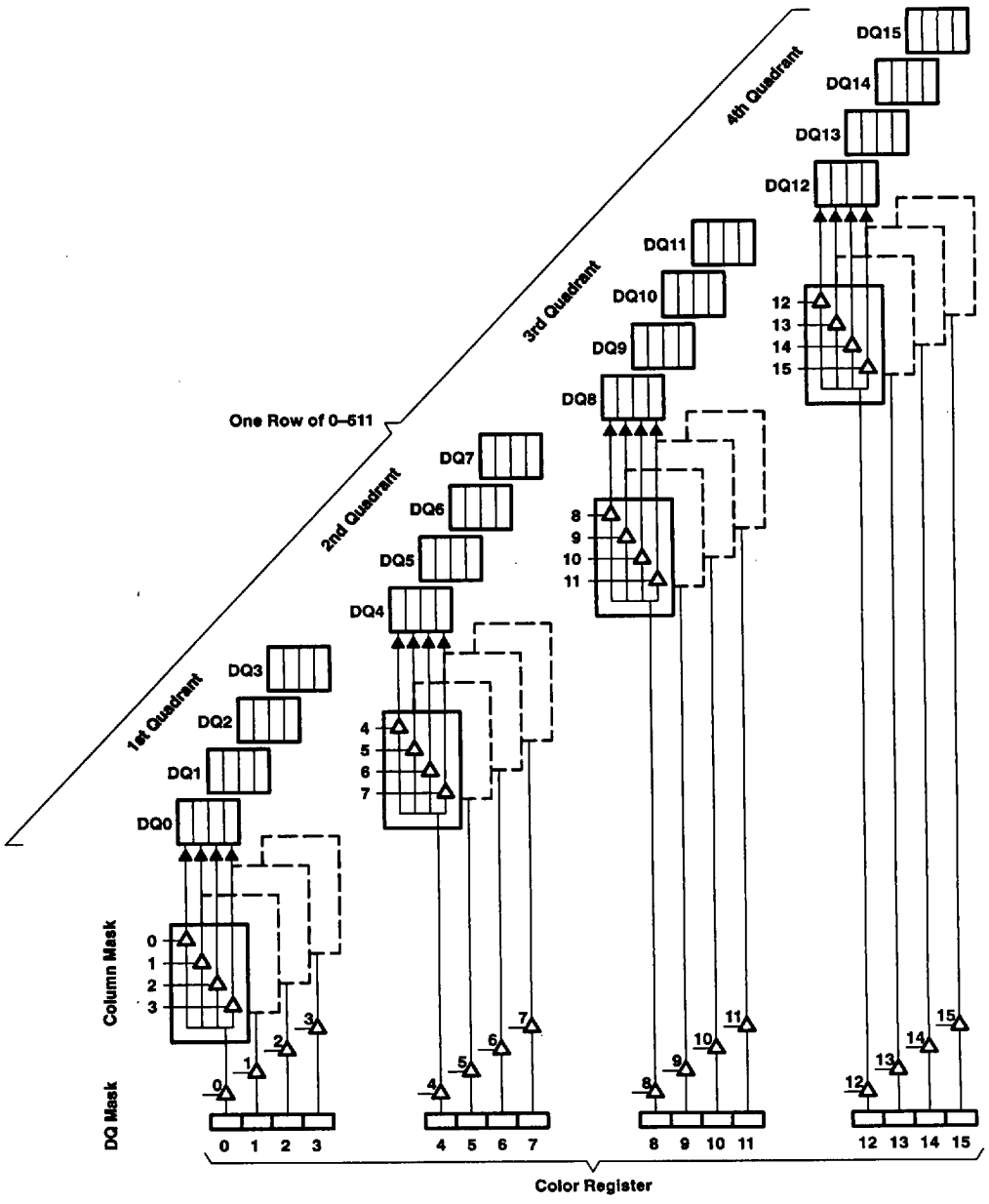

Figure 6. Block Write With Masks

Every 4 columns make a block, which makes 128 blocks along one row. Block 0 comprises columns 0–3, block 1 comprises columns 4–7, block 2 comprises columns 8–11, etc., as below (Figure 7).

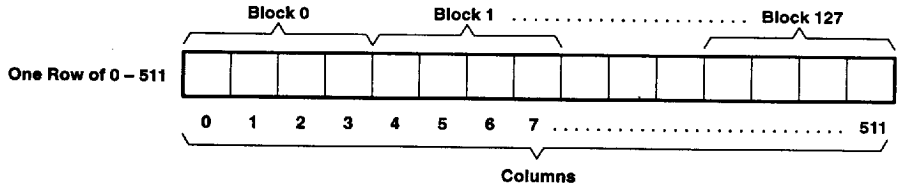

Figure 7. Block Organization

During block write cycles, only the seven most significant column addresses (A2–A8) are latched on the falling edge of $\overline{CAS}$ to decode one of the 128 blocks. Address bits A0–A1 are ignored. (Each one-megabit quadrant has the same block selected.)

A block write cycle is entered in a manner similar to a DRAM write cycle except with DSF held high on the falling edge of $\overline{CAS}$. As in a DRAM write operation, $\overline{WEL}$ and $\overline{WEU}$ enable the corresponding lower and upper DRAM DQ bytes to be written, respectively. The column mask data is input via the DQs and is latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later. The 16-bit color data register must be loaded prior to performing a block write, as described below. Refer to the write-per-bit section for details on use of the write mask capability, allowing additional performance options.

Example of block write:

block write column address = 110000000 (A0–A8 from left to right)

	bit 0			bit 15
color data register =	1011	1011	1100	0111
write mask =	1110	1111	1111	1011
column mask =	1111	0000	0111	1010
	1st Quad	2nd Quad	3rd Quad	4th Quad

Column address bits A0 and A1 are ignored. Block 0 (columns 0–3) is selected for each one-megabit quadrant. The first quadrant has DQ0–DQ2 written with bits 0–2 from the color data register (101) to all four columns of Block 0. DQ3 is not written and retains its previous data due to the write mask register bit 3 being a 0.

The second quadrant (DQ4–DQ7) has all four columns masked off due to the column mask bits 4–7 being 0, so that no data is written.

The third quadrant (DQ8–DQ11) has its four DQs written with bits 8–11 from the color data register (1100) to columns 1–3 of its Block 0. Column 0 is not written and retains its previous data on all four DQs due to the column mask register bit 8 being 0.

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The fourth quadrant (DQ12–DQ15) has DQ12, DQ14, and DQ15 written with bits 12, 14, and 15 from the color data register to column 0 and column 2 of its Block 0. DQ13 retains its previous data on all columns, due to the write mask. Columns 1 and 3 retain their previous data on all DQs due to the column mask. If the previous data for the quadrant was all 0s, the fourth quadrant would contain the following data pattern after the block write operation shown in the previous example.

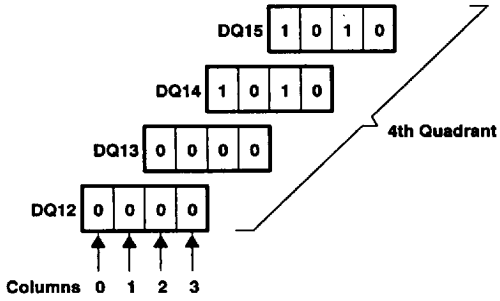
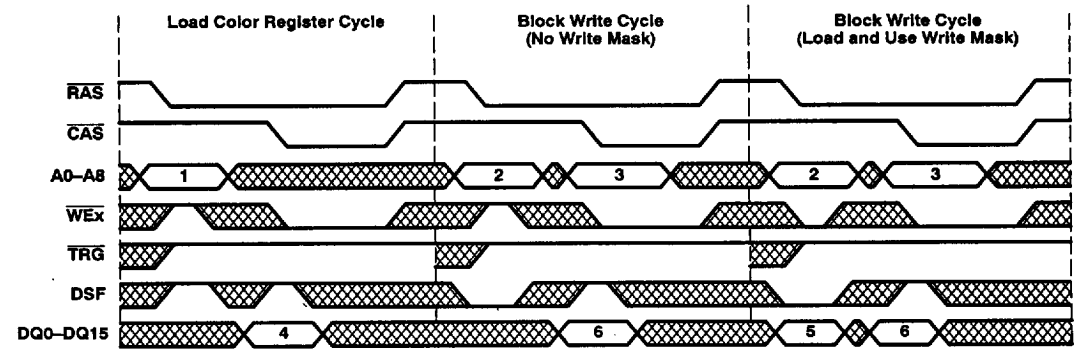


Figure 8. Example of Fourth Quandrant after Bock Write

load color register

The load color register cycle is performed using normal DRAM write cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. The color register is loaded from pins DQ0–DQ15, which are latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later. If only one of the write enables is low, only the corresponding byte of the color register is loaded. When the color register is loaded, it retains data until power is lost or until another load color register cycle is performed. (Figure 9, Figure 10).

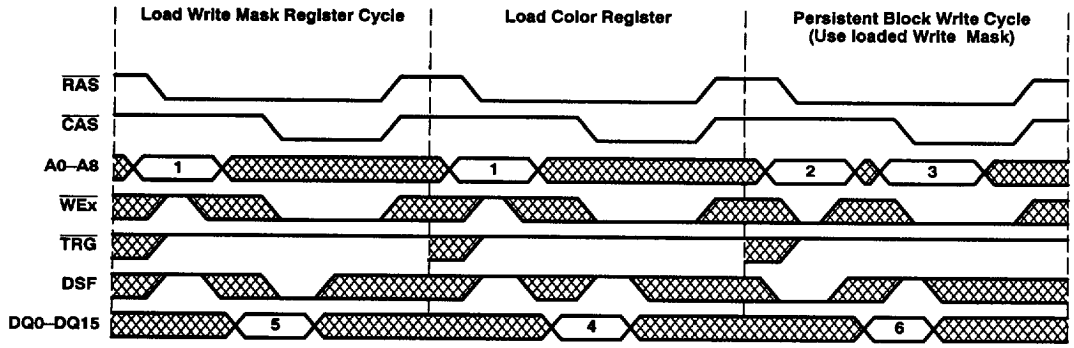


Legend:

2. Refresh Address
2. Row Address
2. Block Address (A2–A8)
2. Color Register Data
2. DQ Mask Data: DQ0–DQ15 are latched on $\overline{RAS}$ falling edge.
2. Column Mask Data: DQ_i–DQ_{i+3} (i=0,4,8,12) are latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later.

= Don't Care

Figure 9. Example of Block Writes With Write Masks



Legend:

1. Refresh Address
2. Row Address
3. Block Address (A2–A8)
4. Color Register Data
5. Write mask data: DQ0–DQ15 are latched on $\overline{CAS}$ falling edge.
6. Column mask data: DQ_i–DQ_{i+3} (i=0,4,8,12) are latched on either the first $\overline{CASx}$ falling edge or the falling edge of $\overline{WE}$, whichever occurs later

= Don't Care

Figure 10. Example of a Persistent Block Write

DRAM to SAM transfer operation

During the DRAM to SAM transfer operation, one half of a row (256 columns) in the DRAM array is selected to be transferred to the 256-bit serial data register. The transfer operation is invoked by bringing $\overline{TRG}$ low and holding $\overline{WEL}$ and $\overline{WEU}$ high on the falling edge of $\overline{RAS}$. The state of DSF, which is latched on the falling edge of $\overline{RAS}$, determines whether the read transfer operation or the split register read transfer operation will be performed.

Table 4. SAM Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CAS}$ FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	$\overline{CAS}$	$\overline{TRG}$	$\overline{WEx}$‡	DSF	DSF	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$ $\overline{WEL}$ $\overline{WEU}$	
Read transfer	1	0	1	0	X	Row Addr	Tap Point	X	X	RT
Split-register read transfer	1	0	1	1	X	Row Addr	Tap Point	X	X	SRT

† DQ0–DQ15 are latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later.
‡ Logic 0 is selected when either or both $\overline{WEL}$ and $\overline{WEU}$ are low.
X: = Don't care.

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read transfer

A read transfer operation loads data from a selected half of a row in the DRAM into the SAM. $\overline{TRG}$ is brought low and latched at the falling edge of $\overline{RAS}$. Nine row address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. The nine column address bits (A0–A8) are latched at the falling edge of $\overline{CAS}$, where address bit A8 selects which half of the row will be transferred. Address bits A0–A7 select one of the SAM's 256 available tap points from which the serial data will be read out (Figure 11).

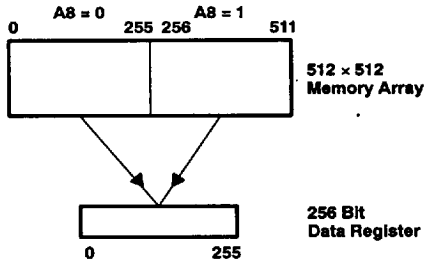


Figure 11. Read Transfer

A read transfer can be performed in three ways: early-load read transfer, real-time or mid-line-load read transfer, and late-load read transfer. Each of these offers the flexibility of controlling the $\overline{TRG}$ trailing edge in the read transfer cycle (Figure 12).

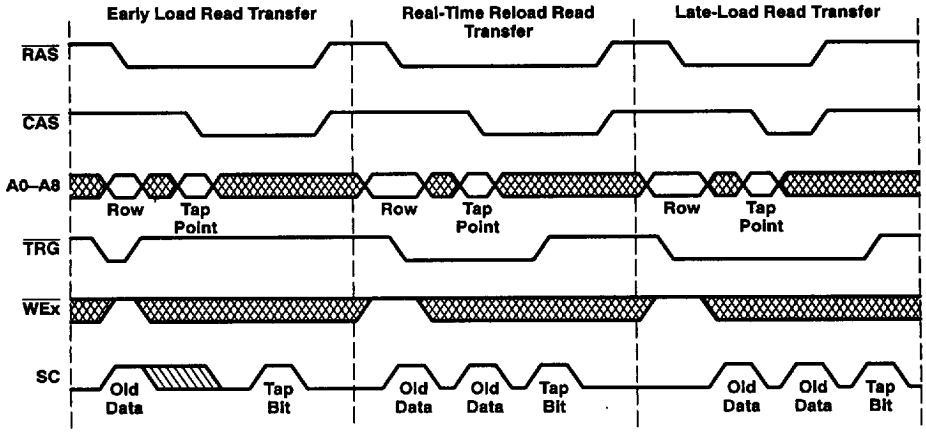


Figure 12. Examples of Read Transfer

split-register read transfer

In the split-register read transfer operation, the serial data register is split into halves. The low half contains bits 0–127, and the high half contains bits 128–255. While one half is being read out of the SAM port, the other half can be loaded from the memory array.

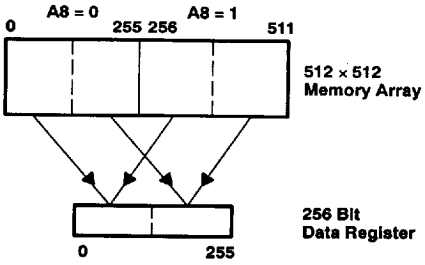
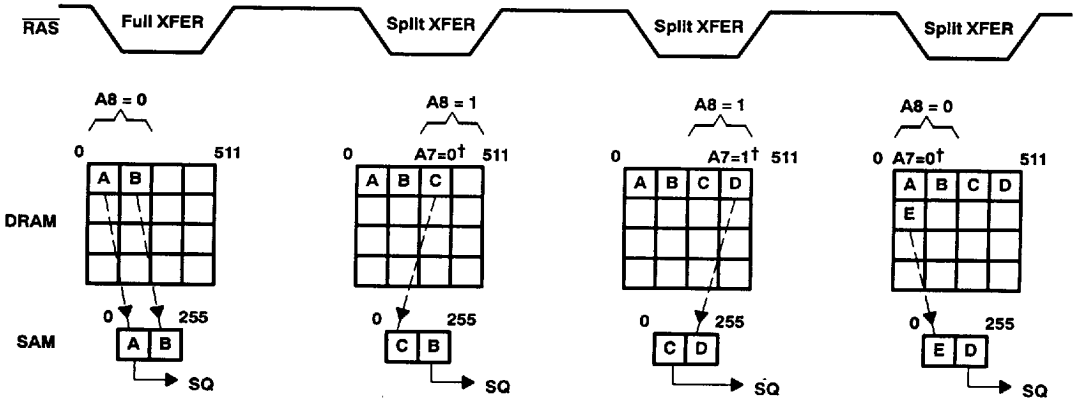


Figure 13. Split Register Read Transfer

To invoke a split-register read transfer cycle, DSF is brought high, $\overline{TRG}$ is brought low, and both are latched at the falling edge of $\overline{RAS}$. Nine row address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. Eight of the nine column address bits (A0–A6 and A8) are latched at the falling edge of $\overline{CAS}$. Column address bit A8 selects which half of the row to be transferred. Column address bits A0–A6 will select one of the 127 tap points in the specified half of the SAM. Column address bit A7 is ignored and the split-register transfer is internally controlled to select the inactive register half.



† A7 shown is internally controlled

Figure 14. Example of Split-Register Read Transfer Operation

A read transfer (non split-register) must precede the first split-register read transfer to ensure proper operation. After the read transfer cycle, the first split-register read transfer can follow immediately without any minimum SC clock requirement. However, there is a minimum requirement of a rising edge of SC between successive split-register read transfer cycles.

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QSF indicates which half of the register is being accessed during serial access operation. When QSF is low, the serial address pointer is accessing the lower (least significant) 128 bits of SAM. When QSF is high, the pointer is accessing the higher (most significant) 128 bits of SAM. QSF changes state upon completing a read transfer cycle. The tap point loaded during the current transfer cycle determines the state of QSF. QSF also changes state when a boundary between two register halves is reached.

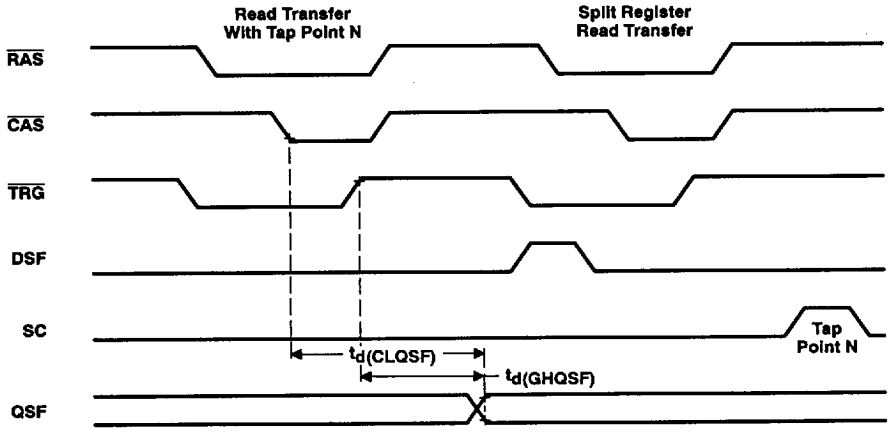

Figure 15. Example of a Split-Register Read Transfer After a Read Transfer

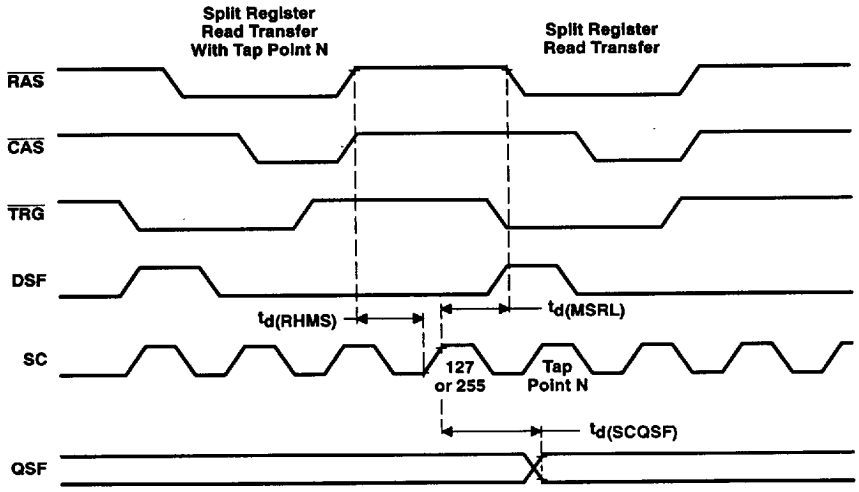

Figure 16. Example of Successive Split-Register Read Transfers

serial access operation

The serial read operation can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during read transfer operations.

Serial data can be read from the SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, then proceeding sequentially to the most significant bit (bit 255) and then wrapping around to the least significant bit (bit 0) (Figure 17).

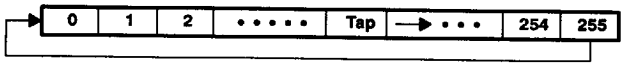

Figure 17. Serial Pointer Direction for Serial Read

For split-register operation, serial data can be read out from the active half of SAM by clocking SC starting at the tap point loaded by the preceding split-register transfer cycle. The serial pointer will then proceed sequentially to the most significant bit of the half, bit 127 or bit 255. If there is a split-register read transfer to the inactive half during this period, the serial pointer will point next to the tap point location loaded by that split register transfer (Figure 18).

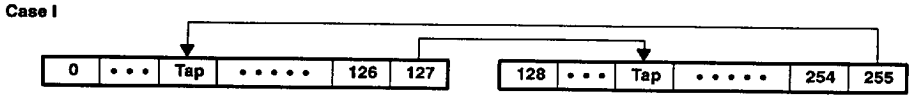

Figure 18. Serial Pointer for Split-Register Read – Case I

If there is no split-register read transfer to the inactive half during this period, the serial pointer will point next to bit 128 or bit 0 respectively (Figure 19).

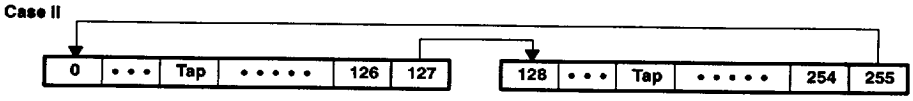

Figure 19. Serial Pointer for Split-Register Read – Case II

power up

To achieve proper device operation, an initial pause of 200 µs is required after power-up, followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles to initialize the DRAM port. A read transfer cycle and two SC cycles are required to initialize the SAM port.

After initialization, the internal state of the TMS55165 is as follows:

	State After Initialization
QSF	Defined by the transfer cycle during initialization
Write mode	Non-persistent mode
Write mask register	Undefined
Color register	Undefined
Serial register tap point	Defined by the transfer cycle during initialization
SAM port	Output mode

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

absolute maximum ratings over operating free-air temperature†

Supply voltage range on any pin except DQ and SQ (see Note 1) ..... – 1 V to 7 V
Voltage range on DQ and SQ (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1.1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	SAM PORT	TMS55165-70		TMS55165-80		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 1 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 5.8 V, V_{CC} = 5.5 V All other pins at 0 to V_{CC}			±10		±10	µA
I_O	Output leakage current (see Note 3)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V			±10		±10	µA
I_{CC1}	Operating current	See Note 4	Standby		165		160	mA
I_{CC1A}	Operating current	$t_{c(SC)}$ = MIN	Active		205		195	
I_{CC2}	Standby current	All clocks = V_{CC}	Standby		5		5	
I_{CC2A}	Standby current	$t_{c(SC)}$ = MIN	Active		50		45	
I_{CC3}	$\overline{RAS}$-only refresh current	See Note 4	Standby		165		160	
I_{CC3A}	$\overline{RAS}$-only refresh current	$t_{c(SC)}$ = MIN	Active		195		185	
I_{CC4}	Page-mode current	$t_{c(P)}$ = MIN (see Note 5)	Standby		100		95	
I_{CC4A}	Page-mode current	$t_{c(SC)}$ = MIN	Active		130		120	
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current	See Note 4	Standby		165		160	
I_{CC5A}	$\overline{CAS}$-before-$\overline{RAS}$ current	$t_{c(SC)}$ = MIN	Active		205		195	
I_{CC6}	Data transfer current	See Note 4	Standby		165		160	
I_{CC6A}	Data transfer current	$t_{c(SC)}$ = MIN	Active		205		195	

NOTES: 3. $\overline{SE}$ is disabled for SQ output leakage tests.
4. Measured with one address change while $\overline{RAS}$ = V_{IL}; $t_{c(rd)}$, $t_{c(W)}$, $t_{c(TRD)}$ = MIN.
5. Measured with one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(DSF)}$	Input capacitance, special function		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SQ and DQ		7	pF
$C_{o(QSF)}$	Output capacitance, QSF		9	pF

NOTE 6: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS55165-70		TMS55165-80		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ (see Note 7)	$t_{d(RLCL)}$ = Max	t_{CAC}		20		20	ns
$t_{a(CA)}$	Access time from column address (see Note 7)	$t_{d(RLCL)}$ = Max	t_{AA}		35		40	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high (see Note 7)	$t_{d(RLCL)}$ = Max	t_{CPA}		40		45	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ (see Note 7)	$t_{d(RLCL)}$ = Max	t_{RAC}		70		80	ns
$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low (see Note 7)		t_{OEA}		20		20	ns
$t_{a(SQ)}$	Access time of SQ from SC high (see Note 7)	C_L = 30 pF	t_{SCA}		20		25	ns
$t_{a(SE)}$	Access time of SQ or QSF from $\overline{SE}$ low (see Note 7)	C_L = 30 pF	t_{SEA}		15		20	ns
$t_{dis(CH)}$	Random output disable time from $\overline{CAS}$ high (see Note 8)	C_L = 50 pF	t_{OFF}	0	20	0	20	ns
$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high (see Note 8)	C_L = 50 pF	t_{OEZ}	0	20	0	20	ns
$t_{dis(SE)}$	Serial output or QSF disable time from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	15	0	20	ns

NOTES: 7. Switching times for RAM port output are measured with a load equivalent to 1 TTL load and 50 pF. Data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V. Switching times for SAM port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V.

8. $t_{dis(CH)}$, $t_{dis(G)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

TEXAS INSTRUMENTS
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timing requirements over recommended ranges of supply voltage and operating free-air temperature†

			TMS55165-70		TMS55165-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 9)	t_{RC}	130		150		ns
$t_{c(W)}$	Write cycle time	t_{WC}	130		150		ns
$t_{c(rdW)}$	Read-modify-write cycle time	t_{RMW}	170		195		ns
$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	45		50		ns
$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{PRMW}	85		90		ns
$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	130		150		ns
$t_{c(SC)}$	Serial clock cycle time (see Note 9)	t_{SCC}	22		30		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CPN}	10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 10)	t_{CAS}	20	10 000	20	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	50		60		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 11)	t_{RAS}	70	10 000	80	10 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{WEx}$ low	t_{WP}	10		15		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		20		20		ns
$t_{w(SCH)}$	Pulse duration, SC high (see Note 9)	t_{SC}	5		10		ns
$t_{w(SCL)}$	Pulse duration, SC low (see Note 9)	t_{SCP}	5		10		ns
$t_{w(GH)}$	Pulse duration, $\overline{TRG}$ high	t_{TP}	20		20		ns
$t_{w(RL)P}$	Pulse duration, $\overline{RAS}$ low (page mode)	t_{RASP}	70	100 000	80	100 000	ns
$t_{su(CA)}$	Setup time, column address before $\overline{CAS}$ low	t_{ASC}	0		0		ns
$t_{su(SFC)}$	Setup time, DSF before $\overline{CAS}$ low	t_{FSC}	0		0		ns
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	0		0		ns
$t_{su(WMR)}$	Setup time, $\overline{WEx}$ before $\overline{RAS}$ low	t_{WSR}	0		0		ns
$t_{su(DQR)}$	Setup time, DQ before $\overline{RAS}$ low	t_{MS}	0		0		ns
$t_{su(TRG)}$	Setup time, $\overline{TRG}$ high before $\overline{RAS}$ low	t_{THS}	0		0		ns
$t_{su(SE)}$	Setup time, $\overline{SE}$ high before $\overline{RAS}$ low	t_{SER}	0		0		ns
$t_{su(SFR)}$	Setup time, DSF low before $\overline{RAS}$ low	t_{FSR}	0		0		ns
$t_{su(DCL)}$	Setup time, data before $\overline{CAS}$ low	t_{DSC}	0		0		ns
$t_{su(DWL)}$	Setup time, data before $\overline{WEx}$ low	t_{DSW}	0		0		ns
$t_{su(rd)}$	Setup time, read command $\overline{WEx}$ high before $\overline{CAS}$ low	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Setup time, early write command, $\overline{WEx}$ low before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write setup time, $\overline{WEx}$ low before $\overline{CAS}$ high	t_{CWL}	15		20		ns
$t_{su(WRH)}$	Write setup time, $\overline{WEx}$ low before $\overline{RAS}$ high with $\overline{TRG}$ = $\overline{WEx}$ = low	t_{RWL}	15		20		ns
$t_{h(CLCA)}$	Hold time, column address after $\overline{CAS}$ low	t_{CAH}	10		15		ns
$t_{h(SFC)}$	Hold time, DSF after $\overline{CAS}$ low	t_{CFH}	10		15		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. All cycle times assume t_t = 3 ns.

10. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].

11. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	TMS55165-70		TMS55165-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low	t_{RAH}	10		10		ns
$t_{h(TRG)}$	Hold time, TRG after $\overline{RAS}$ low	t_{THH}	10		15		ns
$t_{h(RWM)}$	Hold time, write mask, transfer enable after $\overline{RAS}$ low	t_{RWH}	10		10		ns
$t_{h(RDQ)}$	Hold time, DQ after $\overline{RAS}$ low (write mask operation)	t_{MH}	10		10		ns
$t_{h(SFR)}$	Hold time, DSF after $\overline{RAS}$ low	t_{RFH}	10		10		ns
$t_{h(RLCA)}$	Hold time, column-address after $\overline{RAS}$ low (see Note 12)	t_{AR}	30		35		ns
$t_{h(CLD)}$	Hold time, data after $\overline{CAS}$ low	t_{DH}	15		15		ns
$t_{h(RLD)}$	hold time, data after $\overline{RAS}$ low (see Note 12)	t_{DHR}	35		35		ns
$t_{h(WLD)}$	Hold time, data after $\overline{WEx}$ low	t_{DH}	15		15		ns
$t_{h(CHrd)}$	Hold time, read, $\overline{WEx}$ low after $\overline{CAS}$ high (see Note 13)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Hold time, read, $\overline{WEx}$ high after $\overline{RAS}$ high (see Note 13)	t_{RRH}	0		0		ns
$t_{h(CLW)}$	Hold time, write, $\overline{WEx}$ low after $\overline{CAS}$ low	t_{WCH}	15		15		ns
$t_{h(RLW)}$	Hold time, write, $\overline{WEx}$ low after $\overline{RAS}$ low (see Note 12)	t_{WCR}	35		35		ns
$t_{h(WLG)}$	Hold time, $\overline{TRG}$ high after $\overline{WEx}$ low (see Note 14)	t_{OEH}	10		10		ns
$t_{h(SHSQ)}$	Hold time, SQ after SC high	t_{SOH}	5		5		ns
$t_{h(RSF)}$	Hold time, DSF after $\overline{RAS}$ low	t_{FHR}	30		35		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	70		80		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		20		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{WEx}$ low (see Notes 15 and 16)	t_{CWD}	45		45		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 17)	t_{RCD}	20	50	20	60	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	35		40		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CAS}$ high	t_{CAL}	35		40		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{WEx}$ low (see Note 15)	t_{RWD}	95		105		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{WEx}$ low (see Note 15)	t_{AWD}	60		65		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 18)	t_{CHR}	10		15		ns
$t_{d(CLRL)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 18)	t_{CSR}	0		10		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 18)	t_{RPC}	0		0		ns
$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high for DRAM read cycles		20		20		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ	t_{OED}	15		15		ns
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (real-time reload read transfer cycle only)	t_{RTH}	55		60		ns
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 19)	t_{RSD}	70		80		ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 17)	t_{RAD}	15	35	15	40	ns
$t_{d(GLRH)}$	Delay time, $\overline{TRG}$ low to $\overline{RAS}$ high	t_{ROH}	15		15		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{(CHrd)}$ must be satisfied for a read cycle.
14. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
15. Read-modify-write operation only.
16. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
17. The maximum value is specified only to assure $\overline{RAS}$ access time.
18. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.
19. Early-load read transfer cycle only.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)†

		ALT. SYMBOL	TMS55165-70		TMS55165-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 21)	t_{CSD}	20		25		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 20 and 21)	t_{TSL}	5		5		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Notes 20 and 23)	t_{TRD}	–10		–10		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 22)	t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 20)	t_{TSD}	10		15		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split read transfer cycles		20		20		ns
$t_{d(CLTH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high in real-time transfer read cycles	t_{CTH}	5		5		ns
$t_{d(CASH)}$	Delay time, column address to first SC in early load read transfer cycles	t_{ASD}	25		30		ns
$t_{d(CAGH)}$	Delay time, column address to $\overline{TRG}$ high in real-time transfer read cycles	t_{ATH}	10		10		ns
$t_{d(DCL)}$	Delay time, data to $\overline{CAS}$ low	t_{DZC}	0		0		ns
$t_{d(DGL)}$	Delay time, data to $\overline{TRG}$ low	t_{DZO}	0		0		ns
$t_{d(MSRL)}$	Delay time, last (most significant) rising edge of SC to $\overline{RAS}$ low before boundary switch during split read transfer cycles		20		20		ns
$t_{d(SCQSF)}$	Delay time, last (127 or 255) rising edge of SC to QSF switching at the boundary during split read transfer cycles (see Note 24)	t_{SQD}		25		30	ns
$t_{d(CLQSF)}$	Delay time, $\overline{CAS}$ low to QSF switching in transfer read or write cycles (see Note 24)	t_{CQD}		30		35	ns
$t_{d(GHQSF)}$	Delay time, $\overline{TRG}$ high to QSF switching in transfer read or write cycles (see Note 24)	t_{TQD}		25		30	ns
$t_{d(RLQSF)}$	Delay time, $\overline{RAS}$ low to QSF switching in transfer read or write cycles (see Note 24)	t_{RQD}		70		75	ns
$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8	ms
t_t	Transition time	t_T	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 20. Real-time reload read transfer cycle only.
21. Early-load read transfer cycle only.
22. Memory to register (read) transfer cycles only.
23. Late-load read transfer cycle only.
24. Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF and output reference level is V_{OH} / V_{OL} = 2 V/0.8V.

PARAMETER MEASUREMENT INFORMATION

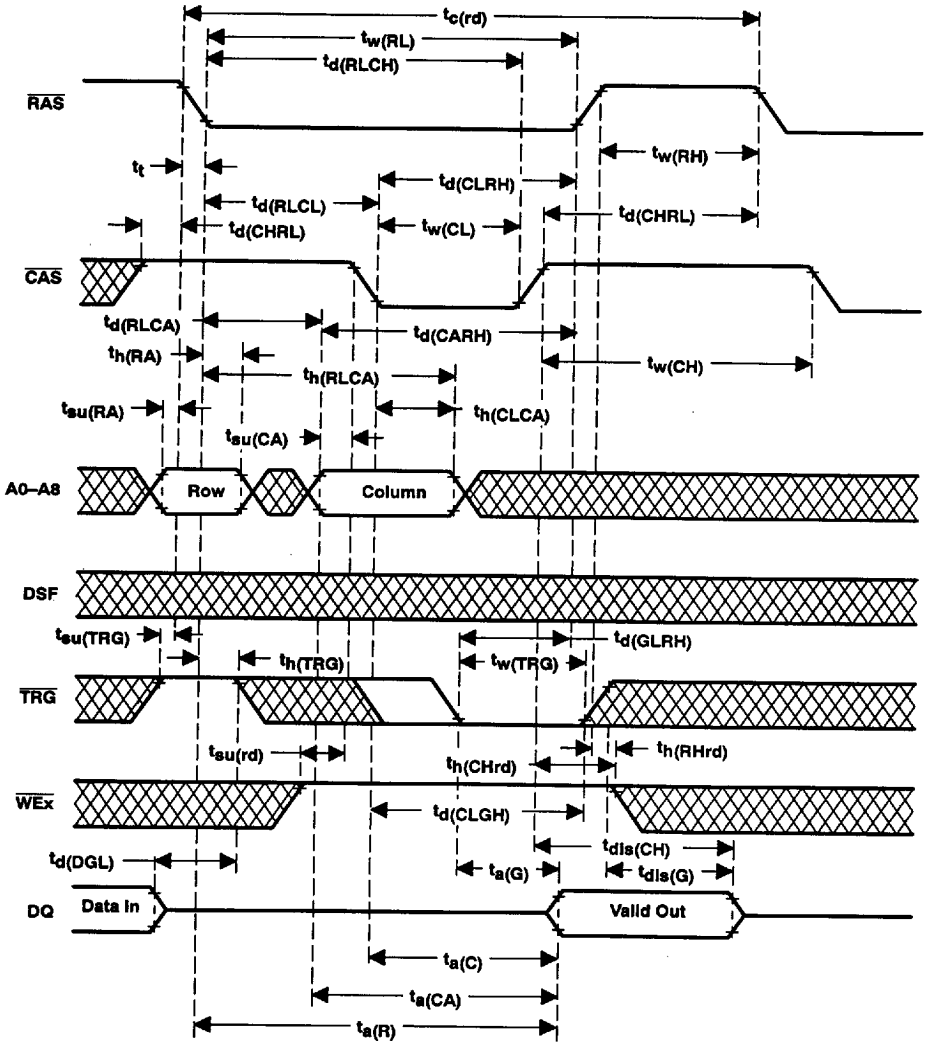

Figure 20. Read Cycle Timing

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POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

PARAMETER MEASUREMENT INFORMATION

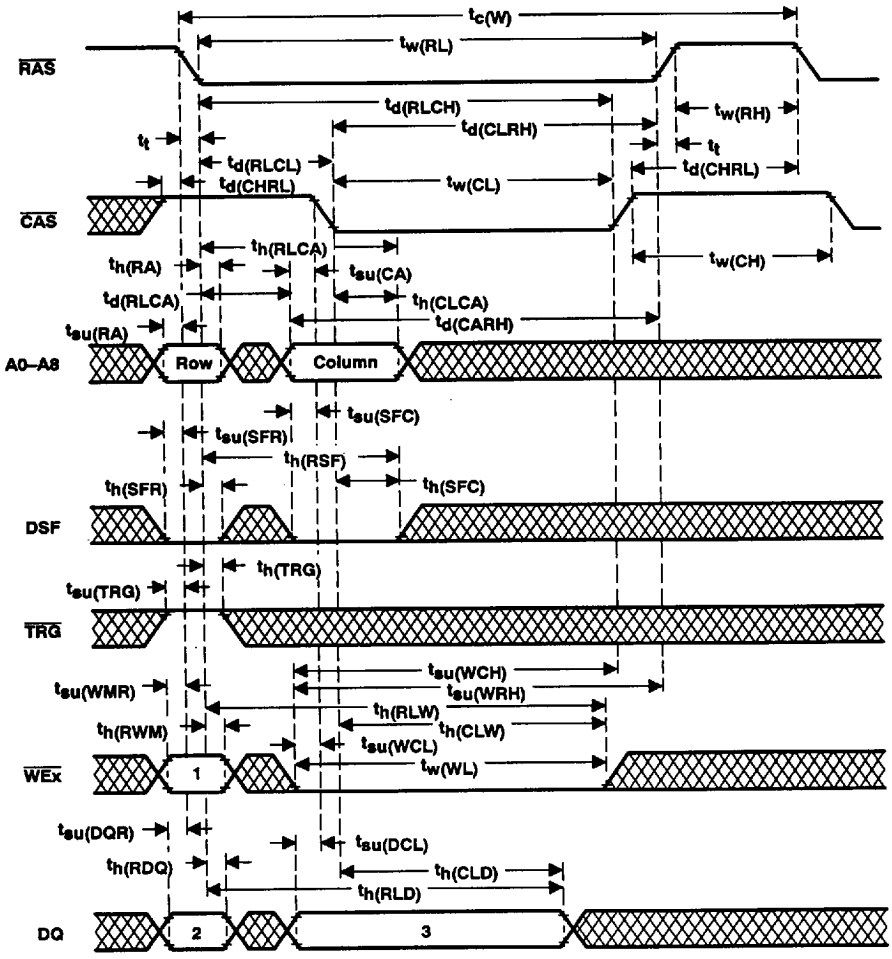


Figure 21. Early Write Cycle Timing

Table 5. Write Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (non-masked)	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

PARAMETER MEASUREMENT INFORMATION

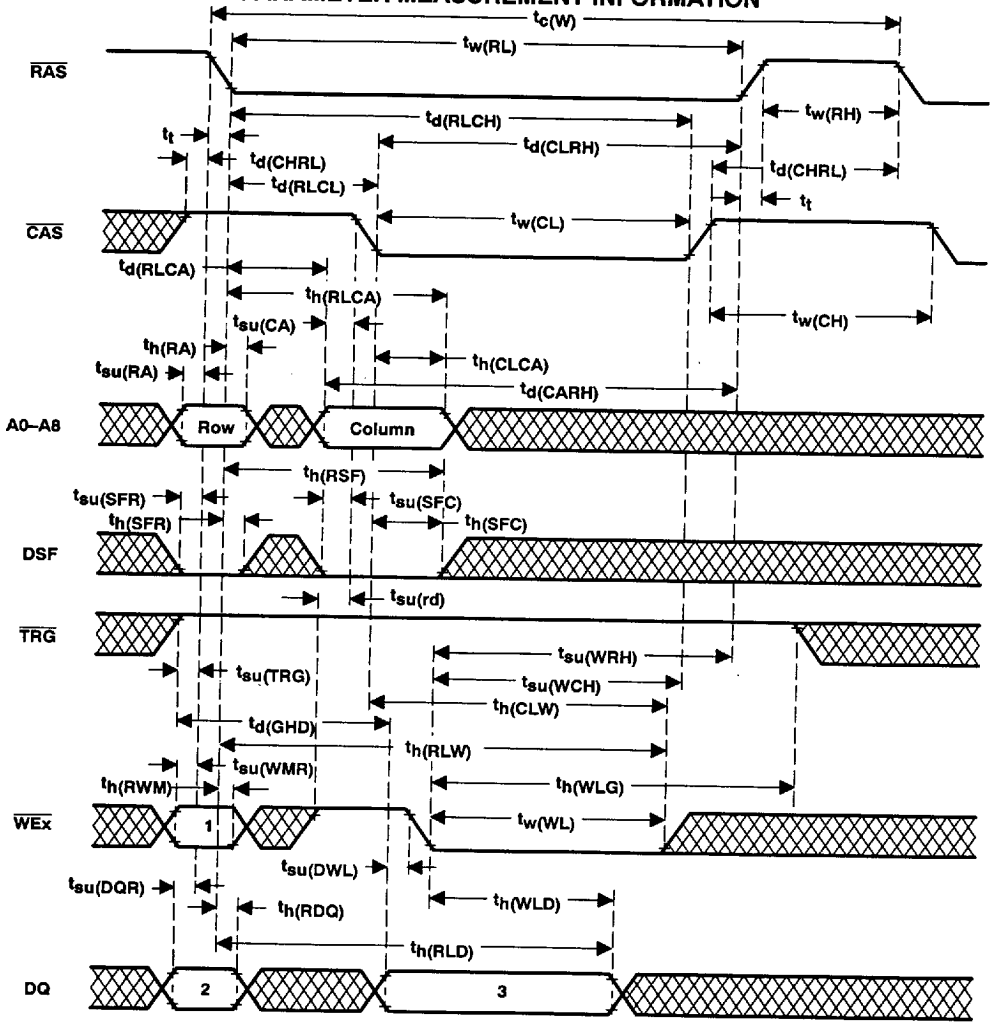


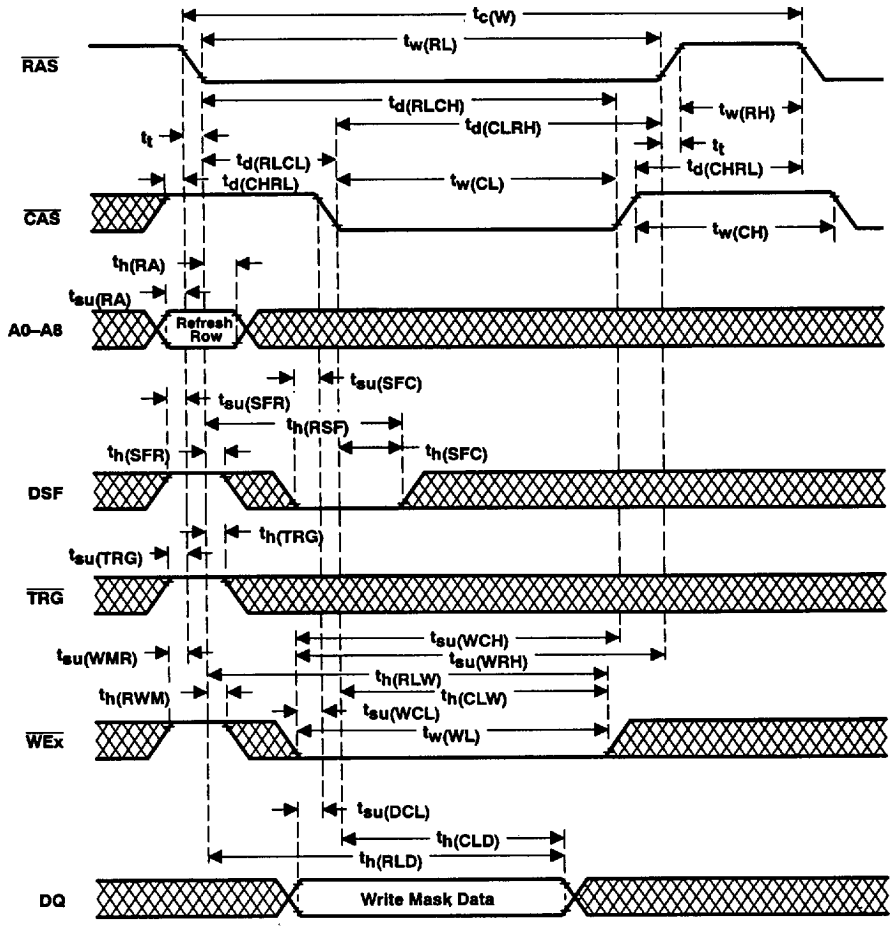
Figure 22. Late Write Cycle Timing (Output-Enable-Controlled Write)

Table 6. Write Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (non-masked)	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

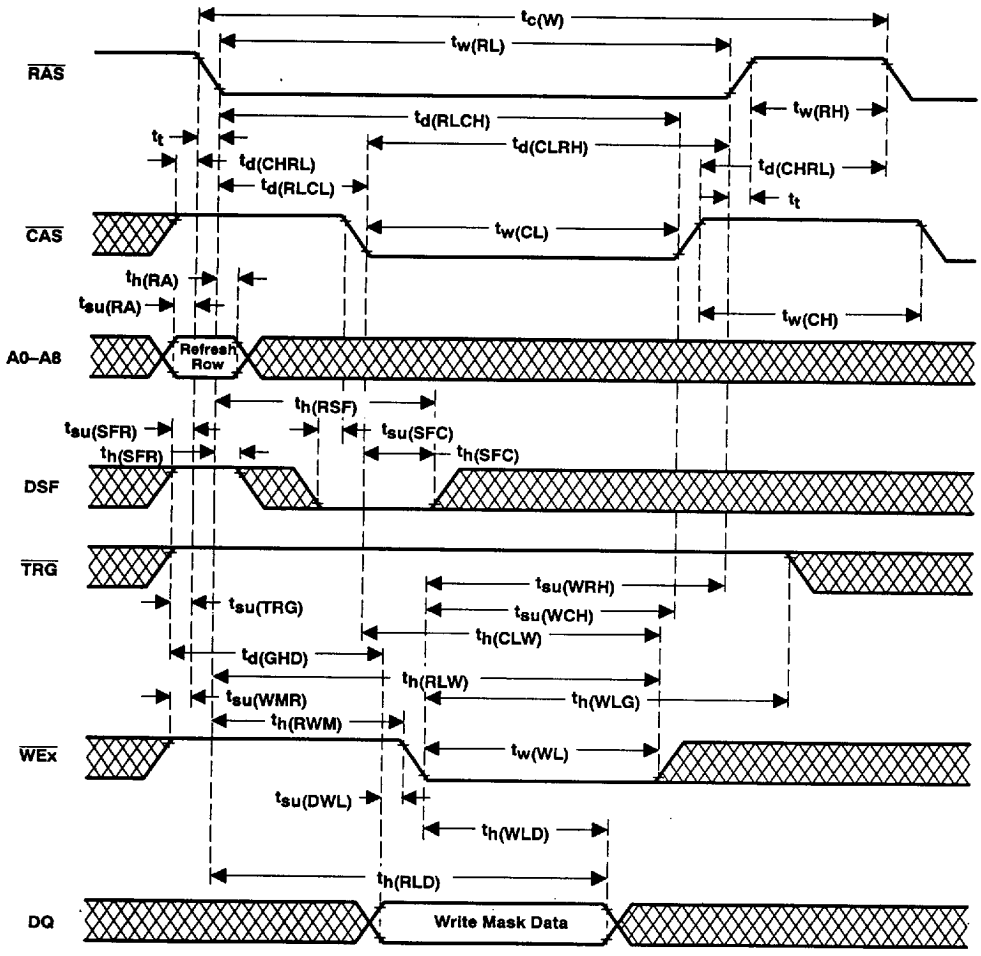
PARAMETER MEASUREMENT INFORMATION



† Load mask register cycle will put the device into the persistent write-per-bit mode.

Figure 23. Load Mask Register Timing (Early Write Load)†

PARAMETER MEASUREMENT INFORMATION



† Load mask register cycle will put the device into the persistent write-per-bit mode.

Figure 24. Load Mask Register Timing (Late Write Load)†

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

PARAMETER MEASUREMENT INFORMATION

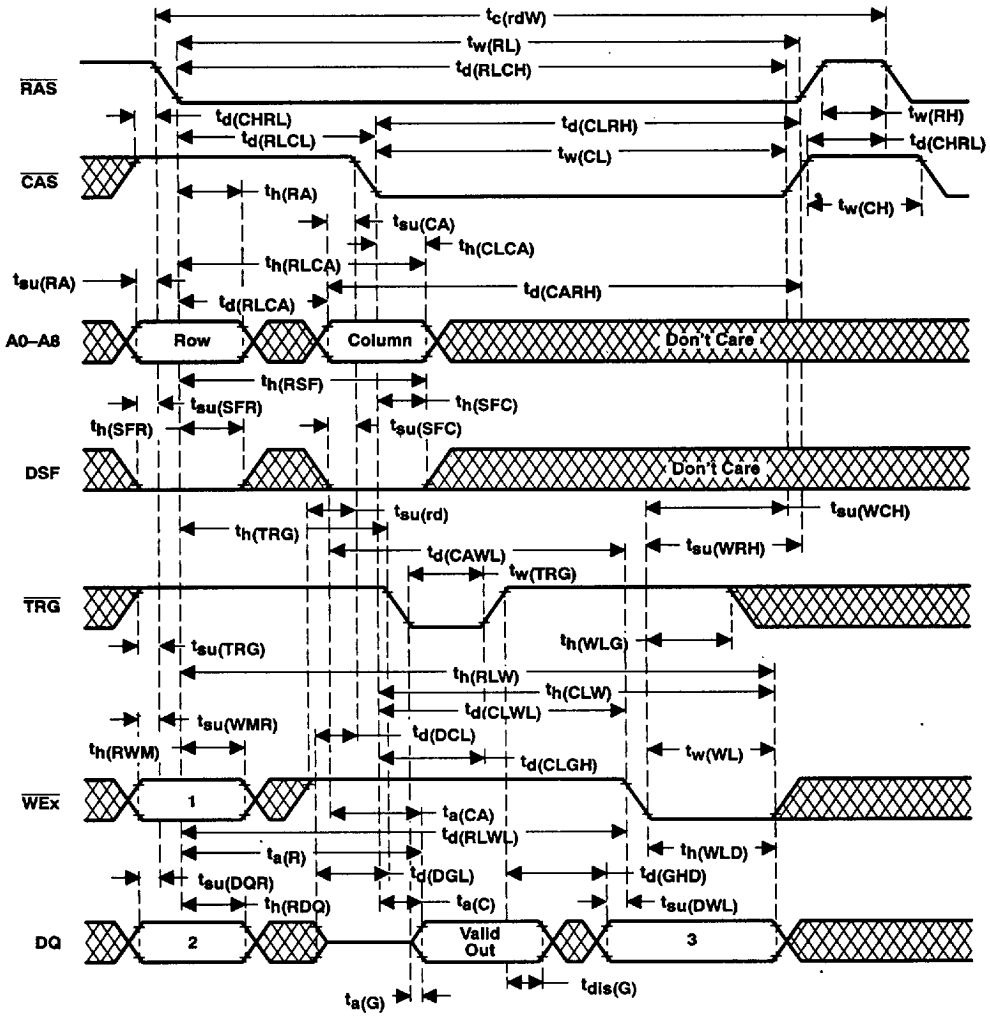
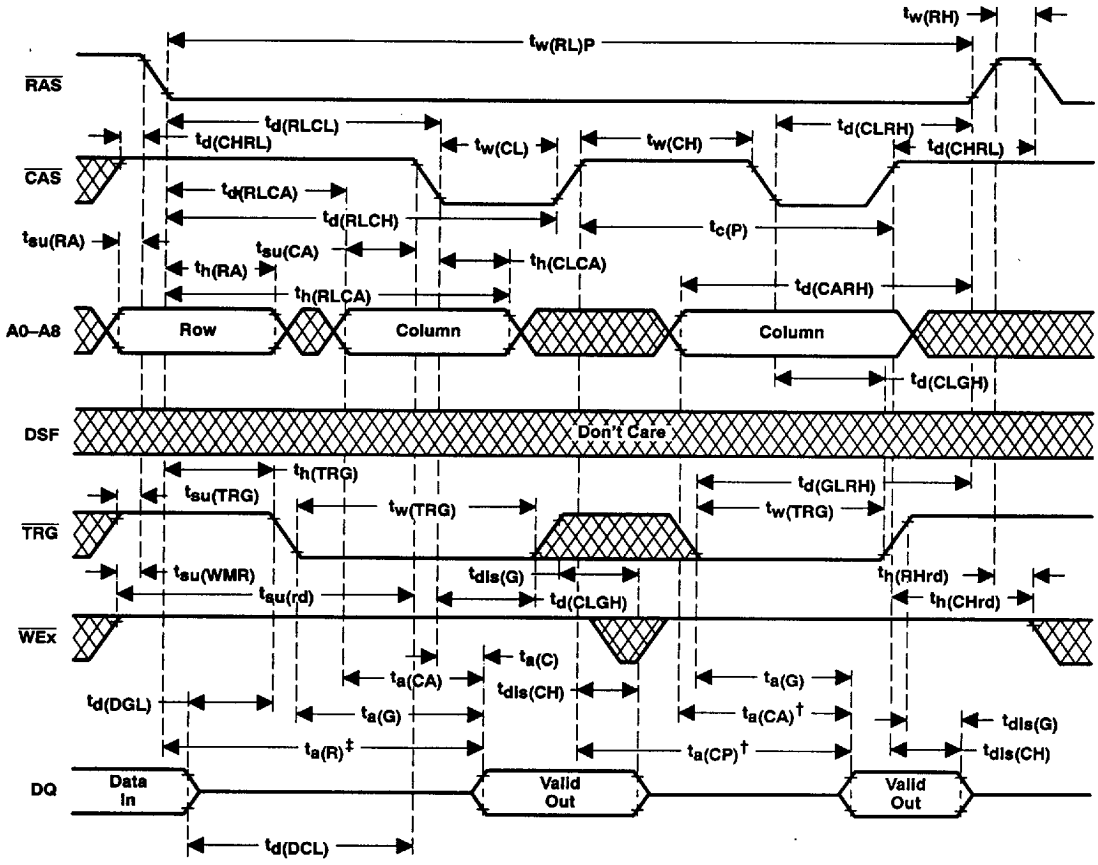


Figure 25. Read-Write/Read-Modify-Write Cycle Timing

Table 7. Write Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (non-masked)	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

PARAMETER MEASUREMENT INFORMATION

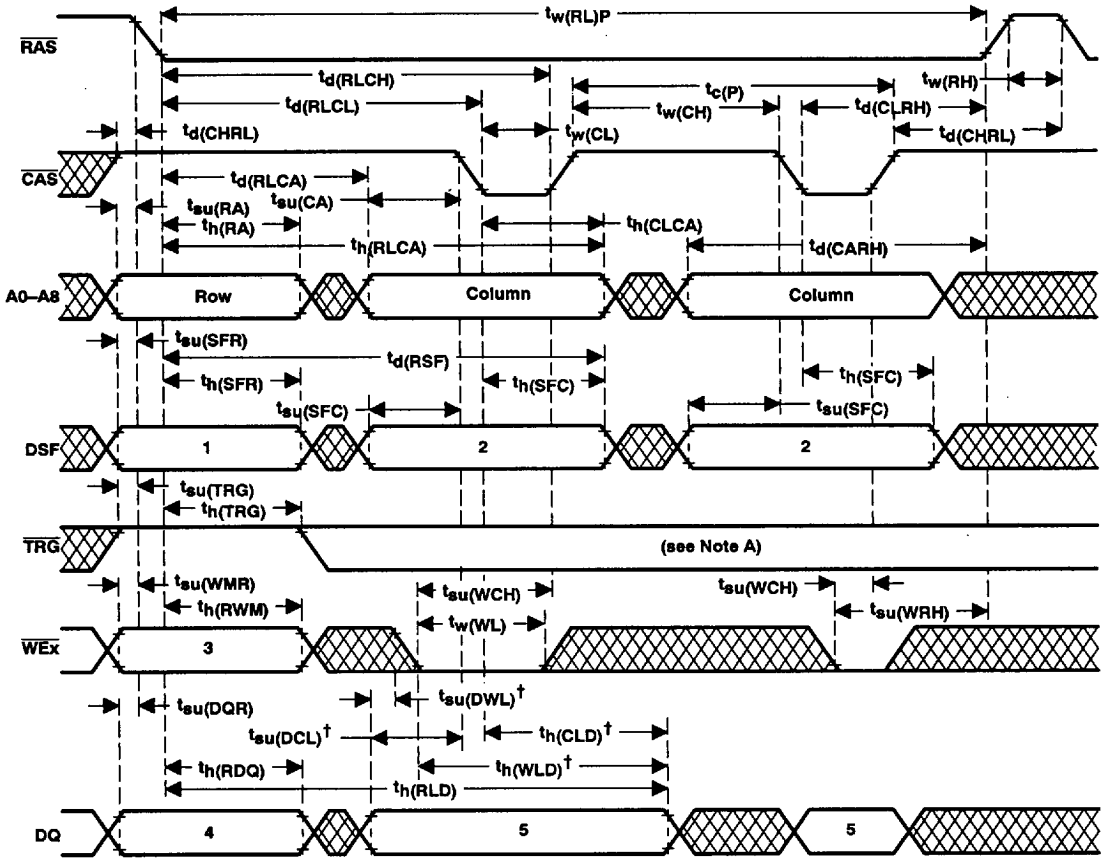


† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output may go from the high-impedance state to an invalid data state prior to the specified access time.
NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.)

Figure 26. Enhanced Page-Mode Read Cycle Timing

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later.

NOTE A: A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write features is used. If the early write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

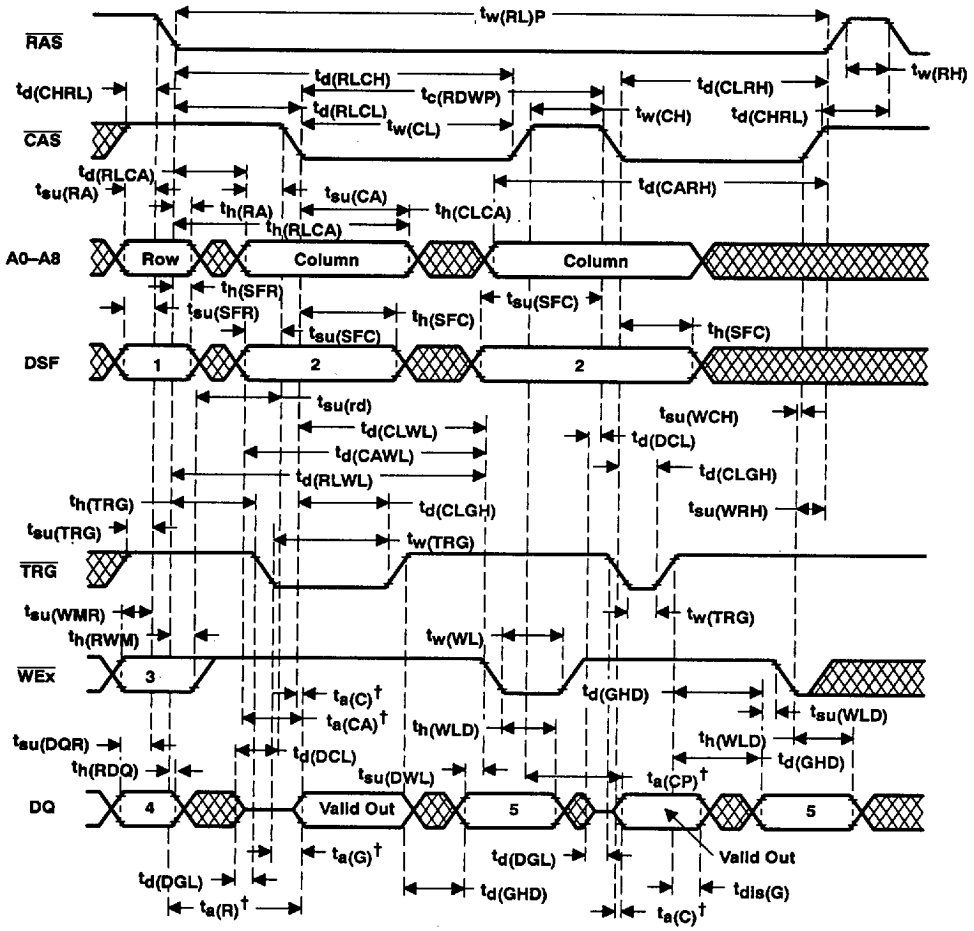
Figure 27. Enhanced Page-Mode Write Cycle Timing

Table 8. Write Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (non-masked)	L	L	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load write mask on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load write mask cycle will set the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CAS}$ is don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



† Output may go from the high-impedance state to an invalid data state prior to the specified access time.
NOTE A: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 28. Enhanced Page-Mode Read-Modify-Write Cycle Timing

Table 9. Write Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (non-masked)	L	L	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load write mask on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$ whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load write mask cycle will set the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CAS}$ is don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION

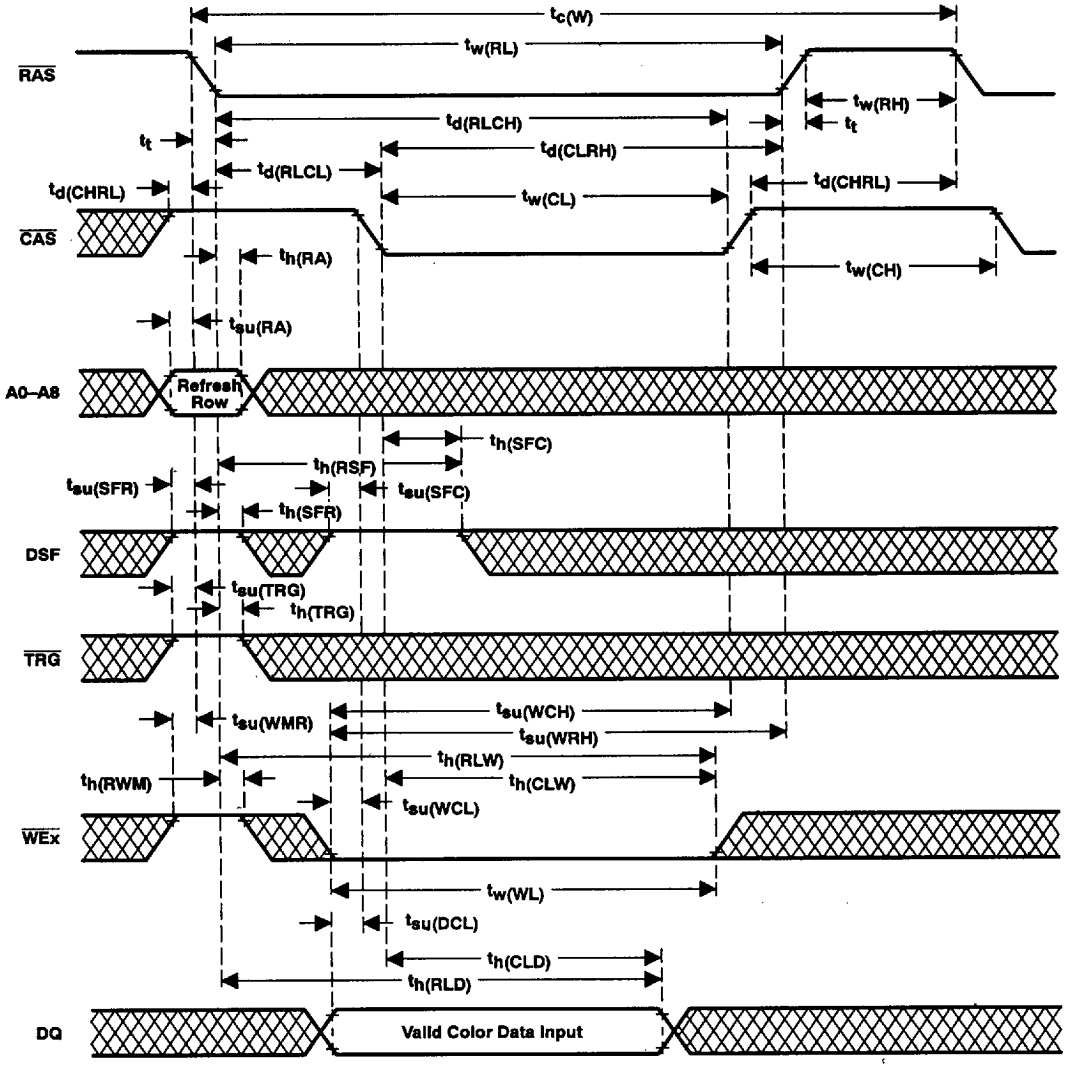


Figure 29. Load Color Register Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION

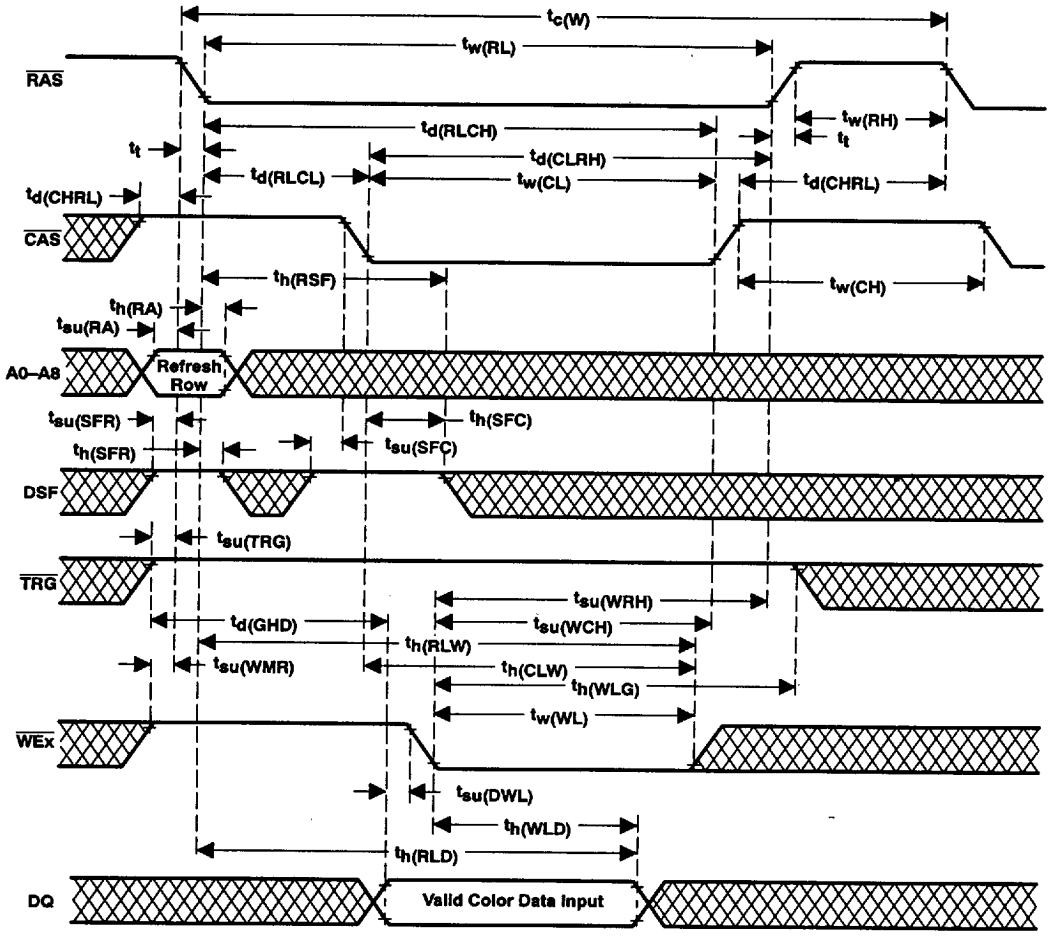


Figure 30. Load Color Register Timing (Late Write Load)

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

PARAMETER MEASUREMENT INFORMATION

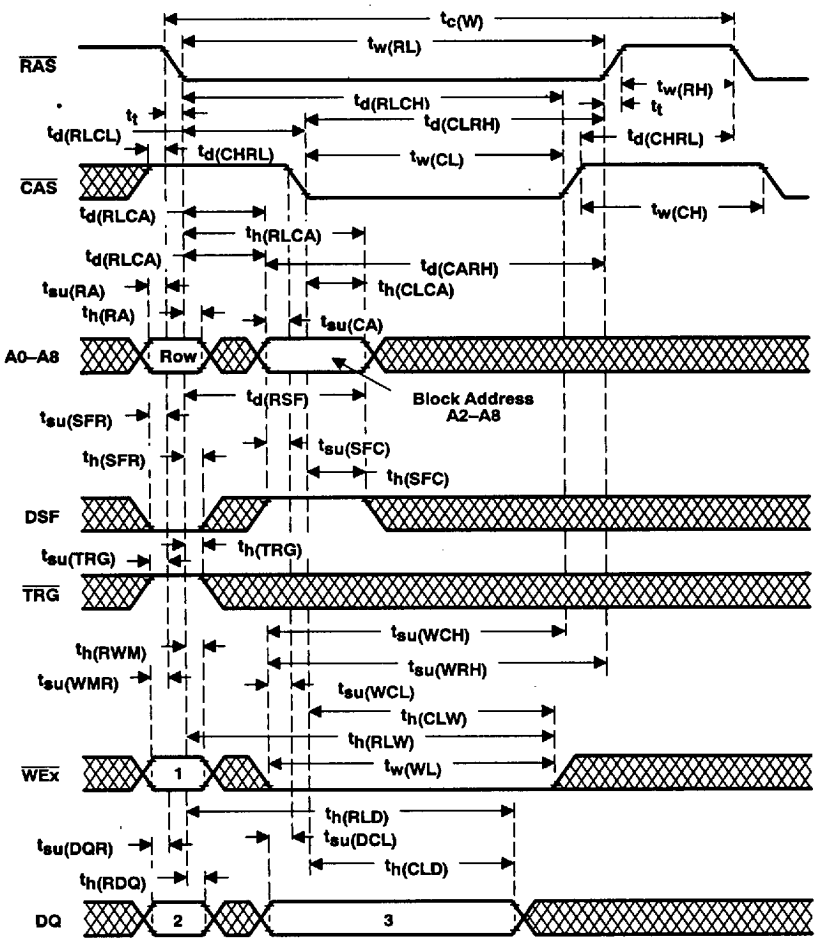


Figure 31. Block Write Timing (Early Write)

Table 10. Block Write Cycle State Table

CYCLE	STATE		
	1	2	3
Block write operation (non-masked)	H	Don't care	Column mask
Block write operation with non-persistent write-per-bit	L	Write mask	Column mask
Block write operation with persistent write-per-bit	L	Don't care	Column mask

Write mask data 0: I/O write disable
1: I/O write enable
Column mask data DQ_i – DQ_{i+3}0: column write disable
(i = 0, 4, 8, 12) 1: column write enable

Example:
DQ_0 — column 0 (address A_1 = 0, A_0 = 0)
DQ_1 — column 1 (address A_1 = 0, A_0 = 1)
DQ_2 — column 2 (address A_1 = 1, A_0 = 0)
DQ_3 — column 3 (address A_1 = 1, A_0 = 1)

PARAMETER MEASUREMENT INFORMATION

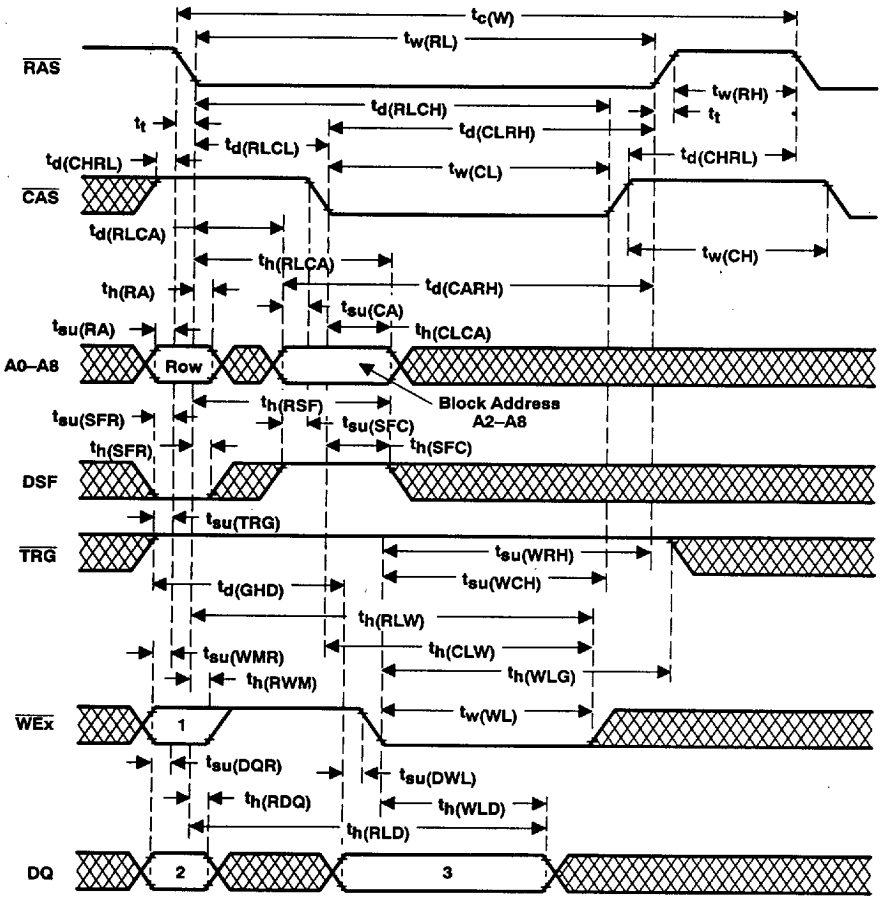


Figure 32. Block Write Timing (Late Write)

Table 11. Block Write Cycle State Table

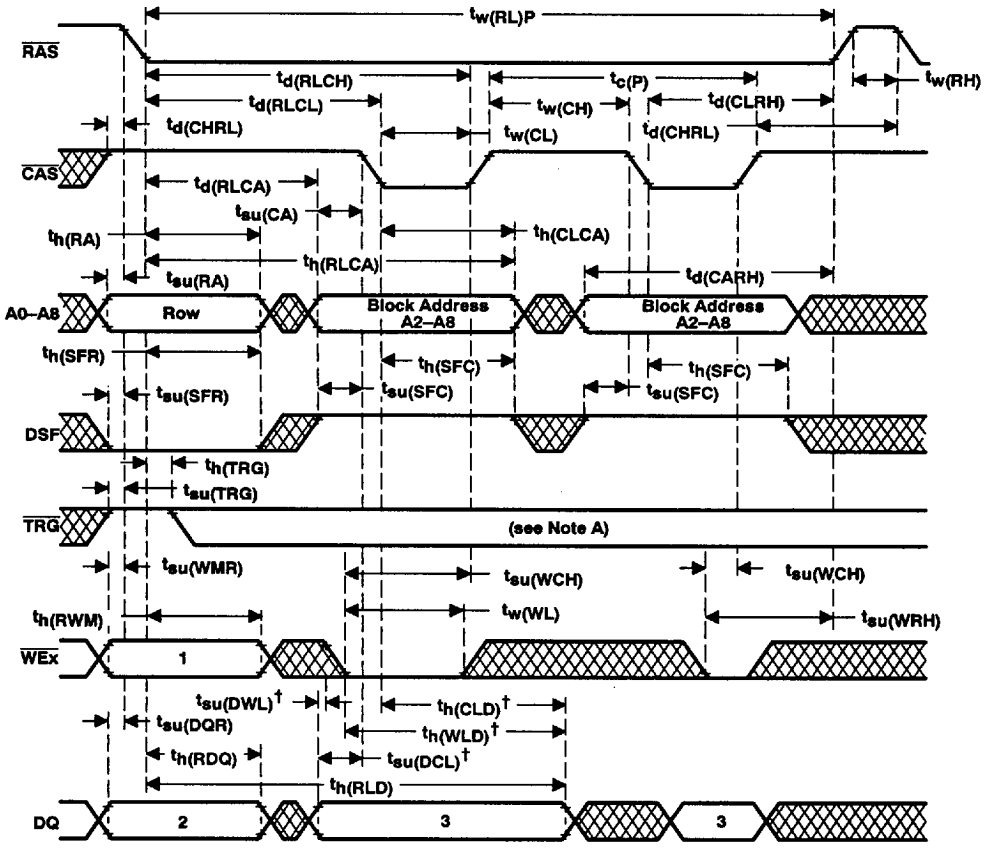
CYCLE	STATE		
	1	2	3
Block write operation (non-masked)	H	Don't care	Column mask
Block write operation with non-persistent write-per-bit	L	Write mask	Column mask
Block write operation with persistent write-per-bit	L	Don't care	Column mask

Write mask data 0: I/O write disable
1: I/O write enable
Column mask data DQ_i – DQ_{i+3}0: column write disable
(i = 0, 4, 8, 12) 1: column write enable

Example:
DQ_0 — column 0 (address A_1 = 0, A_0 = 0)
DQ_1 — column 1 (address A_1 = 0, A_0 = 1)
DQ_2 — column 2 (address A_1 = 1, A_0 = 0)
DQ_3 — column 3 (address A_1 = 1, A_0 = 1)

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

PARAMETER MEASUREMENT INFORMATION



† Referenced the first $\overline{WE}x$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later.

NOTE A: To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write features is used. If the early write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 33. Enhanced Page-Mode Block Write Cycle Timing

Table 12. Block Write Cycle State Table

CYCLE	STATE		
	1	2	3
Block write operation (non-masked)	H	Don't care	Column mask
Block write operation with non-persistent write-per-bit	L	Write mask	Column mask
Block write operation with persistent write-per-bit	L	Don't care	Column mask

Write mask data 0: I/O write disable
1: I/O write enable
Column mask data DQ_i – DQ_{i+3}0: column write disable
(i = 0, 4, 8, 12) 1: column write enable

Example:
DQ_0 — column 0 (address A_1 = 0, A_0 = 0)
DQ_1 — column 1 (address A_1 = 0, A_0 = 1)
DQ_2 — column 2 (address A_1 = 1, A_0 = 0)
DQ_3 — column 3 (address A_1 = 1, A_0 = 1)

PARAMETER MEASUREMENT INFORMATION

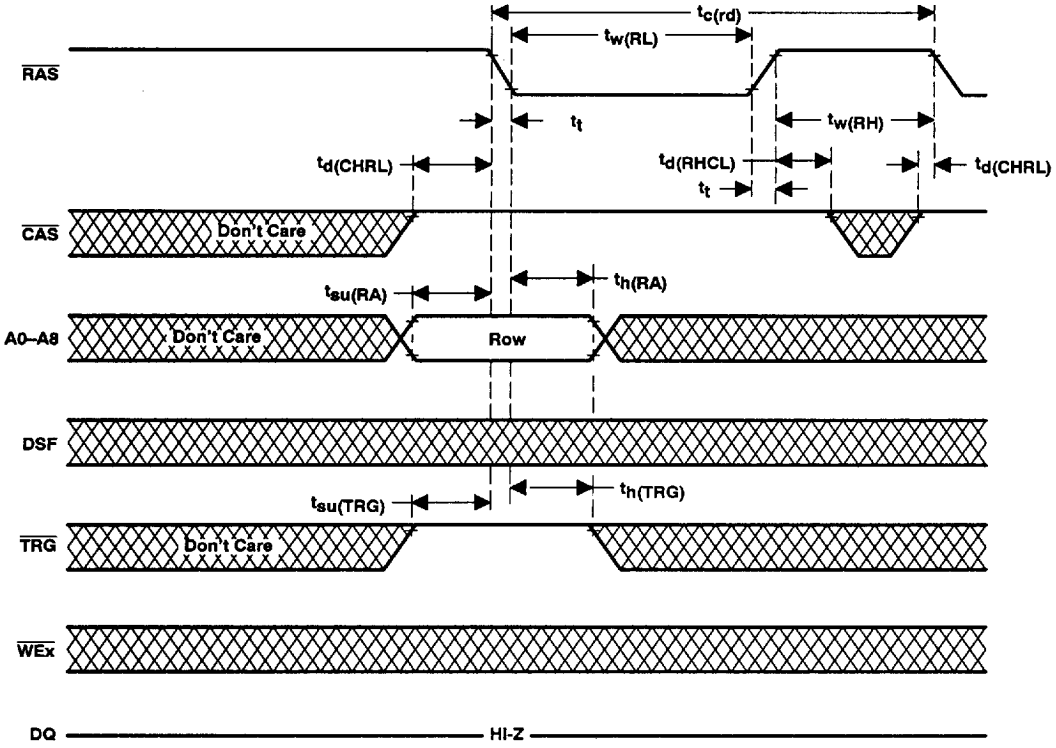


Figure 34. $\overline{\text{RAS}}$-Only Refresh Timing

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POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

PARAMETER MEASUREMENT INFORMATION

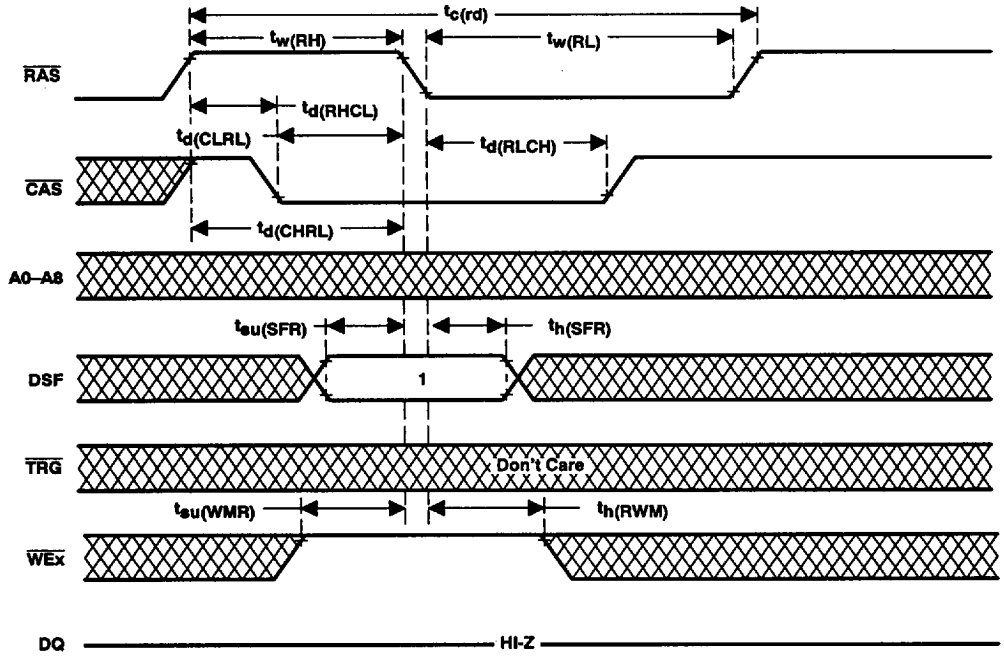


Figure 35. CAS-Before-RAS Refresh

Table 13. CBR Cycle State Table

CYCLE	STATE
	1
CAS-before-RAS refresh with option reset	0
CAS-before-RAS refresh with no reset	1

PARAMETER MEASUREMENT INFORMATION

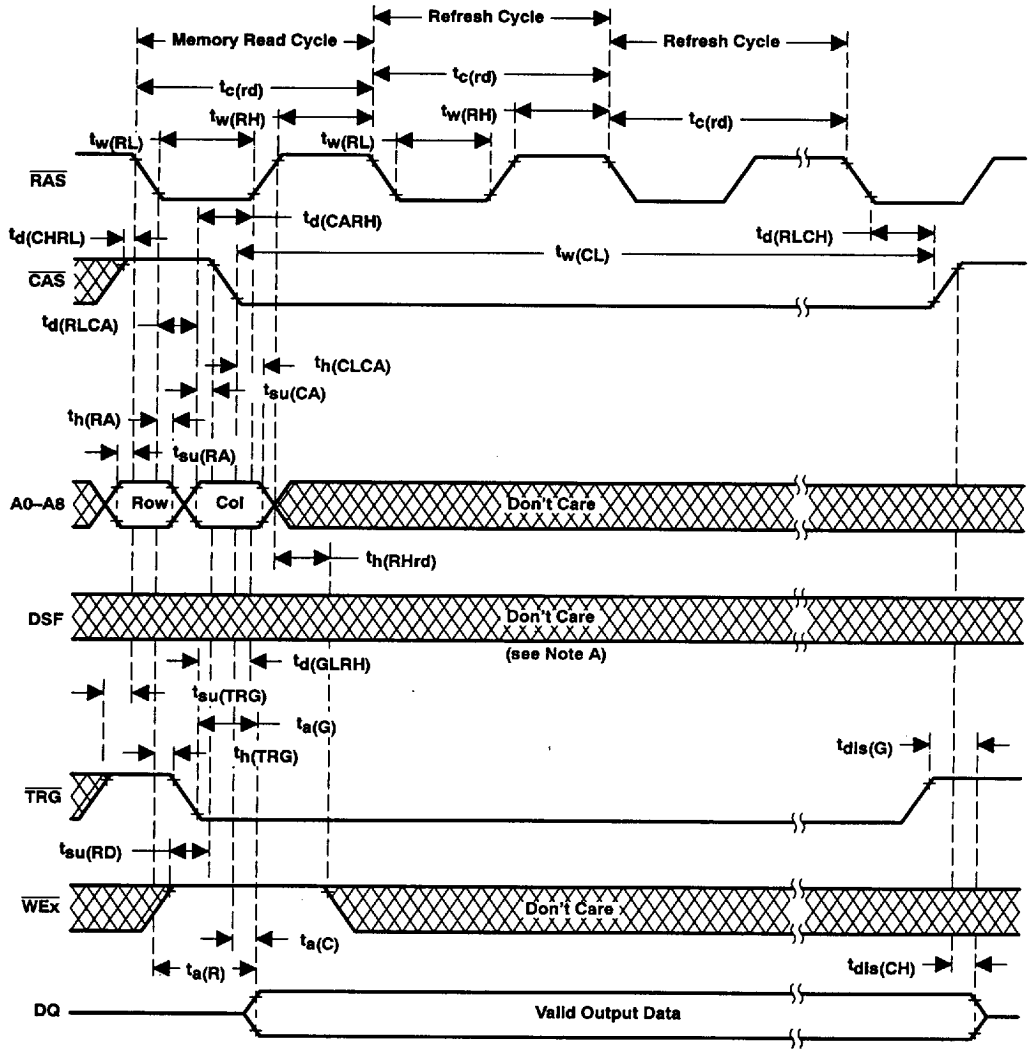
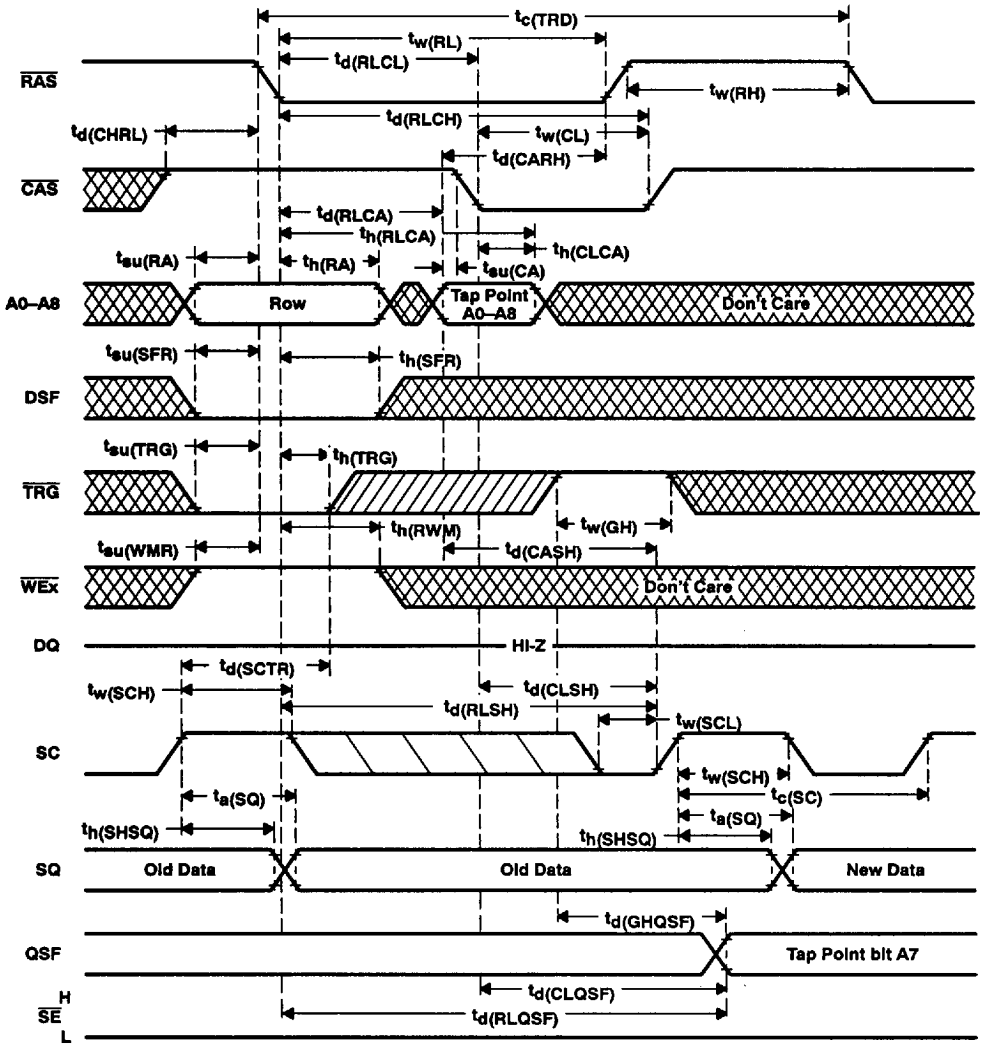


Figure 36. Hidden Refresh Cycle Timing

NOTE A: $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh (option reset) mode will end persistent write-per-bit mode. Hidden refresh will also end the persistent write-per-bit mode regardless of the state of DSF at $\overline{\text{RAS}}$.

PARAMETER MEASUREMENT INFORMATION



† Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH)}$ min.

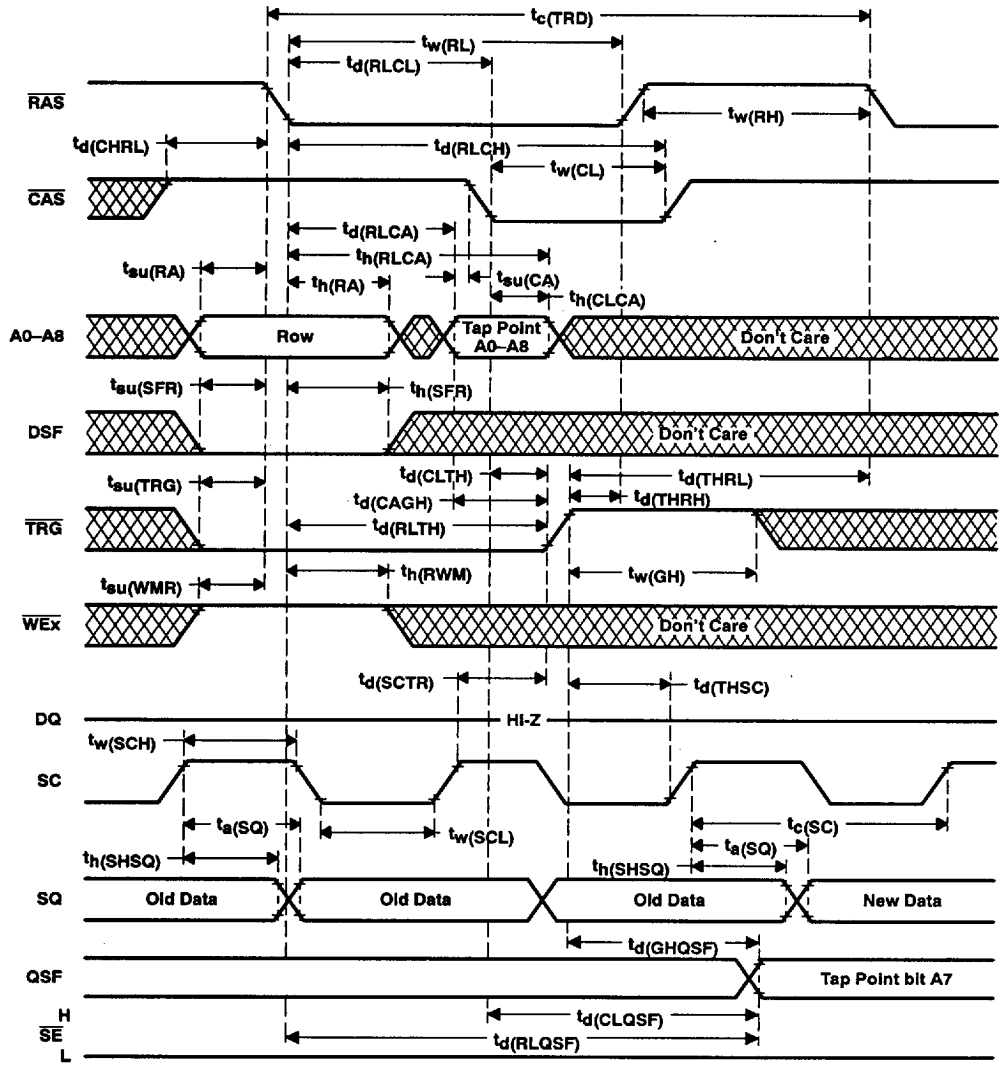
NOTES: A. Random mode (DQ outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: Register tap point, A8: which half of the transferred row.

Figure 37. Read Transfer Timing, Early Load Operation†

PARAMETER MEASUREMENT INFORMATION



† Late load operation is defined as $t_{d(THRH)} < 0$ ns.

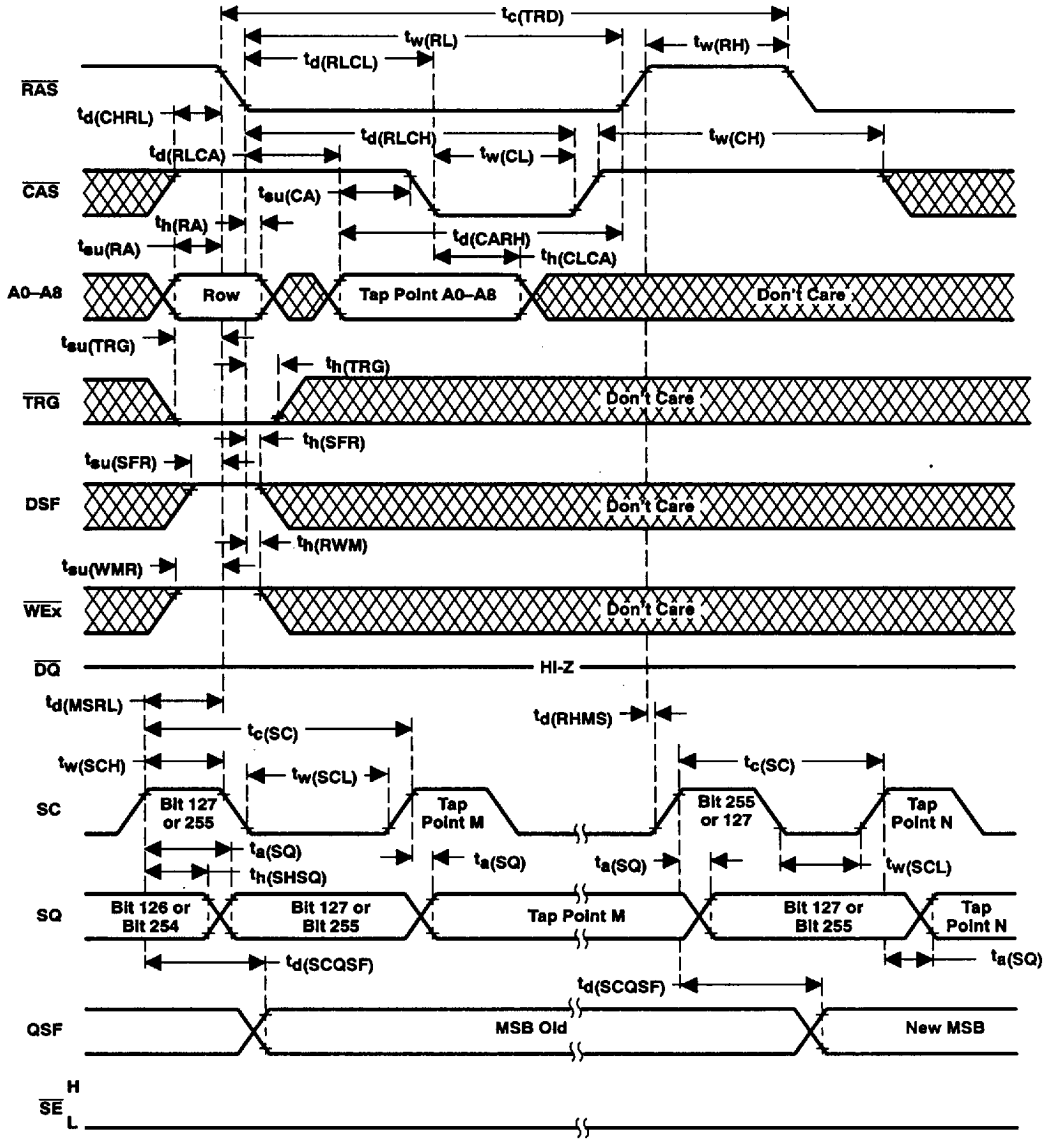
NOTES: A. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

B. Random mode (DQ outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

C. A0–A7: Register tap point, A8: which half of the transferred row.

Figure 38. Read Transfer Timing, Real-Time Reload Operation/Late Load Operation†

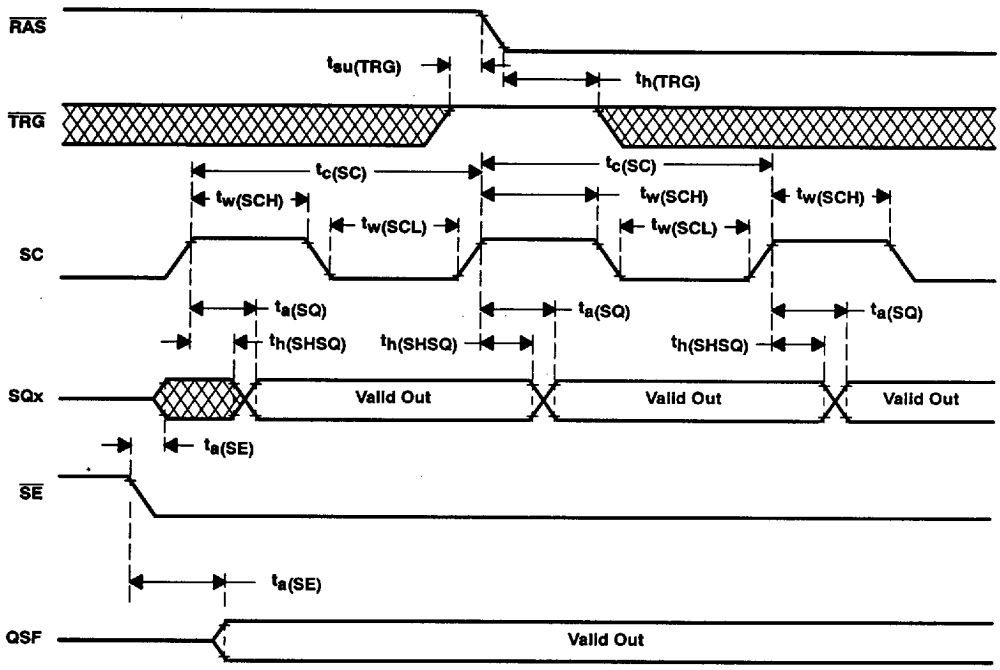
PARAMETER MEASUREMENT INFORMATION



NOTES: A. There is minimum requirement of one rising edge of SC clock between two split register transfer cycles.
B. A0–A6: Tap point of the given half, A7: Don't care, A8: DRAM row half.

Figure 39. Split-Register Read Transfer Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. While reading data through the serial data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register to memory to register data transfer operation.
B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle.

Figure 40. Serial Read Timing

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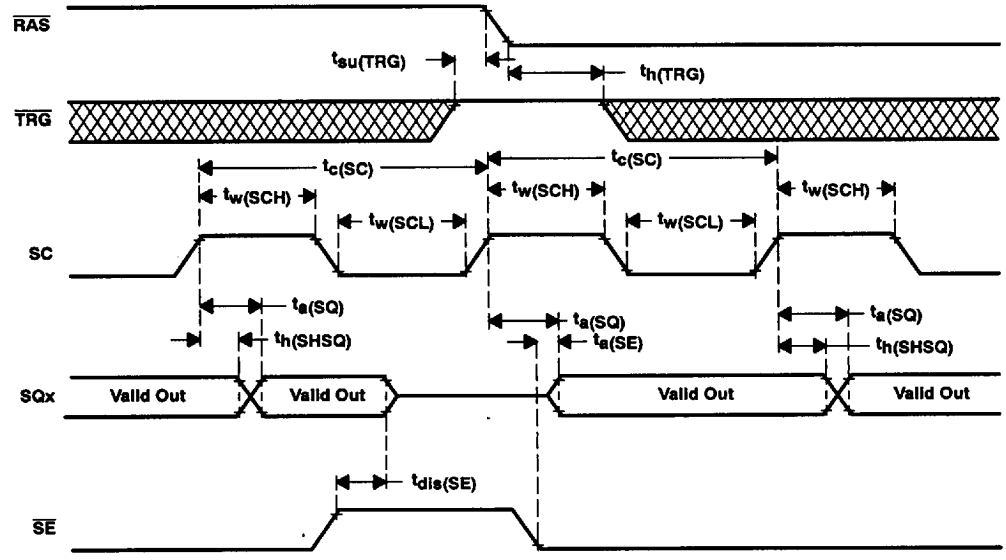
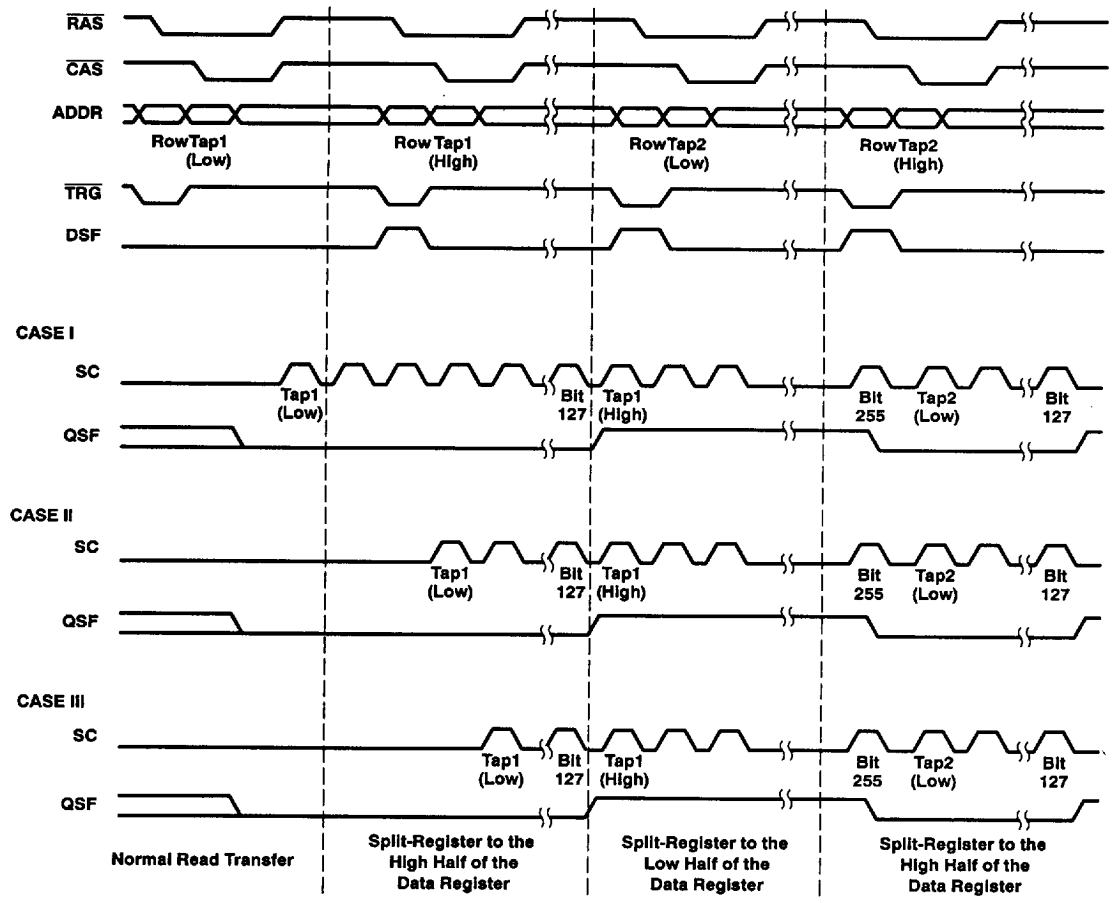


NOTES: A. While reading data through the serial data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register to memory to register data transfer operation.
B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle.

Figure 41. Serial Read Timing ($\overline{SE}$ Controlled Read)

OPERATING SEQUENCE INFORMATION



NOTES: A. In order to achieve proper split-register operation, a normal read transfer should be performed before the first split-register transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can then begin either after the normal read transfer cycle (CASE I), during the first split-register transfer cycle (CASE II), or even after the first split-register transfer cycle (CASE III). There is no minimum requirement of SC clock between the normal read transfer cycle and the first split-register cycle.

B. A split register transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 127 or 255) and the falling edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half. After the $t_{d(MSRL)}$ is met, the split-register transfer into the inactive half must also satisfy the minimum $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 127 or 255). There is a minimum requirement of one rising edge of SC clock between two split-register transfer cycles.

Figure 42. Split-Register Operating Sequence

device symbolization