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# KAI-16070

## 4864 (H) x 3232 (V) Interline CCD Image Sensor

### Description

The KAI-16070 Image Sensor is a 16-megapixel CCD in a 35 mm optical format. Based on the TRUESENSE 7.4 micron Interline Transfer CCD Platform, the sensor provides very high smear rejection and up to 82 dB linear dynamic range through the use of a unique dual-gain amplifier. Flexible readout architecture enables use of 1, 2, or 4 outputs for full resolution readout up to 8 frames per second, while a vertical overflow drain structure suppresses image blooming and enables electronic shuttering for precise exposure control.

The sensor is available with the TRUESENSE Sparse Color Filter Pattern, a technology which provides a 2x improvement in light sensitivity compared to a standard color Bayer part.

The sensor shares common pin-out and electrical configurations with a full family of ON Semiconductor Interline Transfer CCD image sensors, allowing a single camera design to be leveraged in support of multiple devices.

**Table 1. GENERAL SPECIFICATIONS**

| Parameter                   | Typical Value                                                          |
|-----------------------------|------------------------------------------------------------------------|
| Architecture                | Interline CCD; Progressive Scan                                        |
| Total Number of Pixels      | 4932 (H) x 3300 (V)                                                    |
| Number of Effective Pixels  | 4888 (H) x 3256 (V)                                                    |
| Number of Active Pixels     | 4864 (H) x 3232 (V) (15.7 M)                                           |
| Pixel Size                  | 7.4 $\mu\text{m}$ (H) x 7.4 $\mu\text{m}$ (V)                          |
| Active Image Size           | 36.0 mm (H) x 23.9 mm (V)<br>43.2 mm (diag.) 35 mm Optical Format      |
| Aspect Ratio                | 3:2                                                                    |
| Number of Outputs           | 1, 2, or 4                                                             |
| Charge Capacity             | 44,000 electrons                                                       |
| Output Sensitivity          | 9.7 $\mu\text{V}/\text{e}^-$ (low), 33 $\mu\text{V}/\text{e}^-$ (high) |
| Quantum Efficiency          |                                                                        |
| Mono (-AAA)                 | 10%                                                                    |
| Mono (-AXA, -PXA, -QXA)     | 48%                                                                    |
| R, G, B (-CXA)              | 32%, 41%, 39%                                                          |
| R, G, B (-FXA)              | 33%, 40%, 40%                                                          |
| Base ISO                    |                                                                        |
| -AXA                        | 350                                                                    |
| -CXA, -PXA                  | 130, 310 (respectively)                                                |
| -FXA, -PXA                  | 130, 310 (respectively)                                                |
| Read Noise (f = 40 MHz)     | 12 electrons rms                                                       |
| Dark Current                |                                                                        |
| Photodiode / VCCD           | 1 / 145 electrons/s                                                    |
| Dark Current Doubling Temp. |                                                                        |
| Photodiode / VCCD           | 7°C / 9°C                                                              |
| Dynamic Range               |                                                                        |
| High Gain Amp (40 MHz)      | 70 dB                                                                  |
| Dual Amp, 2x2 Bin (40 MHz)  | 82 dB                                                                  |
| Charge Transfer Efficiency  | 0.999999                                                               |
| Blooming Suppression        | > 1000 X                                                               |
| Smear                       | -115 dB                                                                |
| Image Lag                   | < 10 electrons                                                         |
| Maximum Pixel Clock Speed   | 40 MHz                                                                 |
| Maximum Frame Rates         |                                                                        |
| Quad / Dual / Single Output | 8 / 4 / 2 fps                                                          |
| Package                     | 72 pin PGA                                                             |
| Cover Glass                 | AR Coated, 2 Sides or Clear Glass                                      |

NOTE: All parameters are specified at T = 40°C unless otherwise noted.



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**Figure 1. KAI-16070 CCD Image Sensor**

### Features

- Superior Smear Rejection
- Up to 82 dB Linear Dynamic Range
- Bayer Color Pattern, TRUESENSE Sparse Color Filter Pattern, and Monochrome Configurations
- Progressive Scan & Flexible Readout Architecture
- High Frame Rate
- High Sensitivity – Low Noise Architecture
- Package Pin Reserved for Device Identification

### Applications

- Industrial Imaging and Inspection
- Traffic
- Aerial Photography

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# KAI-16070

## ORDERING INFORMATION

**Table 2. ORDERING INFORMATION**

| Part Number          | Description                                                                                                                                 | Marking Code                   |
|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| KAI-16070-AAA-JP-B1  | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Standard Grade                                                 | KAI-16070-AAA<br>Serial Number |
| KAI-16070-AAA-JP-AE  | Monochrome, No Microlens, PGA Package, Taped Clear Cover Serial Number Glass, no coatings, Engineering Grade                                |                                |
| KAI-16070-AXA-JD-B1  | Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 1                                  | KAI-16070-AXA<br>Serial Number |
| KAI-16070-AXA-JD-B2  | Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 2                                  |                                |
| KAI-16070-AXA-JD-AE  | Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade                        |                                |
| KAI-16070-FXA-JD-B1  | Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 1                      | KAI-16070-FXA<br>Serial Number |
| KAI-16070-FXA-JD-B2  | Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 2                      |                                |
| KAI-16070-FXA-JD-AE  | Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade            |                                |
| KAI-16070-QXA-JD-B1  | Gen2 Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 1           | KAI-16070-QXA<br>Serial Number |
| KAI-16070-QXA-JD-B2  | Gen2 Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 2           |                                |
| KAI-16070-QXA-JD-AE  | Gen2 Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade |                                |
| KAI-16070-CXA-JD-B1* | Gen1 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 1                      | KAI-16070-CXA<br>Serial Number |
| KAI-16070-CXA-JD-B2* | Gen1 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 2                      |                                |
| KAI-16070-CXA-JD-AE* | Gen1 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade            |                                |
| KAI-16070-PXA-JD-B1* | Gen1 Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 1           | KAI-16070-PXA<br>Serial Number |
| KAI-16070-PXA-JD-B2* | Gen1 Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 2           |                                |
| KAI-16070-PXA-JD-AE* | Gen1 Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade |                                |

\*Not recommended for new designs.

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at [www.onsemi.com](http://www.onsemi.com).



### ESD Protection

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and

power-down sequences may cause damage to the sensor. See Power-Up and Power-Down Sequence section.

### Bayer Color Filter Pattern

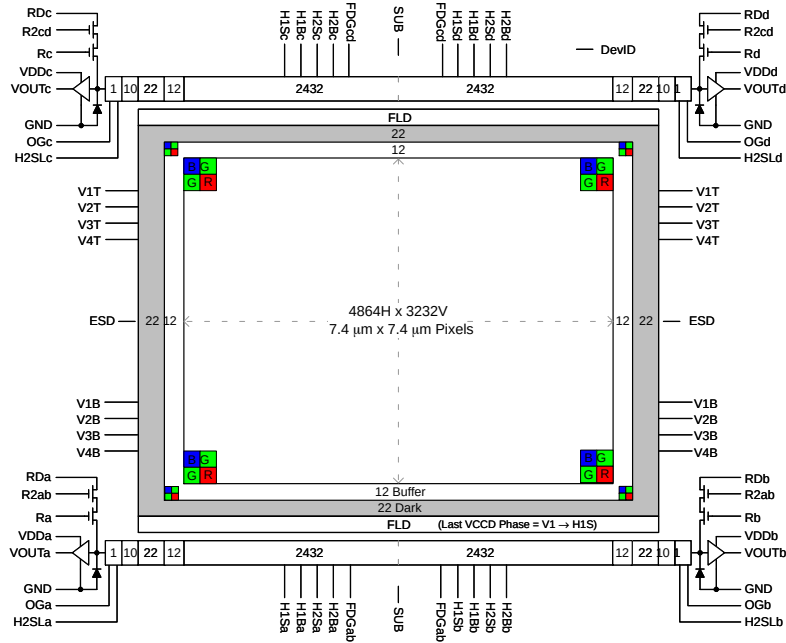


Figure 3. Bayer Color Filter Pattern

### TRUESENSE Sparse Color Filter Pattern

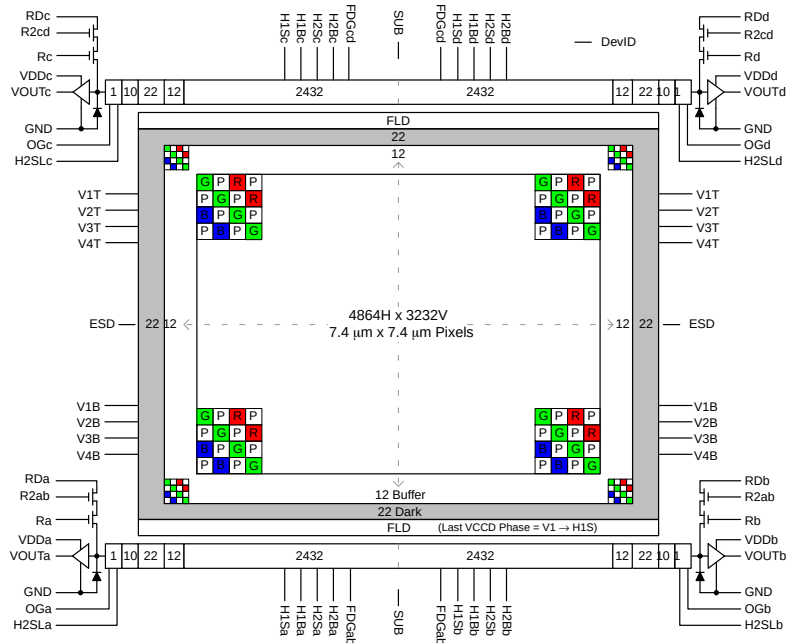


Figure 4. TRUESENSE Sparse Color Filter Pattern



Table 3. PIN DESCRIPTION

| Pin | Name  | Description                                                    |
|-----|-------|----------------------------------------------------------------|
| 1   | V3B   | Vertical CCD Clock, Phase 3, Bottom                            |
| [2] |       | [No Pin – Keyed]                                               |
| 3   | V1B   | Vertical CCD Clock, Phase 1, Bottom                            |
| 4   | V4B   | Vertical CCD Clock, Phase 4, Bottom                            |
| 5   | VDDa  | Output Amplifier Supply, Quadrant a                            |
| 6   | V2B   | Vertical CCD Clock, Phase 2, Bottom                            |
| 7   | GND   | Ground                                                         |
| 8   | VOUta | Video Output, Quadrant a                                       |
| 9   | Ra    | Reset Gate, Standard (High) Gain, Quadrant a                   |
| 10  | RDa   | Reset Drain, Quadrant a                                        |
| 11  | H2SLa | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a |
| 12  | OGa   | Output Gate, Quadrant a                                        |
| 13  | H1Ba  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant a             |
| 14  | H2Ba  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant a             |
| 15  | H2Sa  | Horizontal CCD Clock, Phase 2, Storage, Quadrant a             |
| 16  | H1Sa  | Horizontal CCD Clock, Phase 1, Storage, Quadrant a             |
| 17  | SUB   | Substrate                                                      |
| 18  | FDGab | Fast Line Dump Gate, Bottom                                    |
| 19  | R2ab  | Reset Gate, Low Gain, Quadrants a & b                          |
| 20  | FDGab | Fast Line Dump Gate, Bottom                                    |
| 21  | H2Sb  | Horizontal CCD Clock, Phase 2, Storage, Quadrant b             |
| 22  | H1Sb  | Horizontal CCD Clock, Phase 1, Storage, Quadrant b             |
| 23  | H1Bb  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant b             |
| 24  | H2Bb  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant b             |
| 25  | H2SLb | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant b |
| 26  | OGb   | Output Gate, Quadrant b                                        |
| 27  | Rb    | Reset Gate, Standard (High) Gain, Quadrant b                   |
| 28  | RDb   | Reset Drain, Quadrant b                                        |
| 29  | GND   | Ground                                                         |
| 30  | VOUtb | Video Output, Quadrant b                                       |
| 31  | VDDb  | Output Amplifier Supply, Quadrant b                            |
| 32  | V2B   | Vertical CCD Clock, Phase 2, Bottom                            |
| 33  | V1B   | Vertical CCD Clock, Phase 1, Bottom                            |
| 34  | V4B   | Vertical CCD Clock, Phase 4, Bottom                            |
| 35  | V3B   | Vertical CCD Clock, Phase 3, Bottom                            |
| 36  | ESD   | ESD Protection Disable                                         |

| Pin | Name  | Description                                                    |
|-----|-------|----------------------------------------------------------------|
| 72  | ESD   | ESD Protection Disable                                         |
| 71  | V3T   | Vertical CCD Clock, Phase 3, Top                               |
| 70  | V4T   | Vertical CCD Clock, Phase 4, Top                               |
| 69  | V1T   | Vertical CCD Clock, Phase 1, Top                               |
| 68  | V2T   | Vertical CCD Clock, Phase 2, Top                               |
| 67  | VDDc  | Output Amplifier Supply, Quadrant c                            |
| 66  | VOUtc | Video Output, Quadrant c                                       |
| 65  | GND   | Ground                                                         |
| 64  | RDc   | Reset Drain, Quadrant c                                        |
| 63  | Rc    | Reset Gate, Standard (High) Gain, Quadrant c                   |
| 62  | OGc   | Output Gate, Quadrant c                                        |
| 61  | H2SLc | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c |
| 60  | H2Bc  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant c             |
| 59  | H1Bc  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant c             |
| 58  | H1Sc  | Horizontal CCD Clock, Phase 1, Storage, Quadrant c             |
| 57  | H2Sc  | Horizontal CCD Clock, Phase 2, Storage, Quadrant c             |
| 56  | FDGcd | Fast Line Dump Gate, Top                                       |
| 55  | R2cd  | Reset Gate, Low Gain, Quadrants c & d                          |
| 54  | FDGcd | Fast Line Dump Gate, Top                                       |
| 53  | SUB   | Substrate                                                      |
| 52  | H1Sd  | Horizontal CCD Clock, Phase 1, Storage, Quadrant d             |
| 51  | H2Sd  | Horizontal CCD Clock, Phase 2, Storage, Quadrant d             |
| 50  | H2Bd  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant d             |
| 49  | H1Bd  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant d             |
| 48  | OGd   | Output Gate, Quadrant d                                        |
| 47  | H2SLd | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d |
| 46  | RDd   | Reset Drain, Quadrant d                                        |
| 45  | Rd    | Reset Gate, Standard (High) Gain, Quadrant d                   |
| 44  | VOUtd | Video Output, Quadrant d                                       |
| 43  | GND   | Ground                                                         |
| 42  | V2T   | Vertical CCD Clock, Phase 2, Top                               |
| 41  | VDDd  | Output Amplifier Supply, Quadrant d                            |
| 40  | V4T   | Vertical CCD Clock, Phase 4, Top                               |
| 39  | V1T   | Vertical CCD Clock, Phase 1, Top                               |
| 38  | DevID | Device Identification                                          |
| 37  | V3T   | Vertical CCD Clock, Phase 3, Top                               |

1. Liked named pins are internally connected and should have a common drive signal.

## IMAGING PERFORMANCE

**Table 4. TYPICAL OPERATION CONDITIONS**

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

| Description  | Condition                                       | Notes                                       |
|--------------|-------------------------------------------------|---------------------------------------------|
| Light Source | Continuous red, green and blue LED illumination | For monochrome sensor, only green LED used. |
| Operation    | Nominal operating voltages and timing           |                                             |

**Table 5. SPECIFICATIONS – ALL CONFIGURATIONS**

| Description                                                                                                                                                   | Symbol                     | Min.        | Nom.        | Max.        | Units              | Sam-<br>pling<br>Plan | Temperature<br>Tested At<br>(°C) | Notes |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-------------|-------------|-------------|--------------------|-----------------------|----------------------------------|-------|
| Dark Field Global Non-Uniformity                                                                                                                              | DSNU                       | –           | –           | 5           | mVpp               | Die                   | 27, 40                           |       |
| Bright Field Global Non-Uniformity                                                                                                                            |                            | –           | 2           | 12          | %rms               | Die                   | 27, 40                           | 1     |
| Bright Field Global Peak to Peak Non-Uniformity                                                                                                               | PRNU                       | –           | 10          | 30          | %pp                | Die                   | 27, 40                           | 1     |
| Bright Field Center Non-Uniformity                                                                                                                            |                            | –           | 1           | 2           | %rms               | Die                   | 27, 40                           | 1     |
| Maximum Photo-response Nonlinearity<br>High Gain (4,000 to 20,000 electrons)<br>High Gain (4,000 to 40,000 electrons)<br>Low Gain (8,000 to 80,000 electrons) | NL_HG1<br>NL_HG2<br>NL_LG1 | –<br>–<br>– | 2<br>3<br>6 | –<br>–<br>– | %                  | Design                |                                  | 2     |
| Maximum Gain Difference Between<br>Outputs                                                                                                                    | $\Delta G$                 | –           | 10          | –           | %                  | Design                |                                  | 2     |
| Horizontal CCD Charge Capacity                                                                                                                                | HNe                        | –           | 90          | –           | ke <sup>–</sup>    | Design                |                                  |       |
| Vertical CCD Charge Capacity                                                                                                                                  | VNe                        | –           | 60          | –           | ke <sup>–</sup>    | Design                |                                  |       |
| Photodiode Charge Capacity                                                                                                                                    | PNe                        | –           | 44          | –           | ke <sup>–</sup>    | Die                   | 27, 40                           | 3     |
| Floating Diffusion Capacity – High Gain                                                                                                                       | Fne_HG                     | 40          | –           | –           | ke <sup>–</sup>    | Die                   | 27, 40                           |       |
| Floating Diffusion Capacity – Low Gain                                                                                                                        | Fne_LG                     | 160         | –           | –           | ke <sup>–</sup>    | Die                   | 27, 40                           |       |
| Linear Saturation Level – High Gain                                                                                                                           | Lsat_HG                    | –           | 40          | –           | ke <sup>–</sup>    | Design                |                                  |       |
| Linear Saturation Level – Low Gain                                                                                                                            | Lsat_LG                    | –           | 160         | –           | ke <sup>–</sup>    | Design                |                                  |       |
| Horizontal CCD Charge Transfer<br>Efficiency                                                                                                                  | HCTE                       | 0.999995    | 0.999999    | –           |                    | Die                   |                                  |       |
| Vertical CCD Charge Transfer<br>Efficiency                                                                                                                    | VCTE                       | 0.999995    | 0.999999    | –           |                    | Die                   |                                  |       |
| Photodiode Dark Current                                                                                                                                       | l <sub>pd</sub>            | –           | 2           | 70          | e/p/s              | Die                   | 40                               |       |
| Vertical CCD Dark Current                                                                                                                                     | l <sub>vd</sub>            | –           | 200         | 600         | e/p/s              | Die                   | 40                               |       |
| Image Lag                                                                                                                                                     | Lag                        | –           | –           | 10          | e <sup>–</sup>     | Design                |                                  |       |
| Antiblooming Factor                                                                                                                                           | Xab                        | 1000        | –           | –           |                    | Design                |                                  |       |
| Vertical Smear                                                                                                                                                | S <sub>mr</sub>            | –           | –115        | –           | dB                 | Design                |                                  |       |
| Read Noise (High Gain / Low Gain)                                                                                                                             | n <sub>e-T</sub>           | –           | 12 / 45     | –           | e <sup>–</sup> rms | Design                |                                  | 4     |
| Dynamic Range, Standard                                                                                                                                       | DR                         | –           | 70.5        | –           | dB                 | Design                |                                  | 4, 5  |
| Dynamic Range, Extended Linear<br>Dynamic Range Mode (XLDR)                                                                                                   | XLDR                       | –           | 82.5        | –           | dB                 | Design                |                                  | 4, 5  |
| Output Amplifier DC Offset                                                                                                                                    | V <sub>odc</sub>           | 5           | 9.0         | 14          | V                  | Die                   | 27, 40                           |       |
| Output Amplifier Bandwidth                                                                                                                                    | f <sub>–3db</sub>          | –           | 250         | –           | MHz                | Design                |                                  | 6     |
| Output Amplifier Impedance                                                                                                                                    | R <sub>OUT</sub>           | 100         | 127         | 200         | Ω                  | Die                   | 27, 40                           |       |
| Output Amplifier Sensitivity<br>High Gain<br>Low Gain                                                                                                         | $\Delta V/\Delta N$        | –<br>–      | 33<br>9.7   | –<br>–      | μV/e <sup>–</sup>  | Design                |                                  |       |

1. Per color
2. Value is over the range of 10% to 90% of photodiode saturation.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is 1450 mV. This value is determined while operating the device in the low gain mode. VAB level assigned is valid for both modes; high gain or low gain.
4. At 40 MHz
5. Uses 20LOG (PNe/ n<sub>e-T</sub>)
6. Assumes 5 pF load.



# KAI-16070

**Table 6. KAI-16070-AAA CONFIGURATION WITH NO GLASS**

| Description                        | Symbol            | Min. | Nom. | Max. | Units | Sampling Plan | Temperature Tested At (°C) | Notes |
|------------------------------------|-------------------|------|------|------|-------|---------------|----------------------------|-------|
| Peak Quantum Efficiency            | QE <sub>max</sub> | –    | 10   | –    | %     | Design        |                            | 1     |
| Peak Quantum Efficiency Wavelength | λ <sub>QE</sub>   | –    | 500  | –    | nm    | Design        |                            | 1     |

1. Measurement taken without cover glass.

**Table 7. KAI-16070-AXA, KAI-16070-PXA, AND KAI-16070-QXA CONFIGURATIONS**

| Description                        | Symbol            | Min. | Nom. | Max. | Units | Sampling Plan | Temperature Tested At (°C) | Notes |
|------------------------------------|-------------------|------|------|------|-------|---------------|----------------------------|-------|
| Peak Quantum Efficiency            | QE <sub>max</sub> | –    | 48   | –    | %     | Design        |                            |       |
| Peak Quantum Efficiency Wavelength | λ <sub>QE</sub>   | –    | 500  | –    | nm    | Design        |                            |       |

1. This color filter set configuration (Gen1) is not recommended for new designs.

**Table 8. KAI-16070-FXA AND KAI-16070-QXA GEN2 COLOR CONFIGURATIONS WITH MAR GLASS**

| Description                        |                      | Symbol            | Min. | Nom.              | Max. | Units | Sampling Plan | Temperature Tested At (°C) | Notes |
|------------------------------------|----------------------|-------------------|------|-------------------|------|-------|---------------|----------------------------|-------|
| Peak Quantum Efficiency            | Blue<br>Green<br>Red | QE <sub>max</sub> | –    | 40<br>40<br>34    | –    | %     | Design        |                            |       |
| Peak Quantum Efficiency Wavelength | Blue<br>Green<br>Red | λ <sub>QE</sub>   | –    | 460<br>535<br>605 | –    | nm    | Design        |                            |       |

**Table 9. KAI-16070-CXA AND KAI-16070-PXA GEN1 COLOR CONFIGURATIONS WITH MAR GLASS**

| Description                        |                      | Symbol            | Min. | Nom.              | Max. | Units | Sampling Plan | Temperature Tested At (°C) | Notes |
|------------------------------------|----------------------|-------------------|------|-------------------|------|-------|---------------|----------------------------|-------|
| Peak Quantum Efficiency            | Blue<br>Green<br>Red | QE <sub>max</sub> | –    | 39<br>41<br>32    | –    | %     | Design        |                            | 1     |
| Peak Quantum Efficiency Wavelength | Blue<br>Green<br>Red | λ <sub>QE</sub>   | –    | 470<br>540<br>620 | –    | nm    | Design        |                            | 1     |

1. This color filter set configuration (Gen1) is not recommended for new designs.

Linear Signal Range

High Gain

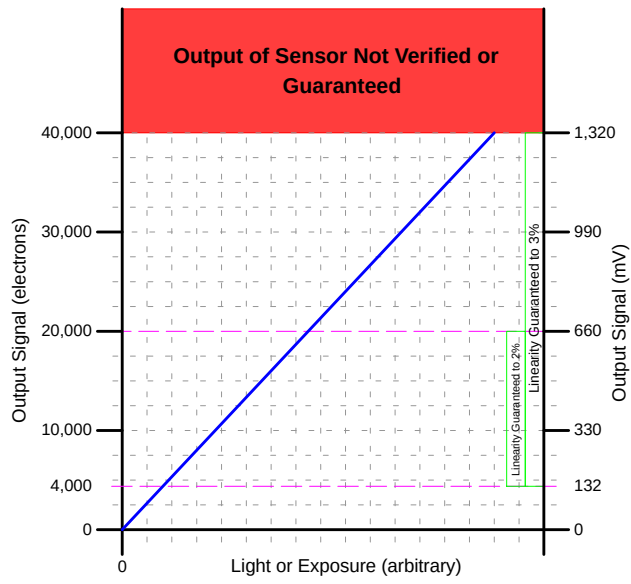


Figure 6. High Gain Linear Signal Range

Low Gain

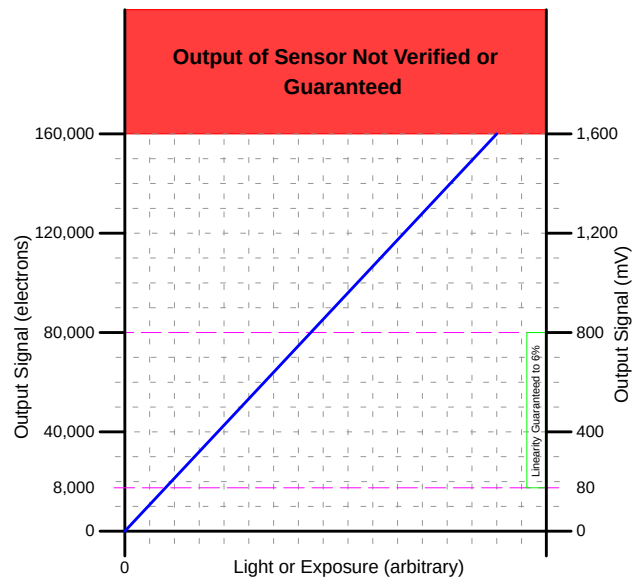


Figure 7. Low Gain Linear Signal Range

## TYPICAL PERFORMANCE CURVES

### Quantum Efficiency

Monochrome without Microlens

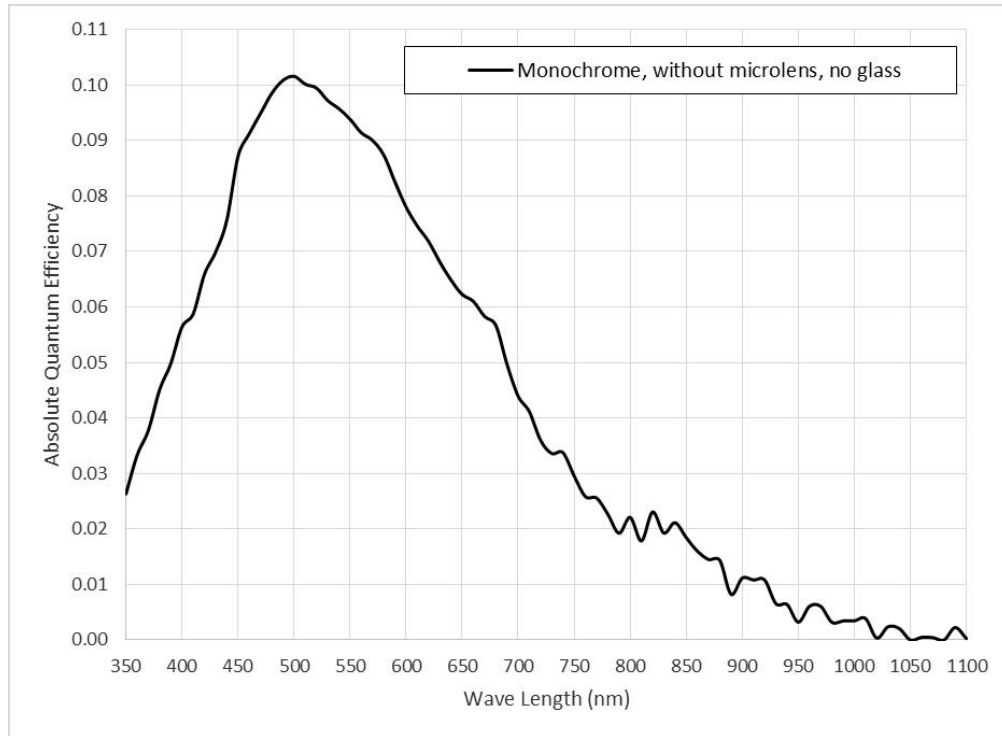


Figure 8. Monochrome without Microlens Quantum Efficiency

Monochrome with Microlens

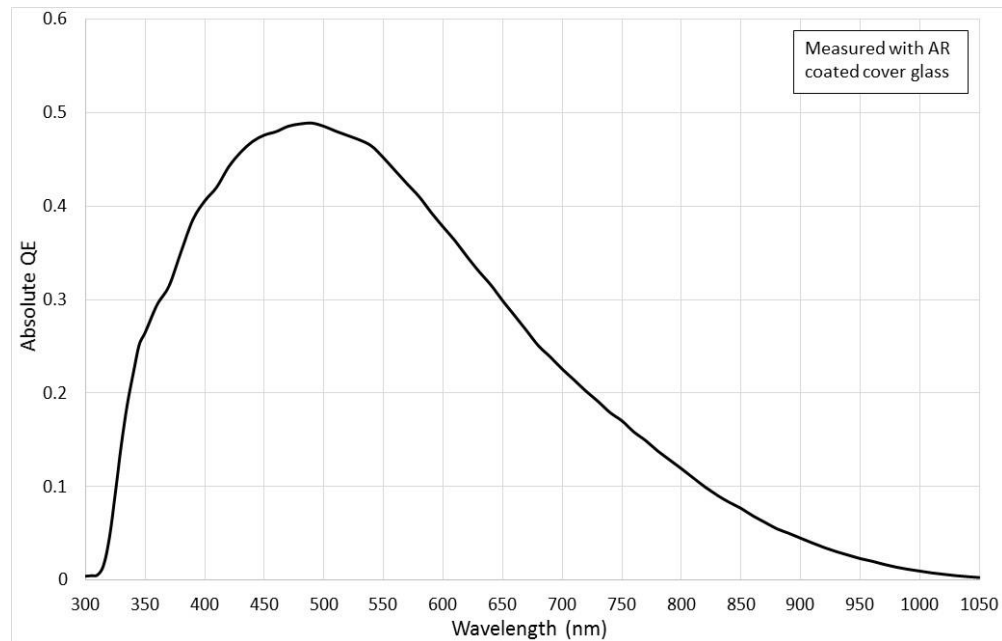


Figure 9. Monochrome with Microlens Quantum Efficiency

Color (Bayer RGB) with Microlens (Gen2 and Gen1 CFA)

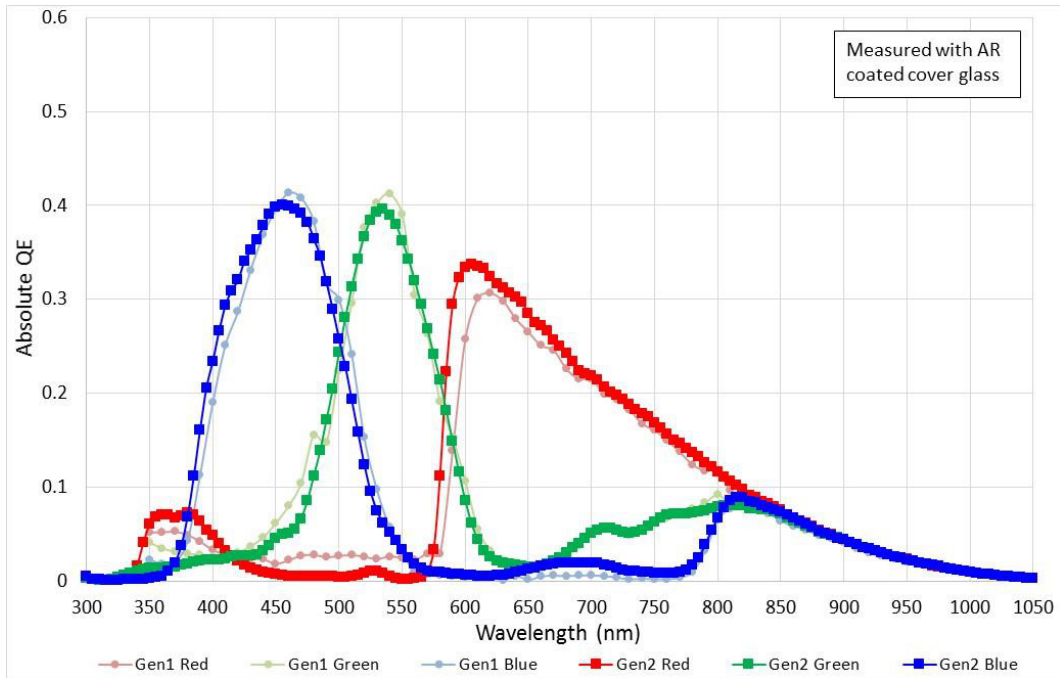


Figure 10. Color (Bayer) with Microlens Quantum Efficiency

Color (TRUESENSE Sparse CFA) with Microlens (Gen2 and Gen1 CFA)

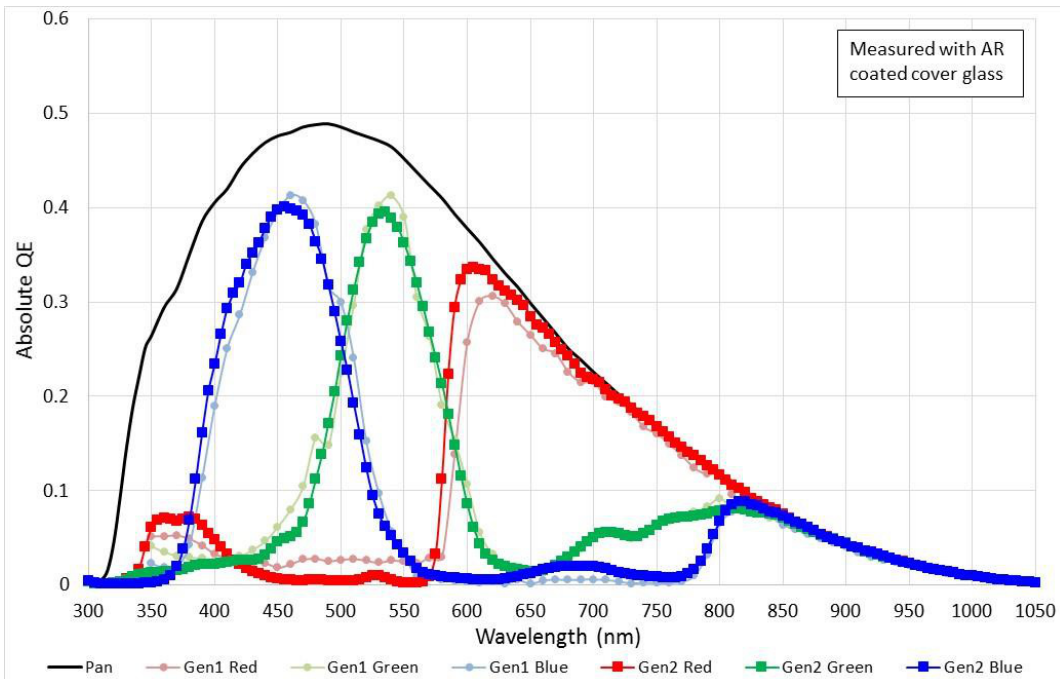


Figure 11. Color (TRUESENSE Sparse CFA) with Microlens Quantum Efficiency

### Angular Quantum Efficiency

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.

For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

### Monochrome with Microlens

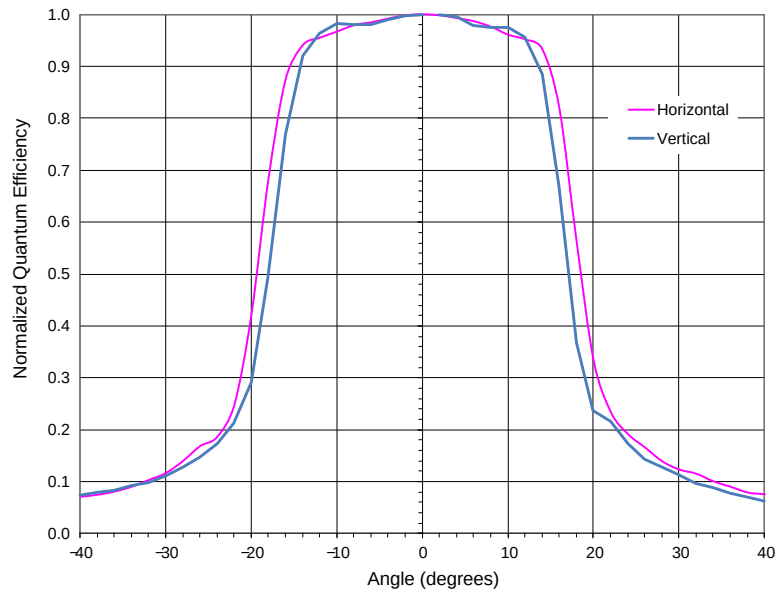


Figure 12. Monochrome with Microlens Angular Quantum Efficiency

### Dark Current versus Temperature

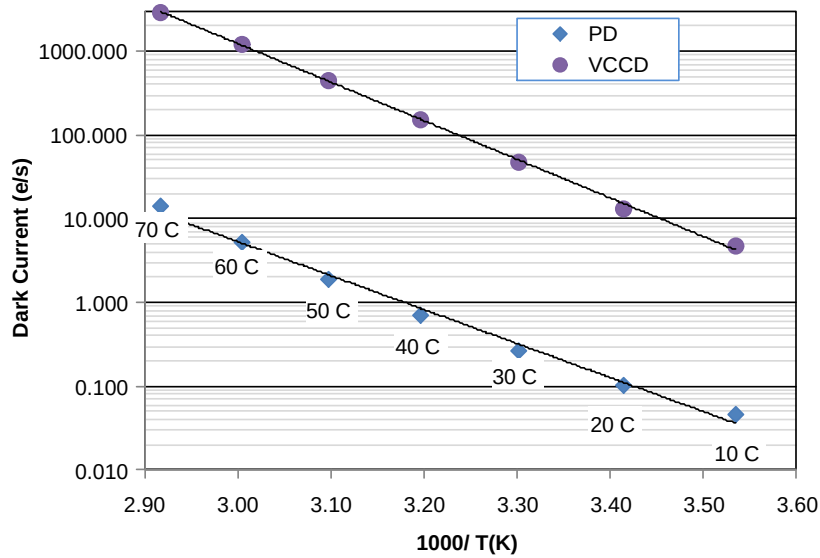


Figure 13. Dark Current versus Temperature

Power – Estimated

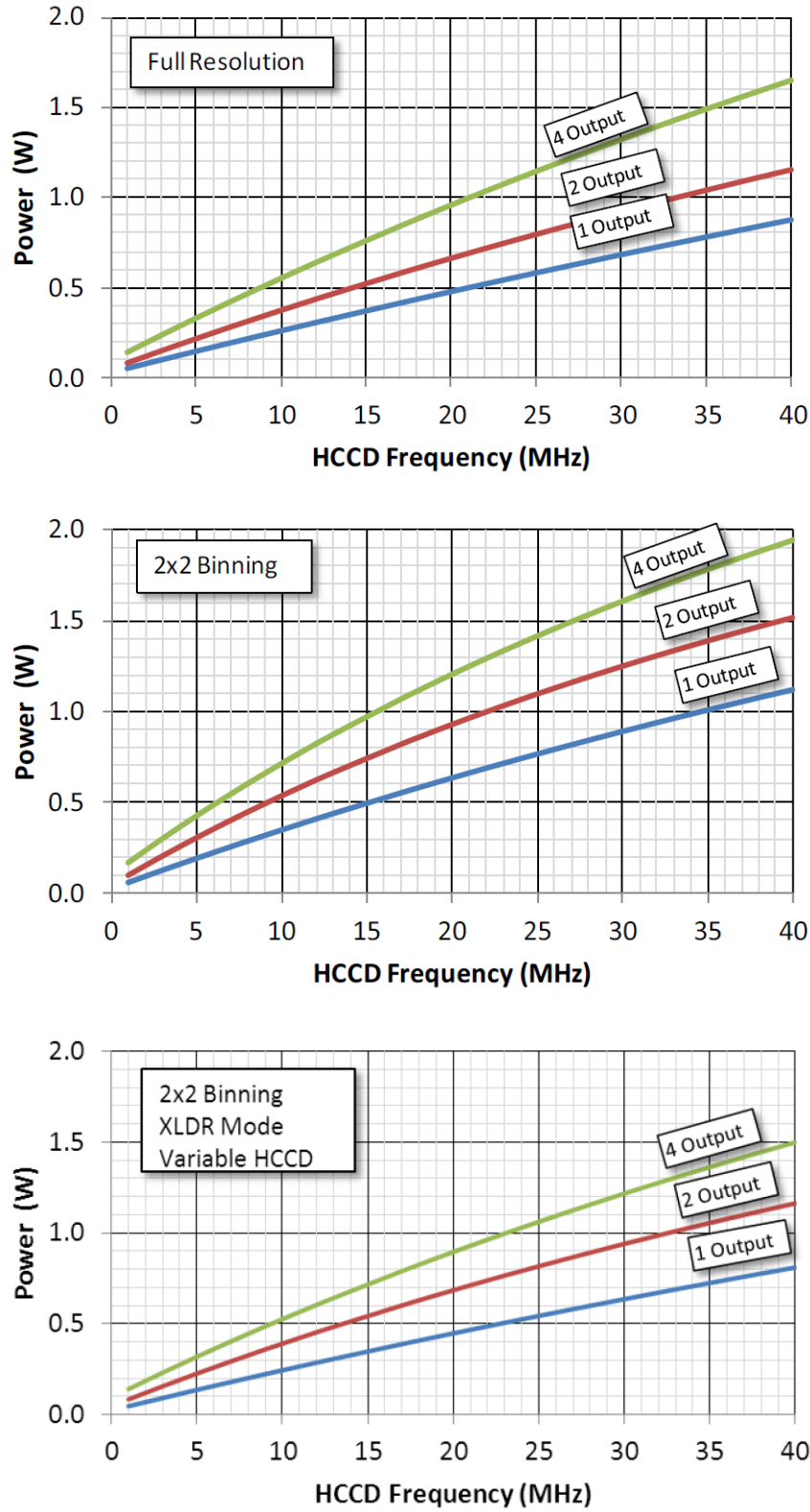


Figure 14. Power

Frame Rates

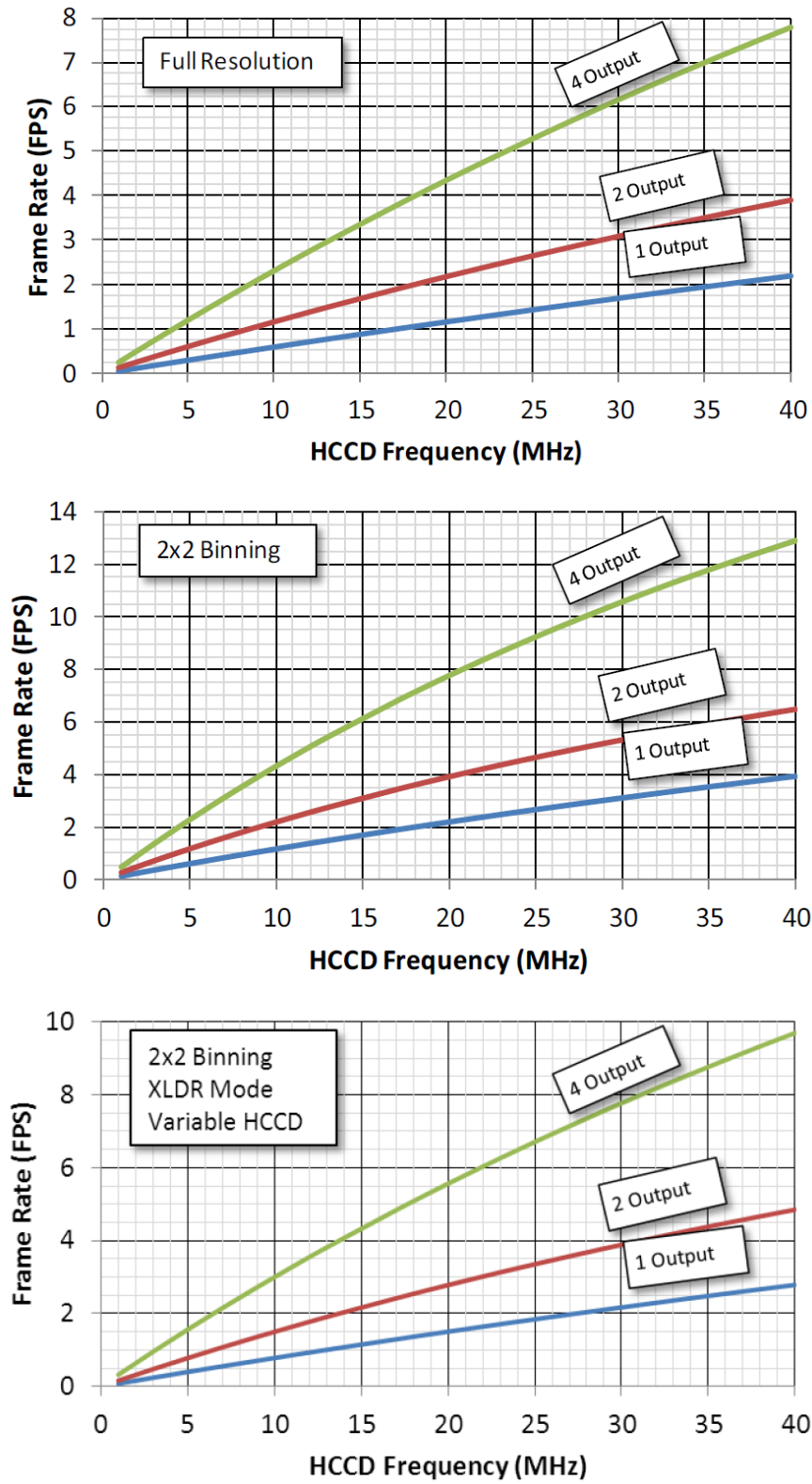


Figure 15. Frame Rates

## DEFECT DEFINITIONS

Table 10. OPERATION CONDITIONS FOR DEFECT TESTING AT 40°C

| Description                 | Condition                                                   | Notes |
|-----------------------------|-------------------------------------------------------------|-------|
| Operational Mode            | One output using VOUTa, continuous readout                  |       |
| HCCD Clock Frequency        | 20 MHz                                                      |       |
| Pixels Per Line             | 5000                                                        | 1     |
| Lines Per Frame             | 3354                                                        | 2     |
| Line Time                   | 266 $\mu$ sec                                               |       |
| Frame Time                  | 894 msec                                                    |       |
| Photodiode Integration Time | PD_Tint = Frame Time = 894 msec, no electronic shutter used |       |
| Temperature                 | 40°C                                                        |       |
| Light Source                | Continuous red, green and blue LED illumination             | 3     |
| Operation                   | Nominal operating voltages and timing                       |       |

1. Horizontal overclocking used.
2. Vertical overclocking used.
3. For monochrome sensor, only the green LED is used.

Table 11. DEFECT DEFINITIONS FOR TESTING AT 40°C

| Description                             | Definition                                                                                              | Grade 1 | Grade 2 Mono | Grade 2 Color | Notes |
|-----------------------------------------|---------------------------------------------------------------------------------------------------------|---------|--------------|---------------|-------|
| Major dark field defective bright pixel | PD_Tint = Frame Time; Defect $\geq$ 325 mV                                                              | 150     | 300          | 300           | 1     |
| Major bright field defective dark pixel | Defect $\geq$ 15%                                                                                       |         |              |               |       |
| Minor dark field defective bright pixel | PD_Tint = Frame Time; Defect $\geq$ 163 mV                                                              | 1500    | 3000         | 3000          |       |
| Cluster defect                          | A group of 2 to 19 contiguous major defective pixels, but no more than 4 adjacent defects horizontally. | 30      | 30           | 30            | 2     |
| Column defect                           | A group of more than 10 contiguous major defective pixels along a single column                         | 0       | 4            | 15            | 2     |

1. For the color devices (KAI-16070-FXA, KAI-16070-QXA, KAI-16070-CXA, and KAI-16070-PXA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).
3. Tested at 40°C with no electronic shutter used.



**Table 12. OPERATION CONDITIONS FOR DEFECT TESTING AT 27°C**

| Description                           | Condition                                                   | Notes |
|---------------------------------------|-------------------------------------------------------------|-------|
| Operational Mode                      | Two outputs, using VOUTa and VOUTc, continuous readout      |       |
| HCCD Clock Frequency                  | 20 MHz                                                      |       |
| Pixels Per Line                       | 5000                                                        | 1     |
| Lines Per Frame                       | 3354                                                        | 2     |
| Line Time                             | 266 $\mu$ sec                                               |       |
| Frame Time                            | 894 msec                                                    |       |
| Photodiode Integration Time (PD_Tint) | PD_Tint = Frame Time = 894 msec, no electronic shutter used |       |
| Temperature                           | 27°C                                                        |       |
| Light Source                          | Continuous red, green and blue LED illumination             | 3     |
| Operation                             | Nominal operating voltages and timing                       |       |

1. Horizontal overclocking used.
2. Vertical overclocking used.
3. For monochrome sensor, only the green LED is used.

**Table 13. DEFECT DEFINITIONS FOR TESTING AT 27°C**

| Description                             | Definition                                                                                              | Grade 1 | Grade 2 Mono | Grade 2 Color | Notes |
|-----------------------------------------|---------------------------------------------------------------------------------------------------------|---------|--------------|---------------|-------|
| Major dark field defective bright pixel | PD_Tint = Frame Time $\rightarrow$ Defect $\geq$ 100 mV                                                 | 150     | 300          | 300           | 1     |
| Major bright field defective dark pixel | Defect $\geq$ 15%                                                                                       |         |              |               |       |
| Minor dark field defective bright pixel | PD_Tint = Frame Time; Defect $\geq$ 52 mV                                                               | 1500    | 3000         | 3000          |       |
| Cluster defect                          | A group of 2 to 19 contiguous major defective pixels, but no more than 4 adjacent defects horizontally. | 30      | 30           | 30            | 2     |
| Column defect                           | A group of more than 10 contiguous major defective pixels along a single column                         | 0       | 4            | 15            | 2     |

1. For the color devices (KAI-16070-FXA, KAI-16070-QXA, KAI-16070-CXA, and KAI-16070-PXA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).
3. Tested at 27°C with no electronic shutter used.
4. Defectivity levels for a unit with the Taped Cover Glass configuration (non-sealed cover glass) of this device cannot be guaranteed after final testing at the factory. Image sensors are tested for defects and are mapped prior to shipment. Additional pixel defects and clusters may appear for devices purchased without a sealed cover glass.

### Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point

defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps. See Figure 16: Regions of interest for the location of pixel 1,1.

## TEST DEFINITIONS

### Test Regions of Interest

Image Area ROI: Pixel (1, 1) to Pixel (4888, 3256)  
 Active Area ROI: Pixel (13, 13) to Pixel (4876, 3244)  
 Center ROI: Pixel (2345, 1527) to Pixel (2444, 1628)  
 Only the Active Area ROI pixels are used for performance and defect tests.

### Overclocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions.

See Figure 16 for a pictorial representation of the regions of interest.

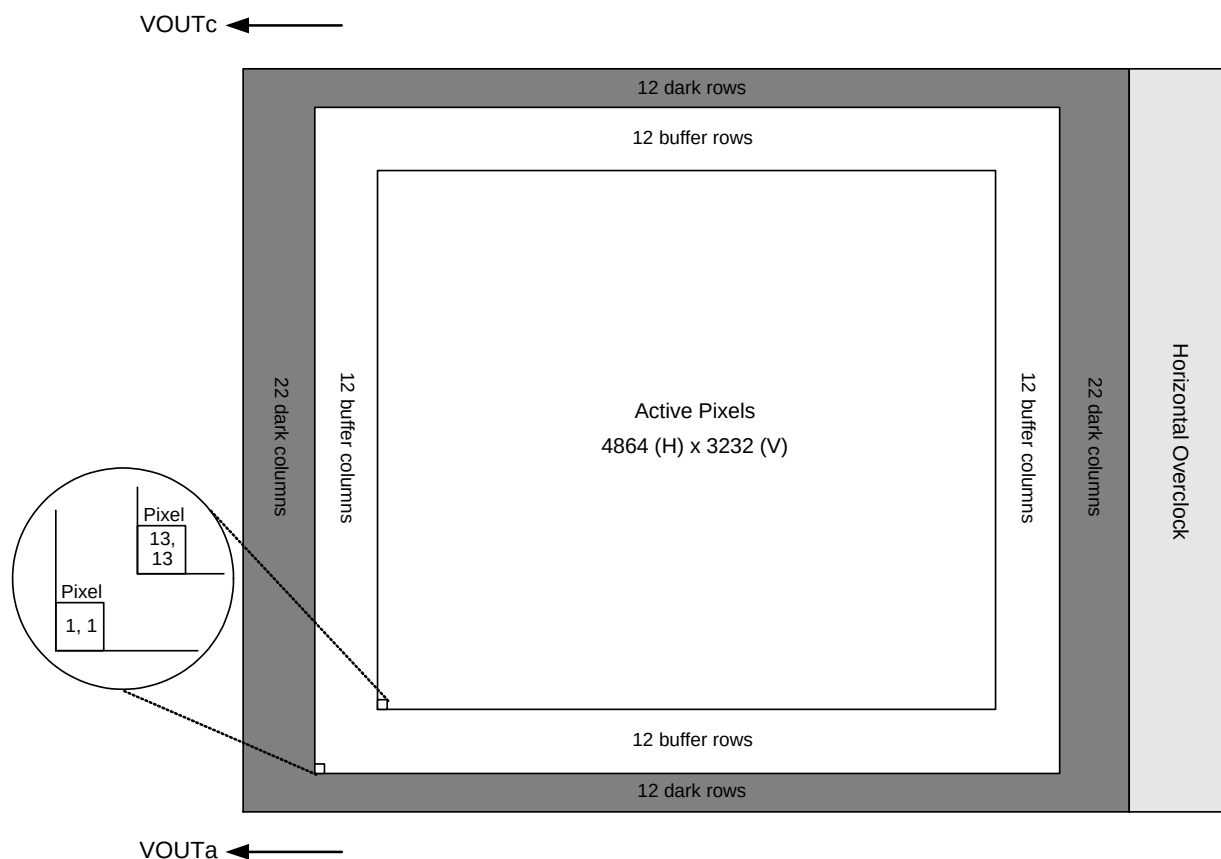


Figure 16. Regions of Interest

## Tests

### Dark Field Global Non-Uniformity

This test is performed under dark field conditions. The sensor is partitioned into 1 mm x 1 mm sub regions, each of which is 135 by 135 pixels in size. The average signal level of each of the sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in counts – Horizontal overlock average in counts) \* mV per count

Where i = 1 to total # of sub regions. During this calculation on the sub regions of interest, the maximum and

$$\text{GlobalNon-Uniformity} = 100 \times \left( \frac{\text{ActiveAreaStandardDeviation}}{\text{ActiveAreaSignal}} \right)$$

Units: %rms.

Active Area Signal = Active Area Average – Dark Column Average

### Global Peak to Peak Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1320 mV. The sensor is partitioned into sub regions of interest, each of which is 135 by 135

$$\text{GlobalUniformity} = 100 \times \frac{\text{MaximumSignal} - \text{MinimumSignal}}{\text{ActiveAreaSignal}}$$

Units: %pp

### Center Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed

$$\text{Center ROI Uniformity} = 100 \times \left( \frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}} \right)$$

Units: %rms.

Center ROI Signal = Center ROI Average – Dark Column Average

### Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 1 mm x 1 mm sub regions, each of which is 135 by 135 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the “Defect Definitions” section.

### Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at approximately 924 mV. Prior

minimum signal levels are found. The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

Units: mVpp (millivolts peak to peak)

### Global Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1320 mV. Global non-uniformity is defined as

pixels in size. The average signal level of each of the before mentioned sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in counts – Horizontal overlock average in counts) \* mV per count

Where i = 1 to total # of sub regions. During this calculation on the sub regions of interest, the maximum and minimum signal levels are found. The global peak to peak uniformity is then calculated as:

the substrate voltage has been set such that the charge capacity of the sensor is 1320 mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels of the sensor. Center uniformity is defined as:

to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1320 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal \* threshold  
Bright defect threshold = Active Area Signal \* threshold

The sensor is then partitioned into 1 mm x 1 mm sub regions of interest, each of which is 135 by 135 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 924 mV
- Dark defect threshold:  $924 \text{ mV} * 15\% = 138 \text{ mV}$
- Bright defect threshold:  $924 \text{ mV} * 15\% = 138 \text{ mV}$
- Region of interest #1 selected. This region of interest is pixels 13, 13 to pixels 147, 147.
  - ◆ Median of this region of interest is found to be 918 mV.
  - ◆ Any pixel in this region of interest that is  $\geq (918 + 138 \text{ mV})$  1062 mV in intensity will be marked defective.
  - ◆ Any pixel in this region of interest that is  $\leq (918 - 138 \text{ mV})$  780 mV in intensity will be marked defective.
- All remaining sub regions of interest are analyzed for defective pixels in the same manner. Any remaining factor of pixels less than 135 pixels that are not covered by this moving ROI is placed over the remaining pixels at the active area boundary. A portion of pixels that were tested in the previous ROI will be retested to keep the test ROI at a full 135 by 135 pixels.

## OPERATION

Table 14. ABSOLUTE MAXIMUM RATINGS

| Description           | Symbol           | Minimum | Maximum | Units | Notes |
|-----------------------|------------------|---------|---------|-------|-------|
| Operating Temperature | T <sub>OP</sub>  | -50     | +70     | °C    | 1     |
| Humidity              | RH               | +5      | +90     | %     | 2     |
| Output Bias Current   | I <sub>out</sub> |         | 60      | mA    | 3     |
| Off-chip Load         | C <sub>L</sub>   |         | 10      | pF    |       |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Noise performance will degrade at higher temperatures.
- T = 25°C. Excessive humidity will degrade MTTF.
- Total for all outputs. Maximum current is -15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

Table 15. ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND

| Description                                                                                          | Minimum   | Maximum    | Units | Notes |
|------------------------------------------------------------------------------------------------------|-----------|------------|-------|-------|
| VDD $\alpha$ , VOUT $\alpha$                                                                         | -0.4      | 17.5       | V     | 1     |
| RD $\alpha$                                                                                          | -0.4      | 15.5       | V     | 1     |
| V1B, V1T                                                                                             | ESD - 0.4 | ESD + 24.0 | V     |       |
| V2B, V2T, V3B, V3T, V4B, V4T                                                                         | ESD - 0.4 | ESD + 14.0 | V     |       |
| FDG $\alpha$ b, FDG $\alpha$ d                                                                       | ESD - 0.4 | ESD + 14.0 | V     |       |
| H1S $\alpha$ , H1B $\alpha$ , H2S $\alpha$ , H2B $\alpha$ , H2SL $\alpha$ , R $\alpha$ , OG $\alpha$ | ESD - 0.4 | ESD + 14.0 | V     | 1     |
| ESD                                                                                                  | -10.0     | 0.0        | V     |       |
| SUB                                                                                                  | -0.4      | +40.0      | V     | 2     |

- $\alpha$  denotes a, b, c or d
- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

## KAI-29050 Compatibility

The KAI-16070 is pin-for-pin compatible with a camera designed for the KAI-29050 image sensor with the following accommodations:

- To operate in accordance with a system designed for KAI-29050, the target substrate voltage should be set to be 2.0 V higher than the value recorded on the KAI-16070 shipping container. This setting will cause the charge capacity to be limited to 20 Ke<sup>-</sup> (or 660 mV).
- On the KAI-16070, pins 19 (R2ab) and 55 (R2cd) should be left floating per the KAI-29050 Device Performance Specification.
- The KAI-16070 will operate in only the high gain mode (33  $\mu$ V/e).
- All timing and voltages are taken from the KAI-29050 specification sheet.

- The number of horizontal and vertical CCD clock cycles is reduced as appropriate.
- In addition, if the intent is to operate the KAI-16070 image sensor in a camera designed for the KAI-29050 sensor that has been modified to accept and process the full 40,000 e<sup>-</sup> (1,320 mV) output, the following changes to the following voltage bias must be made:

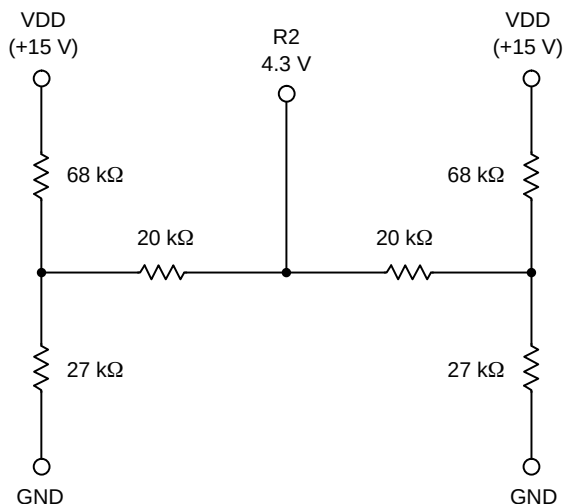
| Voltage Bias Differences | KAI-29050                    | KAI-16070                     |
|--------------------------|------------------------------|-------------------------------|
| Pins 10, 28, 46, and 64  | 12.0 V per the specification | Increase this value to 12.6 V |

NOTE: To make use of the low gain mode or dual gain mode the KAI-16070 voltages and timing specification must be used.

**Reset Pin, Low Gain (R2ab and R2cd)**

The R2ab and R2bc (pins 19 and 55) each have an internal circuit to bias the pins to 4.3 V. This feature assures the device is set to operate in the high gain mode when pins 19

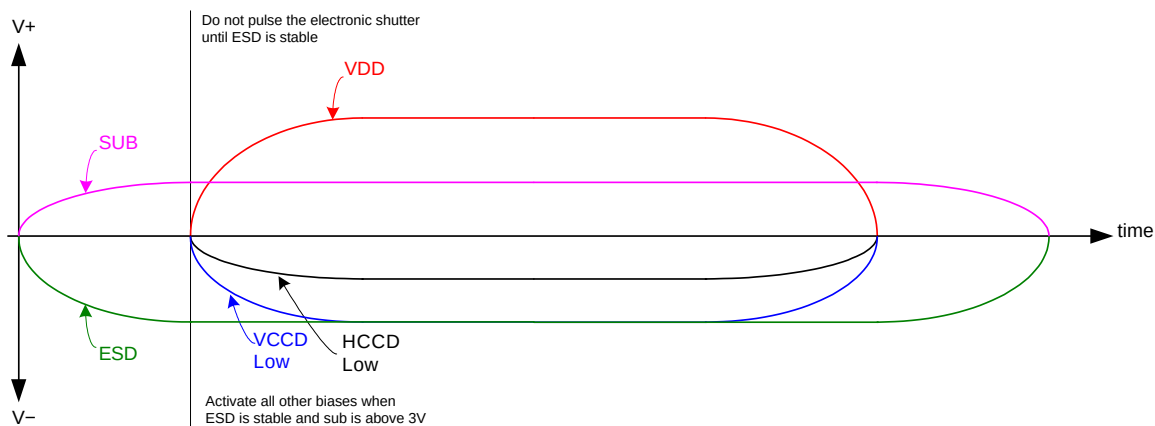
and 55 are not connected in the application to a clock driver (for KAI-29050 compatibility). Typical capacitor coupled drivers will not drive this structure.



**Figure 17. Equivalent Circuit for Reset Gate, Low Gain (R2ab and R2cd)**

### Power-Up and Power-Down Sequence

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor.

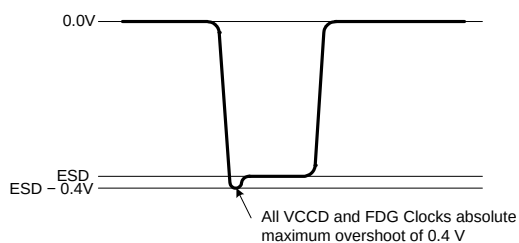


**Figure 18. Power-Up and Power-Down Sequence**

Notes:

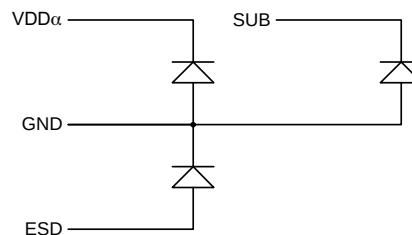
7. Activate all other biases when ESD is stable and SUB is above 3 V
8. Do not pulse the electronic shutter until ESD is stable
9. VDD cannot be +15 V when SUB is 0 V
10. The image sensor can be protected from an accidental improper ESD voltage by current limiting the SUB current to less than 10 mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect the sensor from accidental overshoots of SUB, VDD and ESD during power on and power off. See the figure below.

The VCCD clock waveform must not have a negative overshoot more than 0.4 V below the ESD voltage.



**Figure 19.**

Example of external diode protection for SUB, VDD and ESD.  $\alpha$  denotes a, b, c or d



**Figure 20.**

Table 16. DC BIAS OPERATING CONDITIONS

| Description             | Pins         | Symbol           | Minimum | Nominal | Maximum          | Units | Maximum DC Current | Notes    |
|-------------------------|--------------|------------------|---------|---------|------------------|-------|--------------------|----------|
| Reset Drain             | RD $\alpha$  | RD               | +12.4   | +12.6   | +12.8            | V     | 10 $\mu$ A         | 1, 9     |
| Output Gate             | OG $\alpha$  | OG               | -2.2    | -2.0    | -1.8             | V     | 10 $\mu$ A         | 1        |
| Output Amplifier Supply | VDD $\alpha$ | VDD              | +14.5   | +15.0   | +15.5            | V     | 11.0 mA            | 1,2      |
| Ground                  | GND          | GND              | 0.0     | 0.0     | 0.0              | V     | -1.0 mA            |          |
| Substrate               | SUB          | VSUB             | +5.0    | VAB     | VDD              | V     | 50 $\mu$ A         | 3, 8     |
| ESD Protection Disable  | ESD          | ESD              | -9.5    | -9.0    | V <sub>x_L</sub> | V     | 50 $\mu$ A         | 6, 7, 10 |
| Output Bias Current     | VOU $\alpha$ | I <sub>out</sub> | -3.0    | -5.0    | -10.0            | mA    |                    | 1, 4, 5  |

1.  $\alpha$  denotes a, b, c or d
2. The maximum DC current is for one output. I<sub>dd</sub> = I<sub>out</sub> + I<sub>ss</sub>. See Figure 21.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is the nominal PNe (see Specifications).
4. An output load sink must be applied to each VOUT pin to activate each output amplifier.
5. Nominal value required for 40 MHz operation per output. May be reduced for slower data rates and lower noise.
6. Adherence to the power-up and power-down sequence is critical. See Power-Up and Power-Down Sequence section.
7. ESD maximum value must be less than or equal to V1\_L + 0.4 V and V2\_L + 0.4 V
8. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*
9. 12.0 V may be used if the total output signal desired is 20,000 e<sup>-</sup> or less.
10. Where V<sub>x\_L</sub> is the level set for V1\_L, V2\_L, V3\_L, or V4\_L in the application.

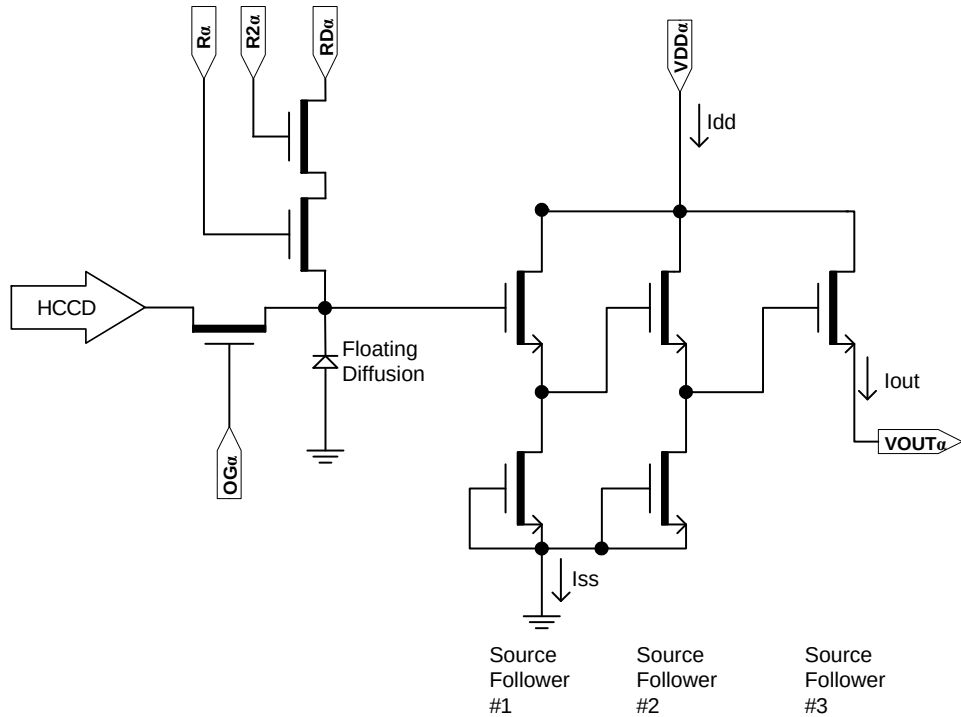


Figure 21. Output Amplifier – Showing Dual Reset Pins



## AC Operating Conditions

Table 17. CLOCK LEVELS

| Description                                   | Pins                       | Symbol           | Level     | Minimum  | Nominal | Maximum  | Units |
|-----------------------------------------------|----------------------------|------------------|-----------|----------|---------|----------|-------|
| Vertical CCD Clock, Phase 1                   | V1B, V1T <sup>1</sup>      | V1_L             | Low       | -8.2     | -8.0    | -7.8     | V     |
|                                               |                            | V1_M             | Mid       | -0.2     | 0.0     | +0.2     |       |
|                                               |                            | V1_H             | High      | +12.8    | +13.0   | +14.0    |       |
| Vertical CCD Clock, Phase 2                   | V2B, V2T <sup>1</sup>      | V2_L             | Low       | -8.2     | -8.0    | -7.8     | V     |
|                                               |                            | V2_H             | High      | -0.2     | 0.0     | +0.2     |       |
| Vertical CCD Clock, Phase 3                   | V3B, V3T <sup>1</sup>      | V3_L             | Low       | -8.2     | -8.0    | -7.8     | V     |
|                                               |                            | V3_H             | High      | -0.2     | 0.0     | +0.2     |       |
| Vertical CCD Clock, Phase 4                   | V4B, V4T <sup>1</sup>      | V4_L             | Low       | -8.2     | -8.0    | -7.8     | V     |
|                                               |                            | V4_H             | High      | -0.2     | 0.0     | +0.2     |       |
| Horizontal CCD Clock, Phase 1 Storage         | H1S $\alpha$ <sup>1</sup>  | H1S_L            | Low       | -5.0 (5) | -4.4    | -4.2     | V     |
|                                               |                            | H1S_A            | Amplitude | +4.2     | +4.4    | +5.0 (5) |       |
| Horizontal CCD Clock, Phase 1 Barrier         | H1B $\alpha$ <sup>1</sup>  | H1B_L            | Low       | -5.0 (5) | -4.4    | -4.2     | V     |
|                                               |                            | H1B_A            | Amplitude | +4.2     | +4.4    | +5.0 (5) |       |
| Horizontal CCD Clock, Phase 2 Storage         | H2S $\alpha$ <sup>1</sup>  | H2S_L            | Low       | -5.0 (5) | -4.4    | -4.2     | V     |
|                                               |                            | H2S_A            | Amplitude | +4.2     | +4.4    | +5.0 (5) |       |
| Horizontal CCD Clock, Phase 2 Barrier         | H2B $\alpha$ <sup>1</sup>  | H2B_L            | Low       | -5.0 (5) | -4.4    | -4.2     | V     |
|                                               |                            | H2B_A            | Amplitude | +4.2     | +4.4    | +5.0 (5) |       |
| Horizontal CCD Clock, Last Phase <sup>2</sup> | H2SL $\alpha$ <sup>1</sup> | H2SL_L           | Low       | -5.2     | -5.0    | -4.8     | V     |
|                                               |                            | H2SL_A           | Amplitude | +4.8     | +5.0    | +5.2     |       |
| Reset Gate                                    | R $\alpha$ <sup>1</sup>    | R_L <sup>3</sup> | Low       | -3.2     | -3.0    | -2.8     | V     |
|                                               |                            | R_A              | Amplitude | +6.0     |         | +6.4     |       |
| Reset Gate                                    | R2ab, R2cd                 | R_L <sup>3</sup> | Low       | -2.0     | -1.8    | -1.6     | V     |
|                                               |                            | R_A              | Amplitude | +6.0     |         | +6.4     |       |
| Electronic Shutter <sup>4</sup>               | SUB                        | VES              | High      | +29.0    | +30.0   | +40.0    | V     |
| Fast Line Dump Gate                           | FDG $\alpha$ <sup>1</sup>  | FDG_L            | Low       | -8.2     | -8.0    | -7.8     | V     |
|                                               |                            | FDG_H            | High      | +4.5     | +5.0    | +5.5     |       |

- $\alpha$  denotes a, b, c or d
- Use separate clock driver for improved speed performance.
- Reset low should be set to -3 volts for signal levels greater than 40,000 electrons.
- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*
- If the minimum horizontal clock low level is used (-5.0 V), then the maximum horizontal clock amplitude should be used (5 V amplitude) to create a -5.0 V to 0.0 V clock.

The figure below shows the DC bias (V<sub>SUB</sub>) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.

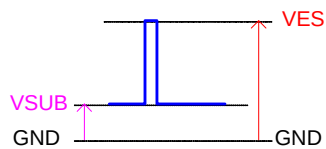


Figure 22.

## Capacitance

Table 18. CAPACITANCE

|      | V1B | V2B | V3B | V4B | V1T | V2T | V3T | V4T | GND | All Pins | Units |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------|-------|
| V1B  | X   | 17  | 11  | 14  | 6   | 5   | 6   | 4   | 24  | 88       | nF    |
| V2B  | X   | X   | 21  | 10  | 5   | 3   | 4   | 3   | 7   | 74       | nF    |
| V3B  | X   | X   | X   | 19  | 6   | 5   | 6   | 4   | 8   | 83       | nF    |
| V4B  | X   | X   | X   | X   | 5   | 4   | 5   | 3   | 23  | 76       | nF    |
| V1T  | X   | X   | X   | X   | X   | 14  | 11  | 17  | 24  | 86       | nF    |
| V2T  | X   | X   | X   | X   | X   | X   | 16  | 6   | 22  | 75       | nF    |
| V3T  | X   | X   | X   | X   | X   | X   | X   | 19  | 11  | 84       | nF    |
| V4T  | X   | X   | X   | X   | X   | X   | X   | X   | 5   | 73       | nF    |
| FDGT | 0.6 | 0.5 | 0.5 | 0.4 | 16  | 3.1 | 1.0 | 1.1 | 94  | 117      | pF    |
| FDGB | 0.6 | 0.5 | 0.5 | 0.4 | 16  | 3.1 | 1.0 | 1.1 | 94  | 117      | pF    |
| VSUB | 2   | 2   | 2   | 2   | 2   | 2   | 2   | 2   | 11  | 11       | nF    |

|     | H2S | H1B | H2B | GND | All Pins | Units |
|-----|-----|-----|-----|-----|----------|-------|
| H1S | 45  | 75  | 44  | 196 | 360      | pF    |
| H2S | X   | 47  | 41  | 281 | 368      | pF    |
| H1B | X   | X   | 12  | 313 | 324      | pF    |
| H2B | X   | X   | X   | 293 | 293      | pF    |

1. Tables show typical cross capacitance between pins of the device.
2. Capacitance is total for all like named pins.

## Device Identification

The device identification pin (DevID) may be used to identify different members of the ON Semiconductor 5.5 micron and 7.4 micron Interline Transfer CCD Platforms.

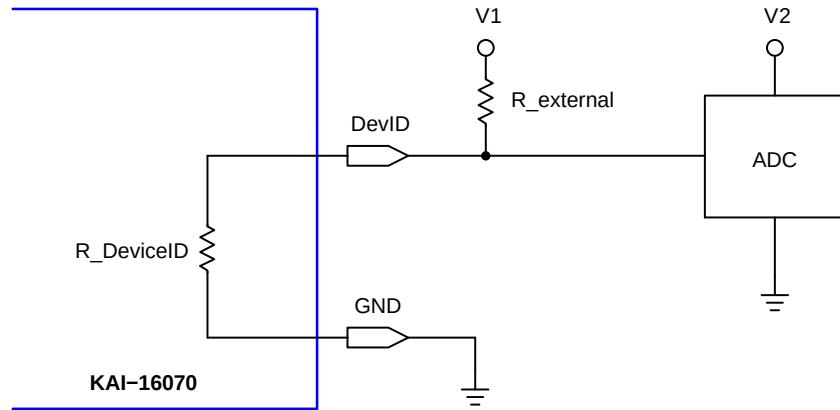
**Table 19. DEVICE IDENTIFICATION**

| Description           | Pins  | Symbol | Minimum | Nominal | Maximum | Units    | Maximum DC Current | Notes   |
|-----------------------|-------|--------|---------|---------|---------|----------|--------------------|---------|
| Device Identification | DevID | DevID  | 32,000  | 40,000  | 48,000  | $\Omega$ | 50 $\mu$ A         | 1, 2, 3 |

1. Nominal value subject to verification and/or change during release of preliminary specifications.
2. If the Device Identification is not used, it may be left disconnected.
3. After Device Identification resistance has been read during camera initialization, it is recommended that the circuit be disabled to prevent localized heating of the sensor due to current flow through the R\_DeviceID resistor.

## Recommended Circuit

Note that V1 must be a different value than V2.



**Figure 23. Device Identification Recommended Circuit**

## TIMING

Table 20. REQUIREMENTS AND CHARACTERISTICS

| Description                                       | Symbol           | Minimum | Nominal | Maximum | Units         | Notes               |
|---------------------------------------------------|------------------|---------|---------|---------|---------------|---------------------|
| Photodiode Transfer                               | $t_{pd}$         | 6       | –       | –       | $\mu\text{s}$ |                     |
| VCCD Leading Pedestal                             | $t_{3p}$         | 16      | –       | –       | $\mu\text{s}$ |                     |
| VCCD Trailing Pedestal                            | $t_{3d}$         | 16      | –       | –       | $\mu\text{s}$ |                     |
| VCCD Transfer Delay                               | $t_d$            | 2       | –       | –       | $\mu\text{s}$ |                     |
| VCCD Transfer                                     | $t_v$            | 4       | –       | –       | $\mu\text{s}$ |                     |
| VCCD Rise, Fall Times                             | $t_{VR}, t_{VF}$ | 5       | –       | 10      | %             | 1, 2                |
| FDG Delay                                         | $t_{fdg}$        | 2       | –       | –       | $\mu\text{s}$ |                     |
| HCCD Delay                                        | $t_{hs}$         | 2       | –       | –       | $\mu\text{s}$ |                     |
| HCCD Transfer                                     | $t_e$            | 25.0    | –       | –       | ns            |                     |
| Shutter Transfer                                  | $t_{sub}$        | 2       | –       | –       | $\mu\text{s}$ |                     |
| Shutter Delay                                     | $t_{hd}$         | 2       | –       | –       | $\mu\text{s}$ |                     |
| Reset Pulse                                       | $t_r$            | 2.5     | –       | –       | ns            |                     |
| Reset – Video Delay                               | $t_{rv}$         | –       | 2.2     | –       | ns            |                     |
| H2SL – Video Delay                                | $t_{hv}$         | –       | 2.2     | –       | ns            |                     |
| Line Time                                         | $t_{line}$       | 77.9    | –       | –       | $\mu\text{s}$ | Dual HCCD Readout   |
|                                                   |                  | 140     | –       | –       |               | Single HCCD Readout |
| Frame Time                                        | $t_{frame}$      | 129     | –       | –       | ms            | Quad HCCD Readout   |
|                                                   |                  | 257     | –       | –       |               | Dual HCCD Readout   |
|                                                   |                  | 461     | –       | –       |               | Single HCCD Readout |
| Line Time (XLDR Bin 2x2)                          | $t_{line}$       | 124.9   | –       | –       | $\mu\text{s}$ | Dual HCCD Readout   |
|                                                   |                  | 217.4   | –       | –       |               | Single HCCD Readout |
| Frame Time (XLDR Bin 2x2)<br>Constant HCCD Timing | $t_{frame}$      | 133     | –       | –       | ms            | Quad HCCD Readout   |
|                                                   |                  | 267     | –       | –       |               | Dual HCCD Readout   |
|                                                   |                  | 466     | –       | –       |               | Single HCCD Readout |
| Frame Time (XLDR Bin 2x2)<br>Variable HCCD Timing | $t_{frame}$      | 103     | –       | –       | ms            | Quad HCCD Readout   |
|                                                   |                  | 206     | –       | –       |               | Dual HCCD Readout   |
|                                                   |                  | 359     | –       | –       |               | Single HCCD Readout |

1. Refer to Figure 41: VCCD Clock Rise Time and Fall Time.

2. Relative to the pulse width,  $t_v$ .

### Timing Flow Charts

In the timing flow charts the number of HCCD clock cycles per row, NH, and the number of VCCD clock cycles per frame, NV, are shown in the following table.

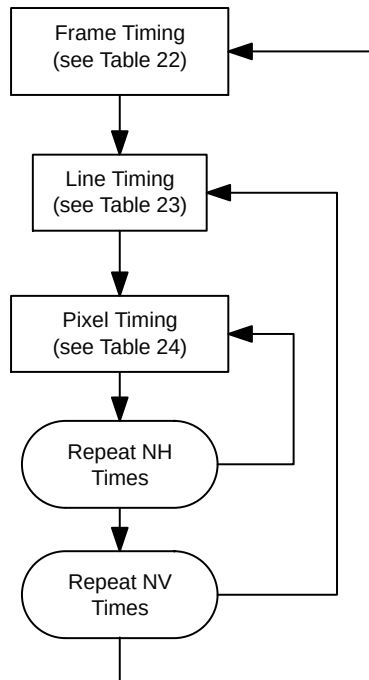
**Table 21. VALUES FOR NH AND NV WHEN OPERATING THE SENSOR IN THE VARIOUS MODES OF RESOLUTION**

|                   | Full Resolution |      | 1/4 Resolution |      | XLDR |      |
|-------------------|-----------------|------|----------------|------|------|------|
|                   | NV              | NH   | NV             | NH   | NV   | NH   |
| Quad              | 1650            | 2477 | 825            | 1238 | 825  | 1238 |
| Dual VOUTa, VOUTc | 1650            | 4943 | 825            | 2471 | 825  | 2471 |
| Dual VOUTa, VOUTb | 3278            | 2477 | 1639           | 1238 | 1639 | 1238 |
| Single VOUTa      | 3278            | 4943 | 1639           | 2471 | 1639 | 2471 |

1. The time to read out one line  $t_{LINE} = \text{Line Timing} + NH / (\text{Pixel Frequency})$ .
2. The time to read out one frame  $t_{FRAME} = NV \cdot t_{LINE} + \text{Frame Timing}$ .
3. Line Timing: See Table 23: Line Timing.
4. Frame Timing: See Table 22: Frame Timing.
5. XLDR: eXtended Linear Dynamic Range.

### No Electronic Shutter

In this case the photodiode exposure time is equal to the time to read out an image. This flow chart applies to both full and 1/4 resolution modes.

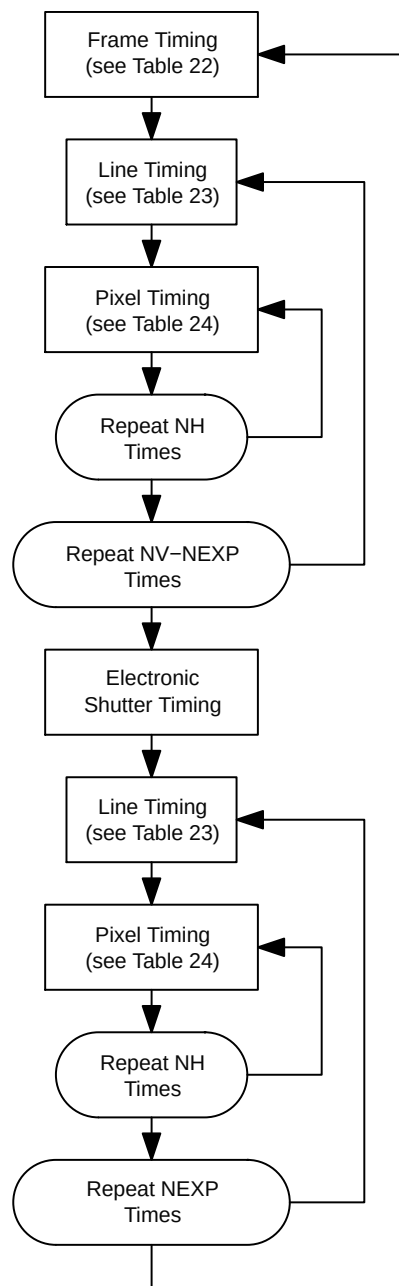


**Figure 24. Timing Flow when Electronic Shutter is Not Used**

### Using the Electronic Shutter

This flow chart applies to both the full and 1/4 resolution modes. The exposure time begins on the falling edge of the electronic shutter pulse on the SUB pin. The exposure time ends on the falling edge of the +13 V to 0 V transition of the

V1T and V1B pins. NEXP is varied to change the exposure time in increments of the line time. The electronic shutter timing is obtained from Figure 33.



NOTE: NEXP: Exposure time in increments of number of lines.

**Figure 25. Timing Flow Chart using the Electronic Shutter for Exposure Control**

### Window Readout Using the Fast Dump

This timing quickly dumps NV1 lines, then reads out NV2 lines, and then quickly dumps another NV3 lines. NV1 + NV2 + NV3 must be greater than or equal to NV. Note when operating in quad or dual VOUTa + VOUTc modes the NV2 valid image lines must be in the center of the pixel array or contained entirely within the bottom half or top half of the pixel array. This is due to the top and bottom middle split of

the VCCD. In the single output or dual VOUTa + VOUTb modes the NV2 valid image lines may be located anywhere within the pixel array.

The line timing with the FDGab and FDGcd pins disabled means those pins are held at a constant -9 V. When they are enabled, they are held at +5 V during a line transfer.

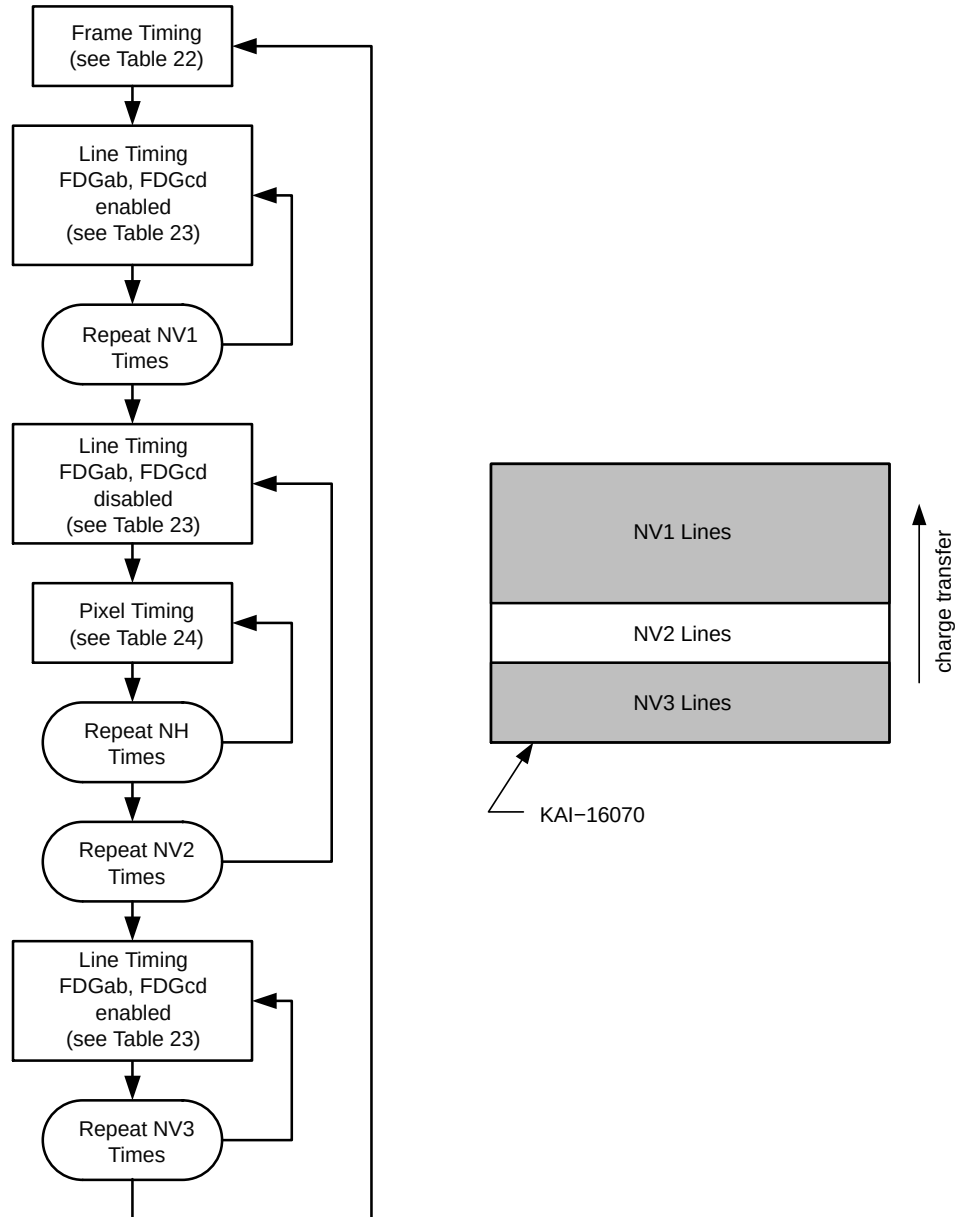
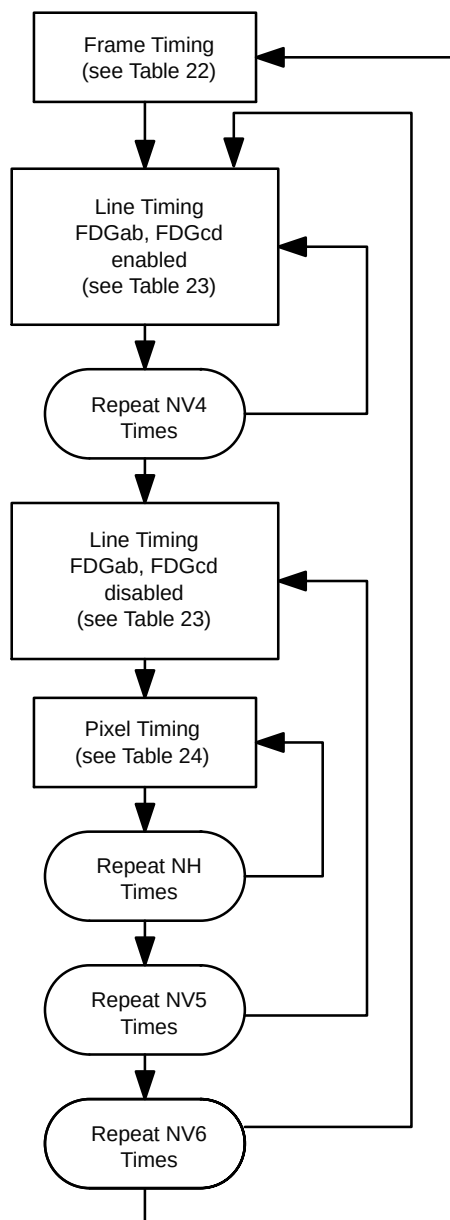


Figure 26. Sub Window Timing Flow Chart

*Line Sampling Readout Using the Fast Dump*

This timing repeats the process of dumping NV4 lines and reading NV5 lines. The total  $NV6 \times (NV4 + NV5)$  must be greater than or equal to NV. This timing can be used for alternately skipping and reading lines. For example, if

NV4 = 2 and NV5 = 1 then every third line will be read out (skip 2 read 1).



**Figure 27. Timing Flow Chart to Alternately Skip and Read Rows for Subsampling**



## Timing Tables

## Frame Timing

This timing table is for transferring charge from the photodiodes to the VCCD.

Table 22. FRAME TIMING

| Device Pin | Full Resolution, High Gain or Low Gain |                  |                  |              | 1/4 Resolution, High Gain or Low Gain |                  |                  |              | 1/4 Resolution XLDR |                  |                  |              |
|------------|----------------------------------------|------------------|------------------|--------------|---------------------------------------|------------------|------------------|--------------|---------------------|------------------|------------------|--------------|
|            | Quad                                   | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa | Quad                                  | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa | Quad                | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa |
| V1T        | F1T                                    |                  | F1B              |              | F1T                                   |                  | F1B              |              | F1T                 |                  | F1B              |              |
| V2T        | F2T                                    |                  | F4B              |              | F2T                                   |                  | F4B              |              | F2T                 |                  | F4B              |              |
| V3T        | F3T                                    |                  | F3B              |              | F3T                                   |                  | F3B              |              | F3T                 |                  | F3B              |              |
| V4T        | F4T                                    |                  | F2B              |              | F4T                                   |                  | F2B              |              | F4T                 |                  | F2B              |              |
| V1B        | F1B                                    |                  |                  |              | F1B                                   |                  |                  |              | F1B                 |                  |                  |              |
| V2B        | F2B                                    |                  |                  |              | F2B                                   |                  |                  |              | F2B                 |                  |                  |              |
| V3B        | F3B                                    |                  |                  |              | F3B                                   |                  |                  |              | F3B                 |                  |                  |              |
| V4B        | F4B                                    |                  |                  |              | F4B                                   |                  |                  |              | F4B                 |                  |                  |              |
| H1Sa       | P1                                     |                  |                  |              | P1Q                                   |                  |                  |              | P1XL                |                  |                  |              |
| H1Ba       | P1                                     |                  |                  |              | P1Q                                   |                  |                  |              | P1XL                |                  |                  |              |
| H2Sa       | P2                                     |                  |                  |              | P2Q                                   |                  |                  |              | P2XL                |                  |                  |              |
| H2Ba       | P2                                     |                  |                  |              | P2Q                                   |                  |                  |              | P2XL                |                  |                  |              |
| Ra         | RHG/RLG                                |                  |                  |              | RHGQ/RLGQ                             |                  |                  |              | RXL                 |                  |                  |              |
| H1Sb       | P1                                     |                  |                  |              | P1Q                                   |                  |                  |              | P1XL                |                  |                  |              |
| H1Bb       | P1                                     | P2               | P1               | P2           | P1Q                                   | P2Q              | P1Q              | P2Q          | P1XL                | P2XL             | P1XL             | P2XL         |
| H2Sb       | P2                                     |                  |                  |              | P2Q                                   |                  |                  |              | P2XL                |                  |                  |              |
| H2Bb       | P2                                     | P1               | P2               | P1           | P2Q                                   | P1Q              | P2Q              | P1Q          | P2XL                | P1XL             | P2XL             | P1XL         |
| Rb         | RHG/RLG                                | (Note 1)         | RHG/RLG          | (Note 1)     | RHGQ/RLGQ                             | (Note 1)         | RHGQ/RLGQ        | (Note 1)     | RXL                 | (Note 1)         | RXL              | (Note 1)     |
| R2ab       | R2HG/R2LG                              |                  |                  |              | R2HGQ/R2LGQ                           |                  |                  |              | R2XL                |                  |                  |              |
| FDGab      | -9 V                                   |                  |                  |              | -9 V                                  |                  |                  |              | -9 V                |                  |                  |              |
| H1Sc       | P1                                     |                  | (Note 1)         |              | P1Q                                   |                  | (Note 1)         |              | P1XL                |                  | (Note 1)         |              |
| H1Bc       | P1                                     |                  | (Note 1)         |              | P1Q                                   |                  | (Note 1)         |              | P1XL                |                  | (Note 1)         |              |
| H2Sc       | P2                                     |                  | (Note 1)         |              | P2Q                                   |                  | (Note 1)         |              | P2XL                |                  | (Note 1)         |              |
| H2Bc       | P2                                     |                  | (Note 1)         |              | P2Q                                   |                  | (Note 1)         |              | P2XL                |                  | (Note 1)         |              |
| Rc         | RHG/RLG                                |                  | (Note 1)         |              | RHGQ/RLGQ                             |                  | (Note 1)         |              | RXL                 |                  | (Note 1)         |              |
| H1Sd       | P1                                     |                  | (Note 1)         |              | P1Q                                   |                  | (Note 1)         |              | P1XL                |                  | (Note 1)         |              |
| H1Bd       | P1                                     | P2               | (Note 1)         |              | P1Q                                   | P2Q              | (Note 1)         |              | P1XL                | P2XL             | (Note 1)         |              |
| H2Sd       | P2                                     |                  | (Note 1)         |              | P2Q                                   |                  | (Note 1)         |              | P2XL                |                  | (Note 1)         |              |
| H2Bd       | P2                                     | P1               | (Note 1)         |              | P2Q                                   | P1Q              | (Note 1)         |              | P2XL                | P1XL             | (Note 1)         |              |
| Rd         | RHG/RLG                                | (Note 1)         | (Note 1)         |              | RHGQ/RLGQ                             | (Note 1)         | (Note 1)         |              | RXL                 | (Note 1)         | (Note 1)         |              |
| R2cd       | R2HG/R2LG                              |                  | (Note 1)         |              | R2HGQ/R2LGQ                           |                  | (Note 1)         |              | R2XL                |                  | (Note 1)         |              |
| FDGcd      | -9 V                                   |                  |                  |              | -9 V                                  |                  |                  |              | -9 V                |                  |                  |              |
| SHP        | SHP1                                   |                  |                  |              | SHPQ                                  |                  |                  |              | (Note 4)            |                  |                  |              |
| SHD        | SHD1                                   |                  |                  |              | SHDQ                                  |                  |                  |              | (Note 5)            |                  |                  |              |

1. This clock should be held at its high level voltage (0 V) or held at +5.0 V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products.
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor.
3. This note left intentionally empty.
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal.
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal.

*Line Timing*

This timing is for transferring one line of charge from the VCCD to the HCCD.

**Table 23. LINE TIMING**

| Device Pin | Full Resolution, High Gain or Low Gain |                  |                  |              | 1/4 Resolution, High Gain or Low Gain |                  |                  |              | 1/4 Resolution XLDR |                  |                  |              |
|------------|----------------------------------------|------------------|------------------|--------------|---------------------------------------|------------------|------------------|--------------|---------------------|------------------|------------------|--------------|
|            | Quad                                   | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa | Quad                                  | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa | Quad                | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa |
| V1T        | L1T                                    |                  | L1B              |              | 2 × L1T                               |                  | 2 × L1B          |              | 2 × L1T             |                  | 2 × L1B          |              |
| V2T        | L2T                                    |                  | L4B              |              | 2 × L2T                               |                  | 2 × L4B          |              | 2 × L2T             |                  | 2 × L4B          |              |
| V3T        | L3T                                    |                  | L3B              |              | 2 × L3T                               |                  | 2 × L3B          |              | 2 × L3T             |                  | 2 × L3B          |              |
| V4T        | L4T                                    |                  | L2B              |              | 2 × L4T                               |                  | 2 × L2B          |              | 2 × L4T             |                  | 2 × L2B          |              |
| V1B        | L1B                                    |                  |                  |              | 2 × L1B                               |                  |                  |              | 2 × L1B             |                  |                  |              |
| V2B        | L2B                                    |                  |                  |              | 2 × L2B                               |                  |                  |              | 2 × L2B             |                  |                  |              |
| V3B        | L3B                                    |                  |                  |              | 2 × L3B                               |                  |                  |              | 2 × L3B             |                  |                  |              |
| V4B        | L4B                                    |                  |                  |              | 2 × L4B                               |                  |                  |              | 2 × L4B             |                  |                  |              |
| H1Sa       | P1L                                    |                  |                  |              | P1LQ                                  |                  |                  |              | P3XL                |                  |                  |              |
| H1Ba       | P1L                                    |                  |                  |              | P1LQ                                  |                  |                  |              | P3XL                |                  |                  |              |
| H2Sa       | P2L                                    |                  |                  |              | P2LQ                                  |                  |                  |              | P4XL                |                  |                  |              |
| H2Ba       | P2L                                    |                  |                  |              | P2LQ                                  |                  |                  |              | P4XL                |                  |                  |              |
| Ra         | RHG/RLG                                |                  |                  |              | RHGQ/RLGQ                             |                  |                  |              | RXL                 |                  |                  |              |
| H1Sb       | P1L                                    |                  |                  |              | P1LQ                                  |                  |                  |              | P3XL                |                  |                  |              |
| H1Bb       | P1L                                    | P2L              | P1L              | P2L          | P1LQ                                  | P2LQ             | P1LQ             | P2LQ         | P3XL                | P4XL             | P3XL             | P4XL         |
| H2Sb       | P2L                                    |                  |                  |              | P2LQ                                  |                  |                  |              | P4XL                |                  |                  |              |
| H2Bb       | P2L                                    | P1L              | P2L              | P1L          | P2LQ                                  | P1LQ             | P2LQ             | P1LQ         | P4XL                | P3XL             | P4XL             | P3XL         |
| Rb         | RHG/RLG                                | (Note 1)         | RHG/RLG          | (Note 1)     | RHGQ/RLGQ                             | (Note 1)         | RHGQ/RLGQ        | (Note 1)     | RXL                 | (Note 1)         | RXL              | (Note 1)     |
| R2ab       | R2HG/R2LG                              |                  |                  |              | R2HGQ/R2LGQ                           |                  |                  |              | R2XL                |                  |                  |              |
| FDGab      | -9 V                                   |                  |                  |              | -9 V                                  |                  |                  |              | -9 V                |                  |                  |              |
| H1Sc       | P1L                                    |                  | (Note 1)         |              | P1LQ                                  |                  | (Note 1)         |              | P3XL                |                  | (Note 1)         |              |
| H1Bc       | P1L                                    |                  | (Note 1)         |              | P1LQ                                  |                  | (Note 1)         |              | P3XL                |                  | (Note 1)         |              |
| H2Sc       | P2L                                    |                  | (Note 1)         |              | P2LQ                                  |                  | (Note 1)         |              | P4XL                |                  | (Note 1)         |              |
| H2Bc       | P2L                                    |                  | (Note 1)         |              | P2LQ                                  |                  | (Note 1)         |              | P4XL                |                  | (Note 1)         |              |
| Rc         | RHG/RLG                                |                  | (Note 1)         |              | RHGQ/RLGQ                             |                  | (Note 1)         |              | RXL                 |                  | (Note 1)         |              |
| H1Sd       | P1L                                    |                  | (Note 1)         |              | P1LQ                                  |                  | (Note 1)         |              | P3XL                |                  | (Note 1)         |              |
| H1Bd       | P1L                                    | P2L              | (Note 1)         |              | P1LQ                                  | P2LQ             | (Note 1)         |              | P3XL                | P4XL             | (Note 1)         |              |
| H2Sd       | P2L                                    |                  | (Note 1)         |              | P2LQ                                  |                  | (Note 1)         |              | P4XL                |                  | (Note 1)         |              |
| H2Bd       | P2L                                    | P1L              | (Note 1)         |              | P2LQ                                  | P1LQ             | (Note 1)         |              | P4XL                | P3XL             | (Note 1)         |              |
| Rd         | RHG/RLG                                | (Note 1)         | (Note 1)         |              | RHGQ/RLGQ                             | (Note 1)         | (Note 1)         |              | RXL                 | (Note 1)         | (Note 1)         |              |
| R2cd       | R2HG/R2LG                              |                  | (Note 1)         |              | R2HGQ/R2LGQ                           |                  | (Note 1)         |              | R2XL                |                  | (Note 1)         |              |
| FDGcd      | -9 V                                   |                  |                  |              | -9 V                                  |                  |                  |              | -9 V                |                  |                  |              |
| SHP        | SHP1                                   |                  |                  |              | SHPQ                                  |                  |                  |              | (Note 4)            |                  |                  |              |
| SHD        | SHD1                                   |                  |                  |              | SHDQ                                  |                  |                  |              | (Note 5)            |                  |                  |              |

1. This clock should be held at its high level voltage (0 V) or held at +5.0 V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products.
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor.
3. The notation 2× L1B means repeat the L1B timing twice for every line. This sums two rows into the HCCD.
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal.
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal.

*Pixel Timing*

This timing is for transferring one pixel from the HCCD to the output amplifier.

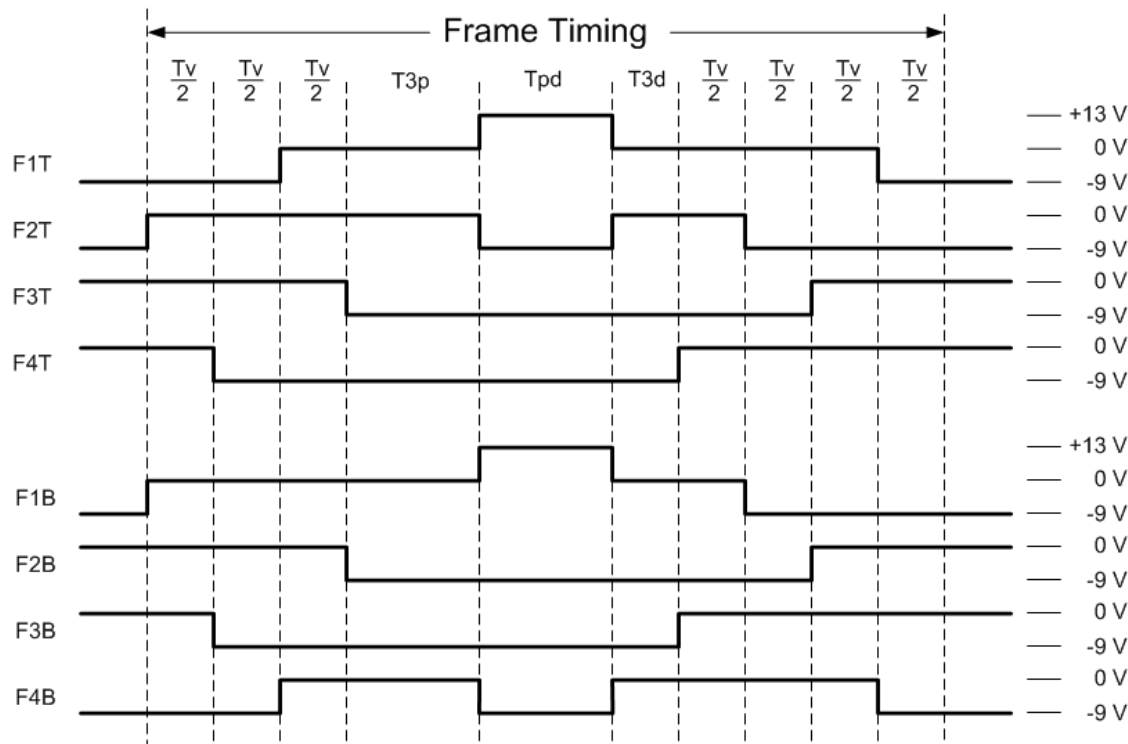
**Table 24. PIXEL TIMING**

| Device Pin   | Full Resolution, High Gain or Low Gain |                  |                  |              | 1/4 Resolution, High Gain or Low Gain |                  |                  |              | 1/4 Resolution XLDR |                  |                  |              |
|--------------|----------------------------------------|------------------|------------------|--------------|---------------------------------------|------------------|------------------|--------------|---------------------|------------------|------------------|--------------|
|              | Quad                                   | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa | Quad                                  | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa | Quad                | Dual VOUTa VOUTc | Dual VOUTa VOUTb | Single VOUTa |
| V1T          | −9 V                                   |                  |                  |              | −9 V                                  |                  |                  |              | −9 V                |                  |                  |              |
| V2T          | −9 V                                   |                  |                  |              | −9 V                                  |                  |                  |              | −9 V                |                  |                  |              |
| V3T          | 0 V                                    |                  |                  |              | 0 V                                   |                  |                  |              | 0 V                 |                  |                  |              |
| V4T          | 0 V                                    |                  |                  |              | 0 V                                   |                  |                  |              | 0 V                 |                  |                  |              |
| V1B          | −9 V                                   |                  |                  |              | −9 V                                  |                  |                  |              | −9 V                |                  |                  |              |
| V2B          | 0 V                                    |                  |                  |              | 0 V                                   |                  |                  |              | 0 V                 |                  |                  |              |
| V3B          | 0 V                                    |                  |                  |              | 0 V                                   |                  |                  |              | 0 V                 |                  |                  |              |
| V4B          | −9 V                                   |                  |                  |              | −9 V                                  |                  |                  |              | −9 V                |                  |                  |              |
| H1Sa         | P1                                     |                  |                  |              | P1Q                                   |                  |                  |              | P1XL                |                  |                  |              |
| H1Ba         | P1                                     |                  |                  |              | P1Q                                   |                  |                  |              | P1XL                |                  |                  |              |
| H2Sa         | P2                                     |                  |                  |              | P2Q                                   |                  |                  |              | P2XL                |                  |                  |              |
| H2Ba         | P2                                     |                  |                  |              | P2Q                                   |                  |                  |              | P2XL                |                  |                  |              |
| Ra           | RHG/RLG                                |                  |                  |              | RHGQ/RLGQ                             |                  |                  |              | RXL                 |                  |                  |              |
| H1Sb         | P1                                     |                  |                  |              | P1Q                                   |                  |                  |              | P1XL                |                  |                  |              |
| H1Bb         | P1                                     | P2               | P1               | P2           | P1Q                                   | P2Q              | P1Q              | P2Q          | P1XL                | P2XL             | P1XL             | P2XL         |
| H2Sb         | P2                                     |                  |                  |              | P2Q                                   |                  |                  |              | P2XL                |                  |                  |              |
| H2Bb         | P2                                     | P1               | P2               | P1           | P2Q                                   | P1Q              | P2Q              | P1Q          | P2XL                | P1XL             | P2XL             | P1XL         |
| Rb           | RHG/RLG                                | (Note 1)         | RHG/RLG          | (Note 1)     | RHGQ/RLGQ                             | (Note 1)         | RHGQ/RLGQ        | (Note 1)     | RXL                 | (Note 1)         | RXL              | (Note 1)     |
| R2ab         | R2HG/R2LG                              |                  |                  |              | R2HGQ/R2LGQ                           |                  |                  |              | R2XL                |                  |                  |              |
| R2ab         | −9 V                                   |                  |                  |              | −9 V                                  |                  |                  |              | −9 V                |                  |                  |              |
| H1Sc         | P1                                     |                  | (Note 1)         |              | P1Q                                   |                  | (Note 1)         |              | P1XL                |                  | (Note 1)         |              |
| H1Bc         | P1                                     |                  | (Note 1)         |              | P1Q                                   |                  | (Note 1)         |              | P1XL                |                  | (Note 1)         |              |
| H2Sc         | P2                                     |                  | (Note 1)         |              | P2Q                                   |                  | (Note 1)         |              | P2XL                |                  | (Note 1)         |              |
| H2Bc         | P2                                     |                  | (Note 1)         |              | P2Q                                   |                  | (Note 1)         |              | P2XL                |                  | (Note 1)         |              |
| Rc           | RHG/RLG                                |                  | (Note 1)         |              | RHGQ/RLGQ                             |                  | (Note 1)         |              | RXL                 |                  | (Note 1)         |              |
| H1Sd         | P1                                     |                  | (Note 1)         |              | P1Q                                   |                  | (Note 1)         |              | P1XL                |                  | (Note 1)         |              |
| H1Bd         | P1                                     | P2               | (Note 1)         |              | P1Q                                   | P2Q              | (Note 1)         |              | P1XL                | P2XL             | (Note 1)         |              |
| H2Sd         | P2                                     |                  | (Note 1)         |              | P2Q                                   |                  | (Note 1)         |              | P2XL                |                  | (Note 1)         |              |
| H2Bd         | P2                                     | P1               | (Note 1)         |              | P2Q                                   | P1Q              | (Note 1)         |              | P2XL                | P1XL             | (Note 1)         |              |
| Rd           | RHG/RLG                                | (Note 1)         | (Note 1)         |              | RHGQ/RLGQ                             | (Note 1)         | (Note 1)         |              | RXL                 | (Note 1)         | (Note 1)         |              |
| R2cd         | R2HG/R2LG                              |                  | (Note 1)         |              | R2HGQ/R2LGQ                           |                  | (Note 1)         |              | R2XL                |                  | (Note 1)         |              |
| R2ab         | −9 V                                   |                  |                  |              | −9 V                                  |                  |                  |              | −9 V                |                  |                  |              |
| SHP (Note 2) | SHP1                                   |                  |                  |              | SHPQ                                  |                  |                  |              | (Note 4)            |                  |                  |              |
| SHD (Note 2) | SHD1                                   |                  |                  |              | SHDQ                                  |                  |                  |              | (Note 5)            |                  |                  |              |

1. This clock should be held at its high level voltage (0 V) or held at +5.0 V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products.
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor.
3. This note intentionally left empty.
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal.
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal.

Timing Diagrams

Frame TimingDiagrams



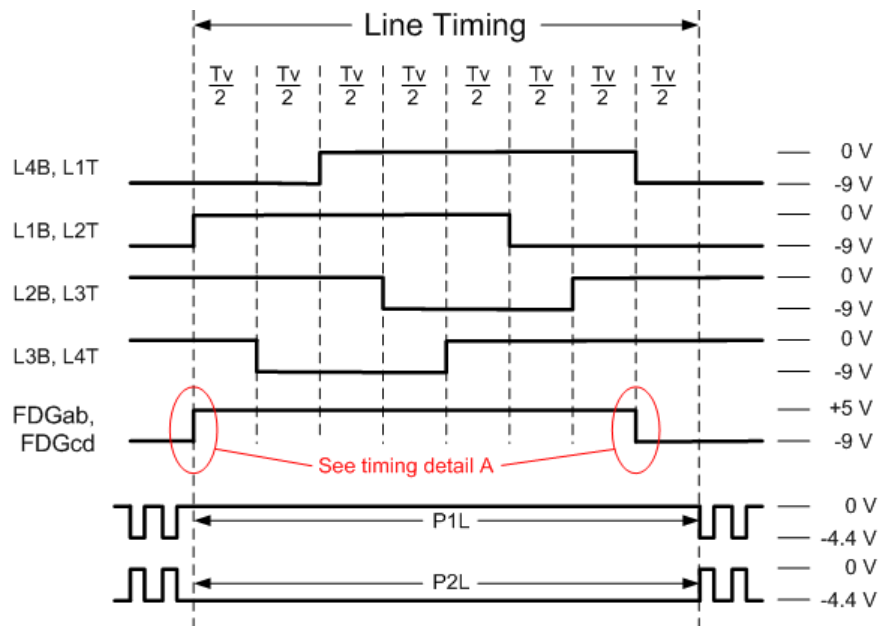
NOTE: See Table 22 for pin assignments.

Figure 28. Frame Timing Diagram

The charge in the photodiodes begins its transfer to the VCCD on the rising edge of the +13 V pulse and is completed by the falling edge of the +13 V pulse on F1T and

F1B. During the time period when F1T and F1B are at +13 V antiblooming protection is disabled. The photodiode integration time ends on the falling edge of the +13 V pulse.

Line Timing Diagrams

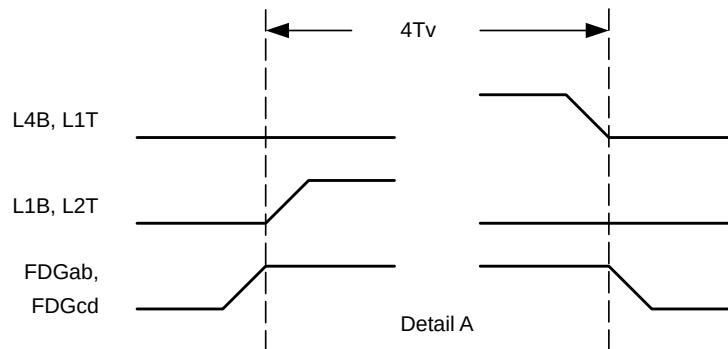


NOTE: See Table 23 for device pin assignments.

Figure 29. Line Timing Diagram

If the line is to be dumped then clock the FDGab and FDGcd pins as shown. This dumping process eliminates a line of charge and the HCCD does not have to be clocked.

To transfer a line from the VCCD to the HCCD without dumping the charge, hold the FDGab and FDGcd pins at a constant -9 V.

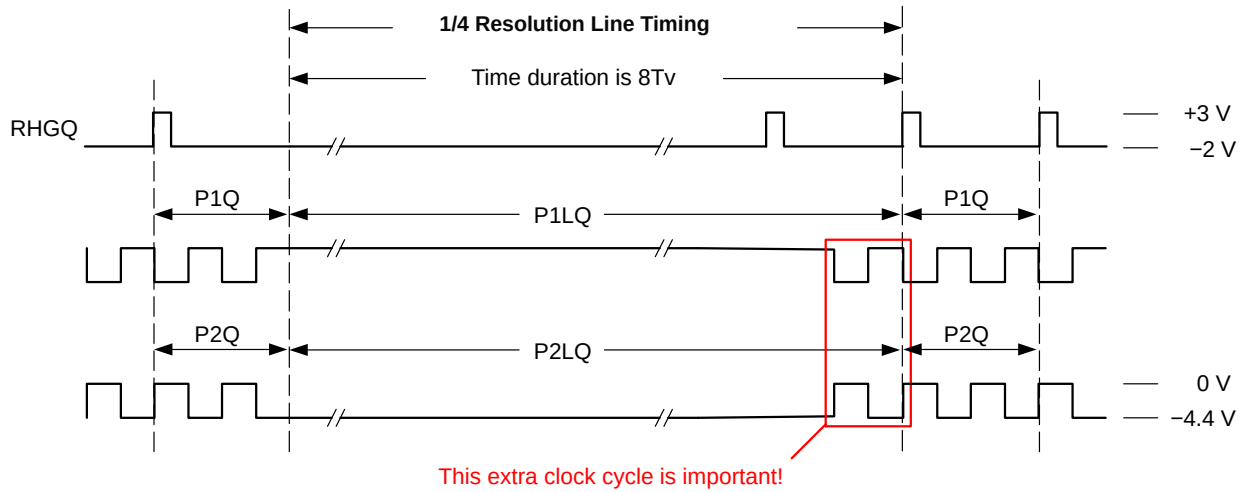


NOTE: See Table 23 for device pin assignments.

Figure 30. Fast Dump Gate Timing Detail A

When the VCCD is clocked while the FDGab and FDGcd pins are at +5 V, charge is diverted to a drain instead of transferring to the HCCD. The FDG pins must be at +5 V before the first VCCD timing edge begins its transition. The

FDG pin must not begin its transition from +5 V back to -9 V until the last VCCD timing edge has completed its transition.

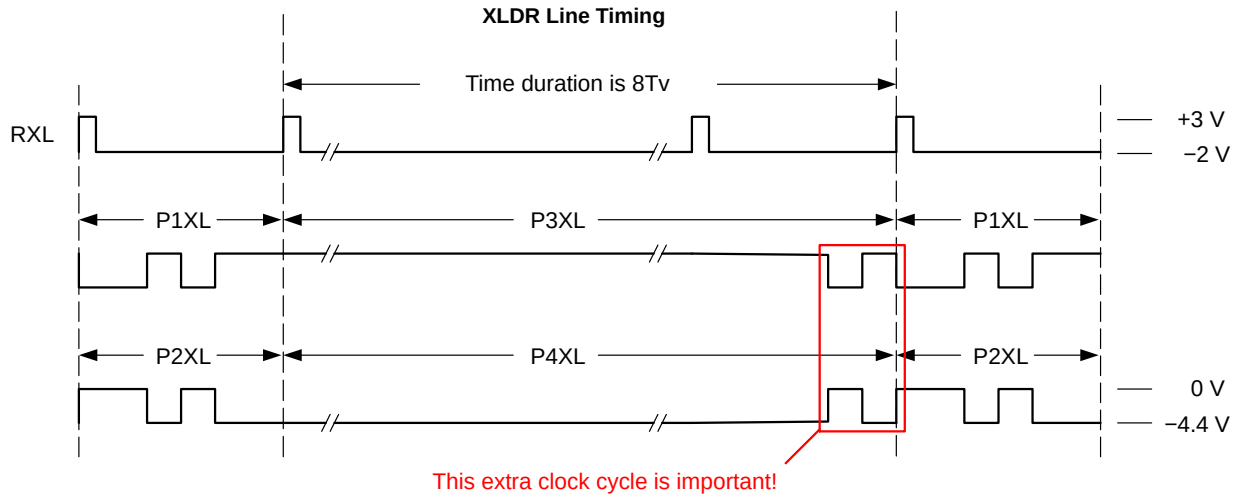


NOTE: See Table 23 center column for pin assignments.

**Figure 31. 1/4 Resolution Line Timing Diagram**

The HCCD 1/4 resolution timing has one HCCD clock cycle added. This does a one pixel shift of the HCCD before the 2-pixel charge summing starts on the output amplifier. The one pixel shift is necessary because of the odd number

(11 pixels) of dummy pixels at the start of the HCCD. Without the one pixel shift the last dark reference columns would be summed with the first photoactive column instead of adding together the first two photoactive columns.



NOTE: See Table 23 right columns for pin assignments.

**Figure 32. XLDR Line Timing Diagram**

Like the 1/4 resolution mode, the XLDR timing also sums two pixels on the output amplifier sense node. Therefore it also requires one HCCD clock cycle within the line timing.

Electronic Shutter Timing Diagram

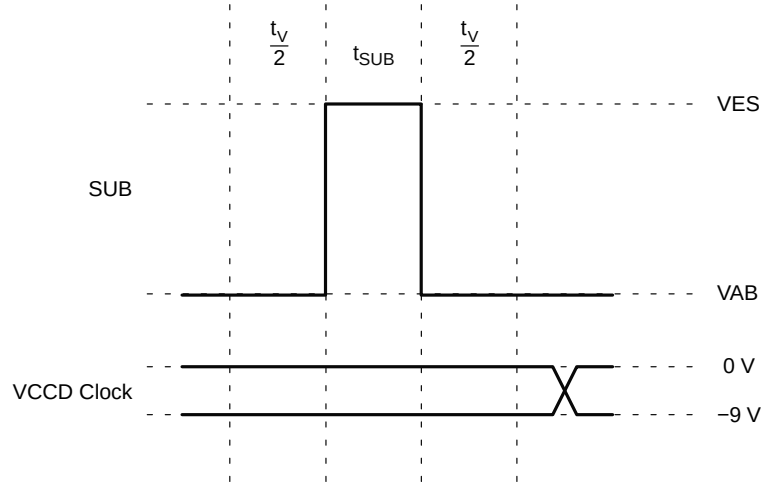


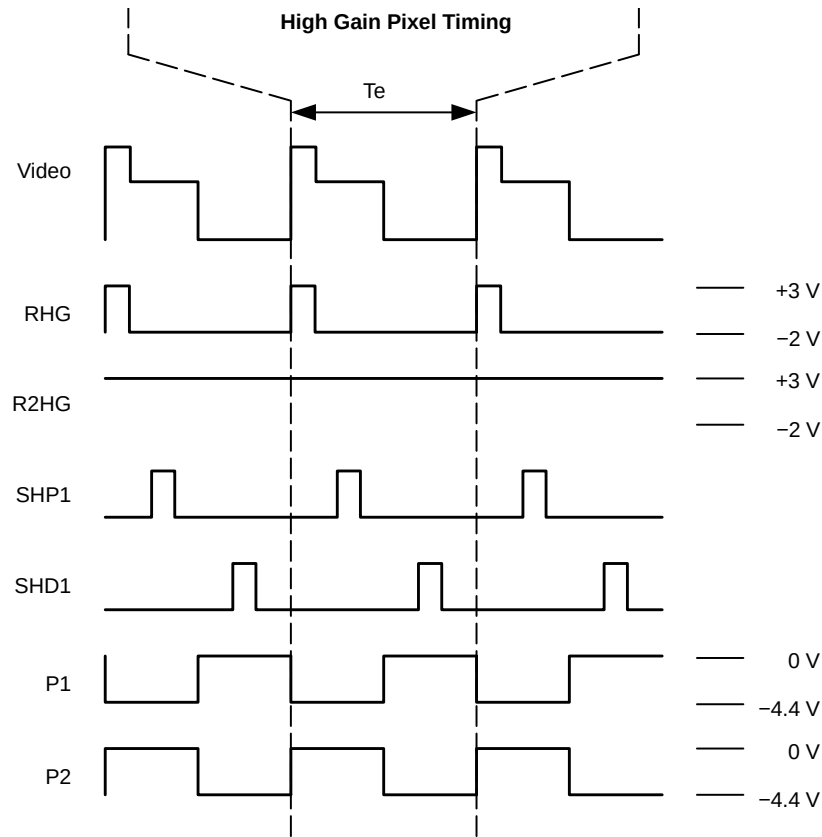
Figure 33. Electronic Shutter Timing Diagram

The electronic shutter pulse can be inserted at the end of any line of the HCCD timing. The HCCD should be empty when the electronic shutter is pulsed. A recommended position for the electronic shutter is just after the last pixel is read out of a line. The VCCD clocks should not resume until at least  $t_V/2$   $\mu$ s after the electronic shutter pulse has finished. The HCCD clocks can be run during the electronic

shutter pulse as long as the HCCD does not contain valid image data.

For short exposures less than one line time, the electronic shutter pulse can appear inside the frame timing diagram of Figure 28. Any electronic shutter pulse transition should be  $t_V/2$  away from any VCCD clock transition.

Pixel Timing Diagrams



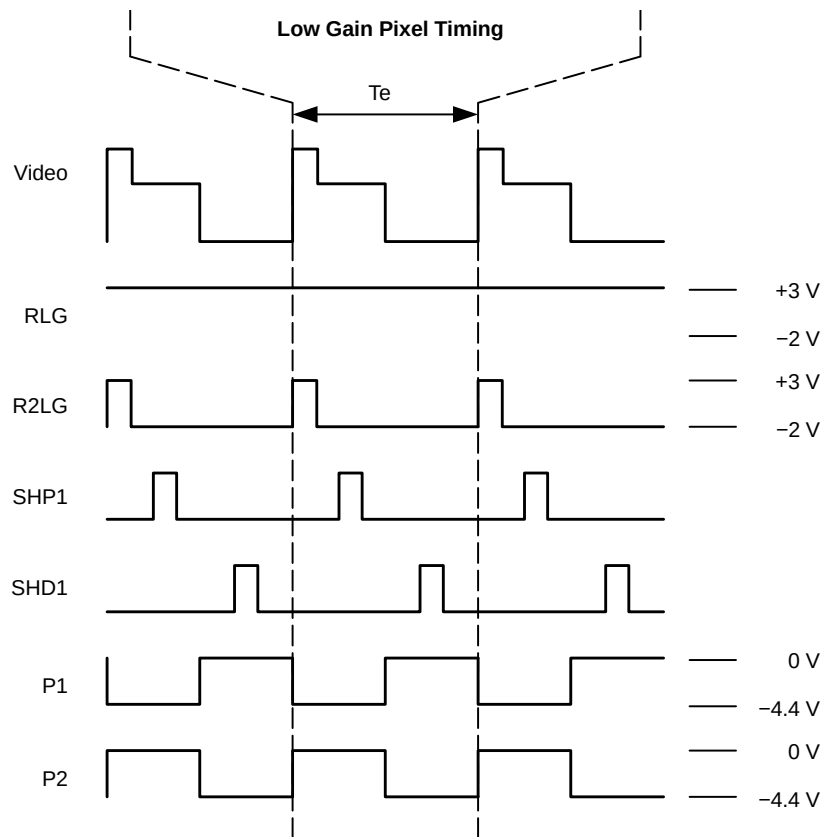
NOTE: See Table 24 left columns for pin assignments.

Figure 34. High Gain Pixel Timing

Use this pixel timing to read out every pixel at high gain. If the sensor is to be permanently operated at high gain, the R2ab and R2cd pins can be left floating or set to any DC voltage between +3 V and +5 V. They are internally biased

to +4.3 V. The SHP1 and SHD1 pulses indicate where the camera electronics should sample the video waveform. The SHP1 and SHD1 pulses are not applied to the image sensor.



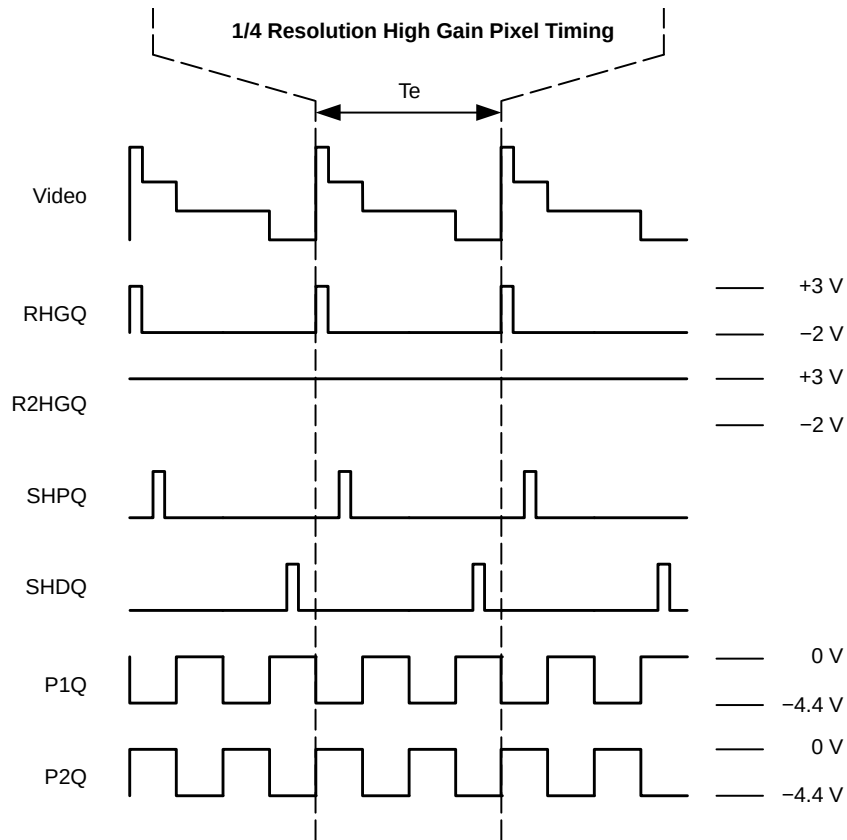


NOTE: See Table 24 left columns for pin assignments.

**Figure 35. Low Gain Pixel Timing**

Use this timing to read out every pixel at low gain. If the sensor is to be permanently operated at low gain, the Ra, Rb, Rc, and Rd pins can be set to any DC voltage between +3 V

and +5 V. The SHP1 and SHD1 pulses indicate where the camera electronics should sample the video waveform. The SHP1 and SHD1 pulses are not applied to the image sensor.

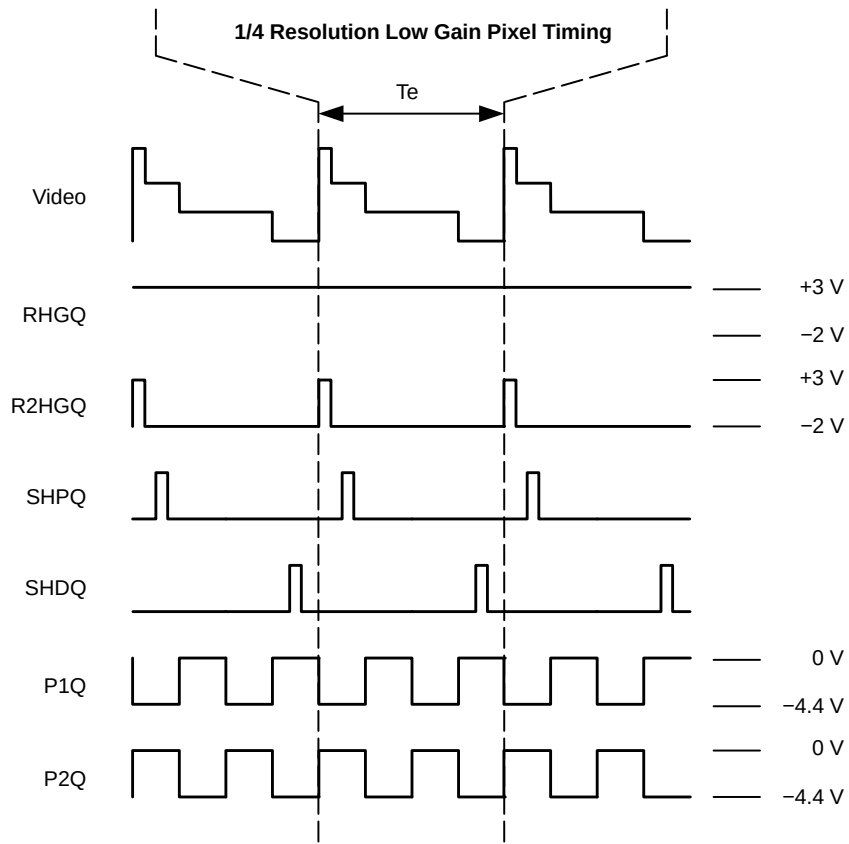


NOTE: See Table 24 center columns for pin assignments.

**Figure 36. 1/4 Resolution High Gain Pixel Timing**

Use this pixel timing to read out every pixel at high gain. If the sensor is to be permanently operated at high gain, the R2ab and R2cd pins can be left floating or set to any DC voltage between +3 V and +5 V. They are internally biased to +4.3 V. The SHPQ and SHDQ pulses indicate where the camera electronics should sample the video waveform. The SHPQ and SHDQ pulses are not applied to the image sensor.

The Ra, Rb, Rc, and Rd pins are pulsed at half the frequency of the HCCD clocks. This causes two pixels to be summed on the output amplifier sense node. The SHPQ and SHDQ clocks are also half the frequency of the HCCD clocks.

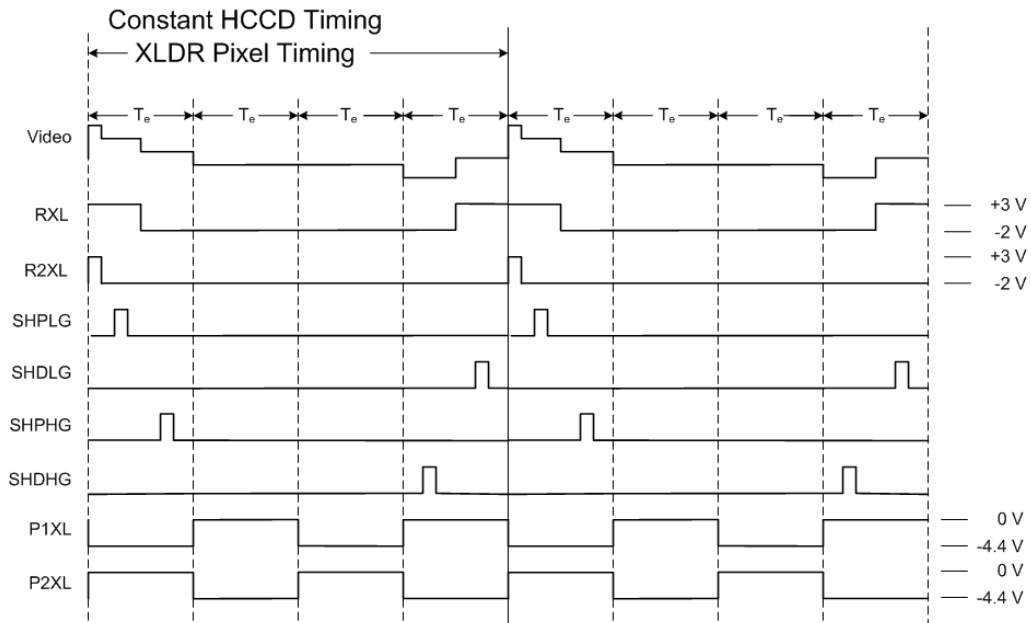


NOTE: See Table 24 center columns for pin assignments.

**Figure 37. 1/4 Resolution Low Gain Pixel Timing**

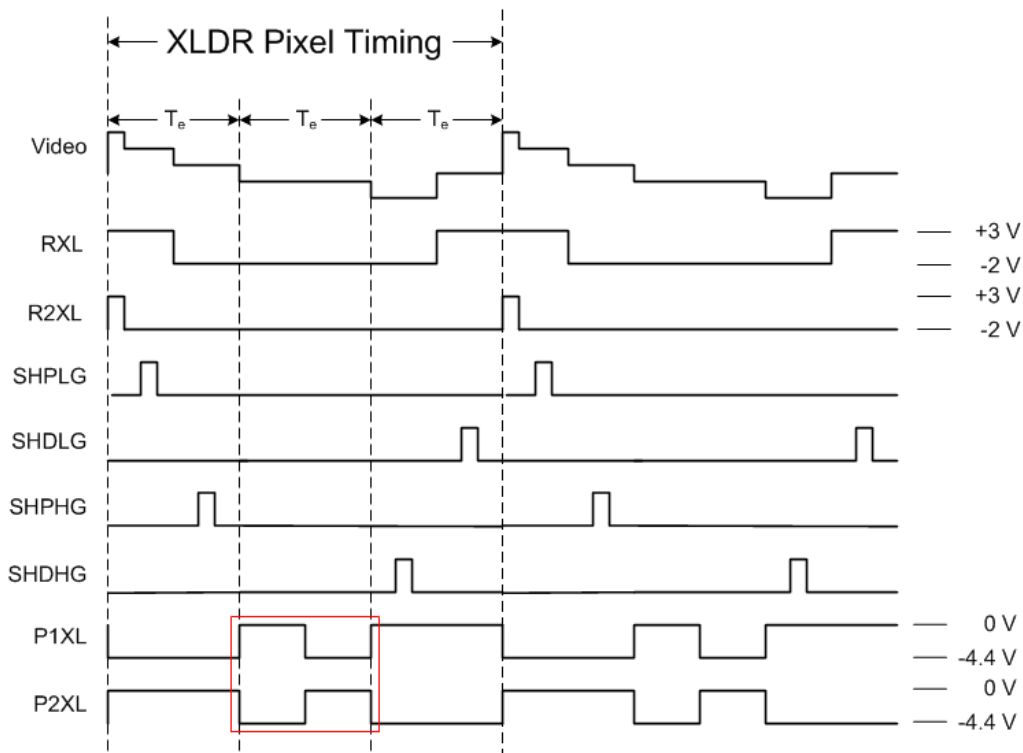
Use this timing to read out every pixel at low gain. If the sensor is to be permanently operated at low gain, the Ra, Rb, Rc, and Rd pins can be set to any DC voltage between +3 V and +5 V. The SHPQ and SHDQ pulses indicate where the camera electronics should sample the video waveform. The SHPQ and SHDQ pulses are not applied to the image sensor.

The R2ab, and R2cd pins are pulsed at half the frequency of the HCCD clocks. This causes two pixels to be summed on the output amplifier sense node. The SHPQ and SHDQ clocks are also half the frequency of the HCCD clocks.



NOTE: See Table 24 right columns for pin assignments.

**Figure 38. XLDR Timing with Constant HCCD. Operating at 20 MHz**



NOTE: See Table 24 right columns for pin assignments.

**Figure 39. XLDR Timing with Variable HCCD Clocking**

Use this pixel timing to operate the image sensor in the extended linear dynamic range mode (XLDR). This mode requires two sets of analog front end (AFE) signal processing electronics for each output. As shown in

Figure 39, one AFE samples the pixel at low gain (SHPLG and SHDLG) and the other AFE samples the pixel at high gain (SHPHG and SHDHG).

Two HCCD pixels are summed on the output amplifier to obtain enough charge to fully use the 82 dB dynamic range of the XLDR timing. Combined with two-line VCCD summing, a total of 160,000 electrons of signal (4x 40,000) can be sampled with 12 electrons or less noise. 82 dB linear dynamic range is very large. Make certain the camera optics is capable of focusing an 82 dB dynamic range image on the

sensor. Lens flare caused by inexpensive optics or even dust on the lens will limit the dynamic range.

This timing shows the HCCD in Figure 39, not being clocked at a constant frequency. If this is a problem for the HCCD timing generator, then the HCCD may be clocked at a constant frequency at the expense of about 33% slower frame rate.

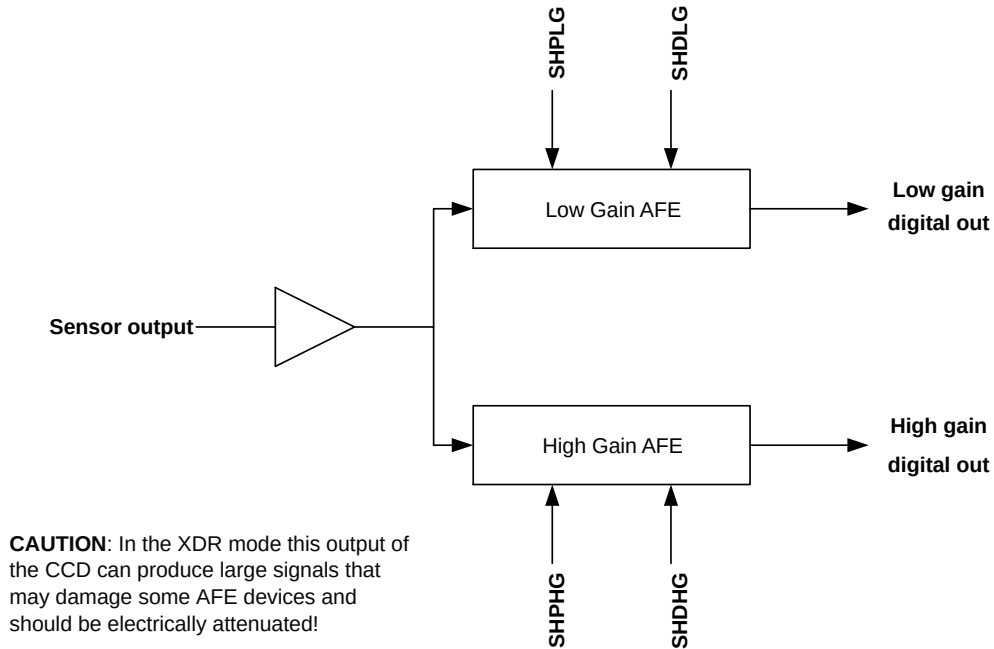


Figure 40. Block Diagram Showing the AFE Connections for XLDR Timing

#### VCCD Clock Rise and Fall Time

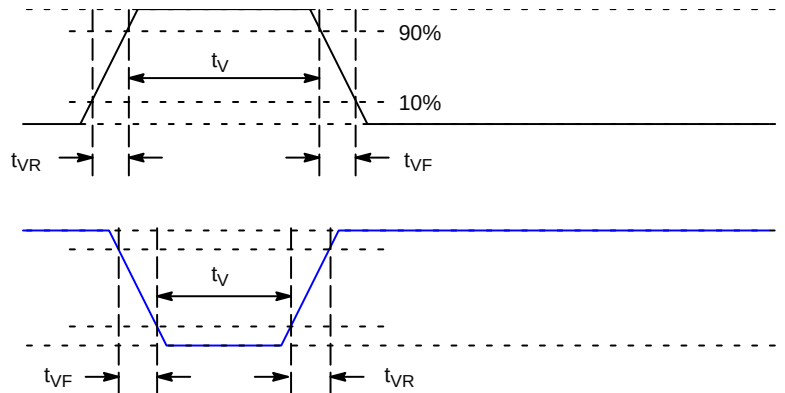
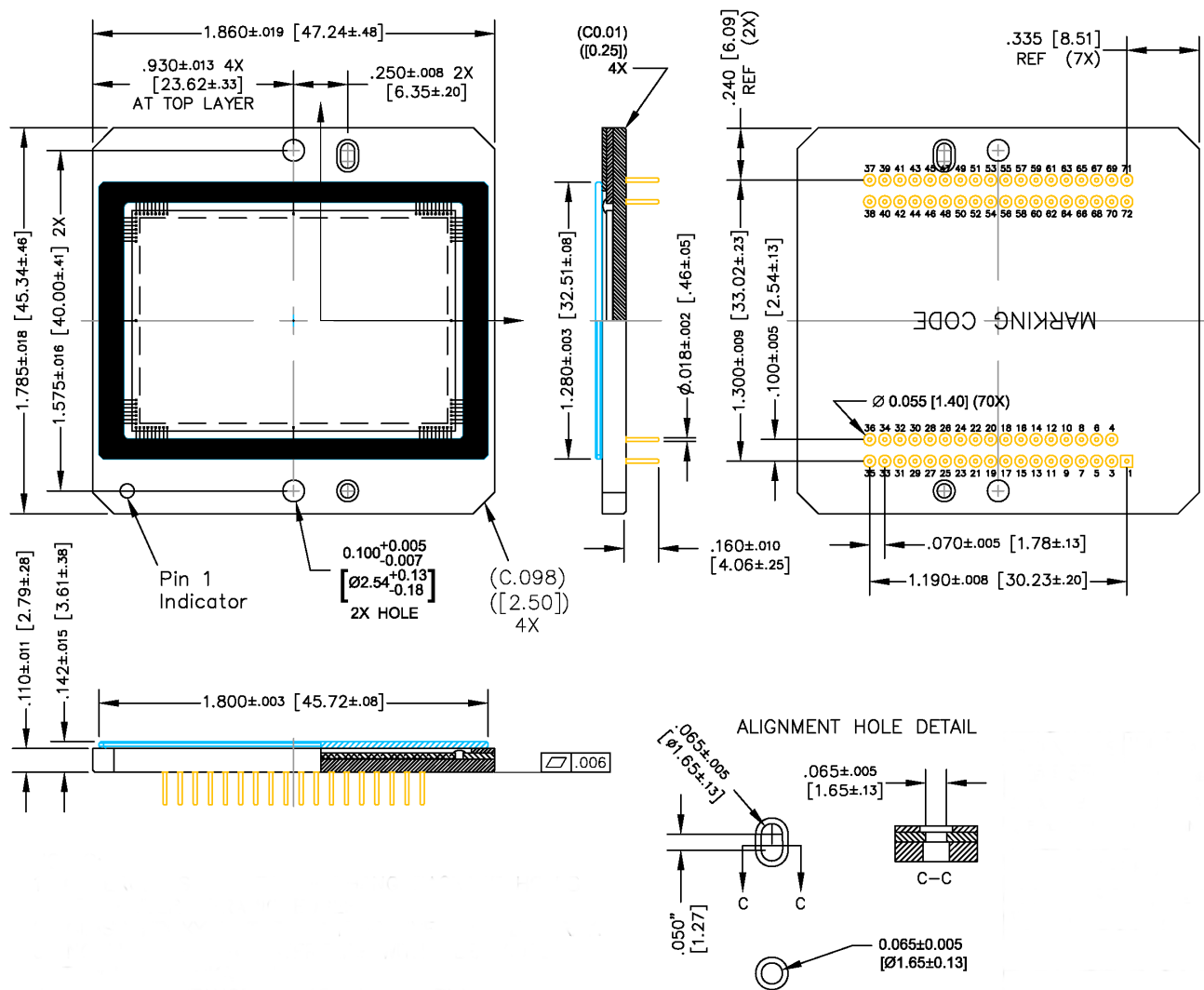


Figure 41. VCCD Clock Rise Time and Fall Time

## MECHANICAL INFORMATION

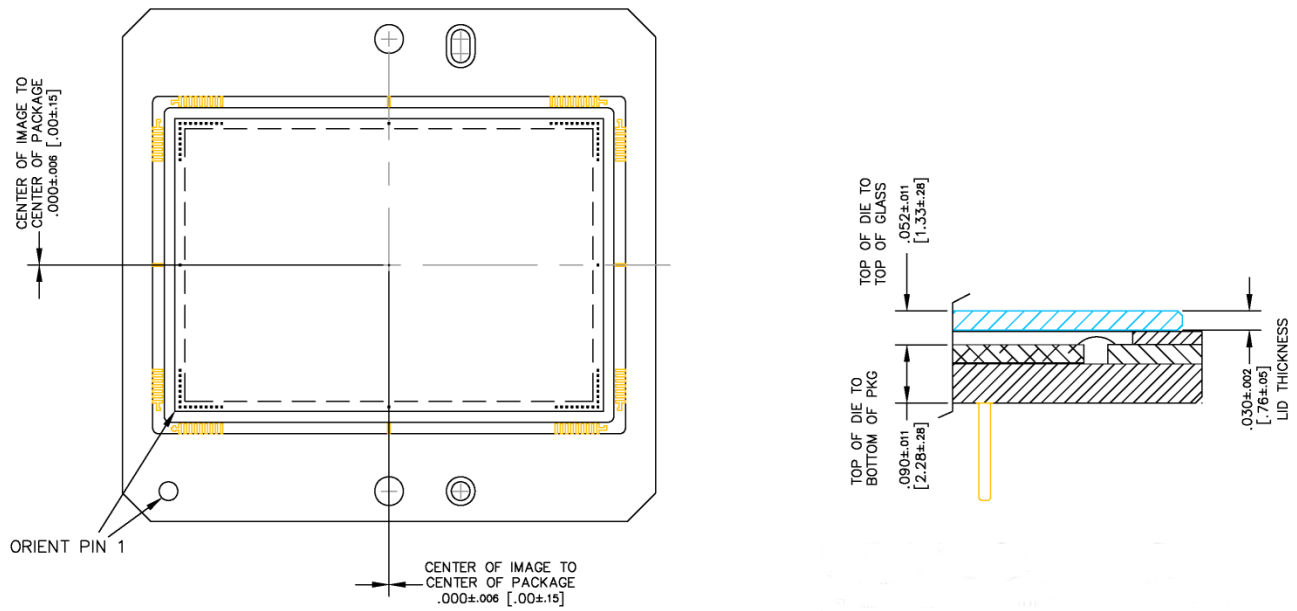
## Completed Assembly



## Notes:

1. See Ordering Information for marking code.
2. Cover glass not to overhang package holes or outer ceramic edges.
3. Glass epoxy not to extend over image array.
4. No materials to interfere with clearance through package holes.
5. Units: IN [MM]

Figure 42. Completed Assembly of Sealed Cover Glass Configuration (1 of 2)



Notes:  
1. Units IN [MM]

Figure 43. Completed Assembly of Sealed Cover Glass Configuration (2 of 2)

SHOWN WITH TAPED-ON COVER GLASS

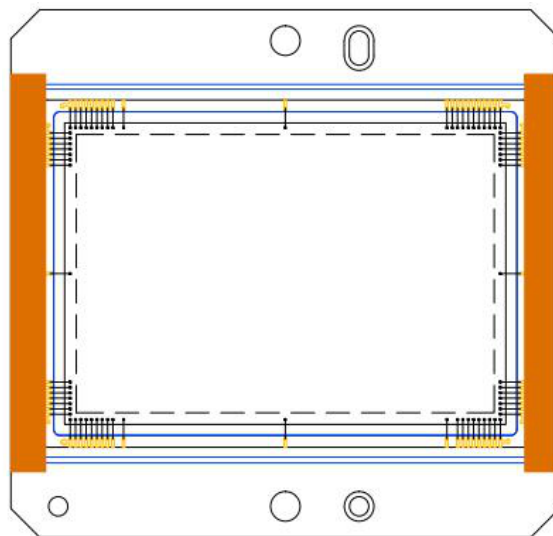
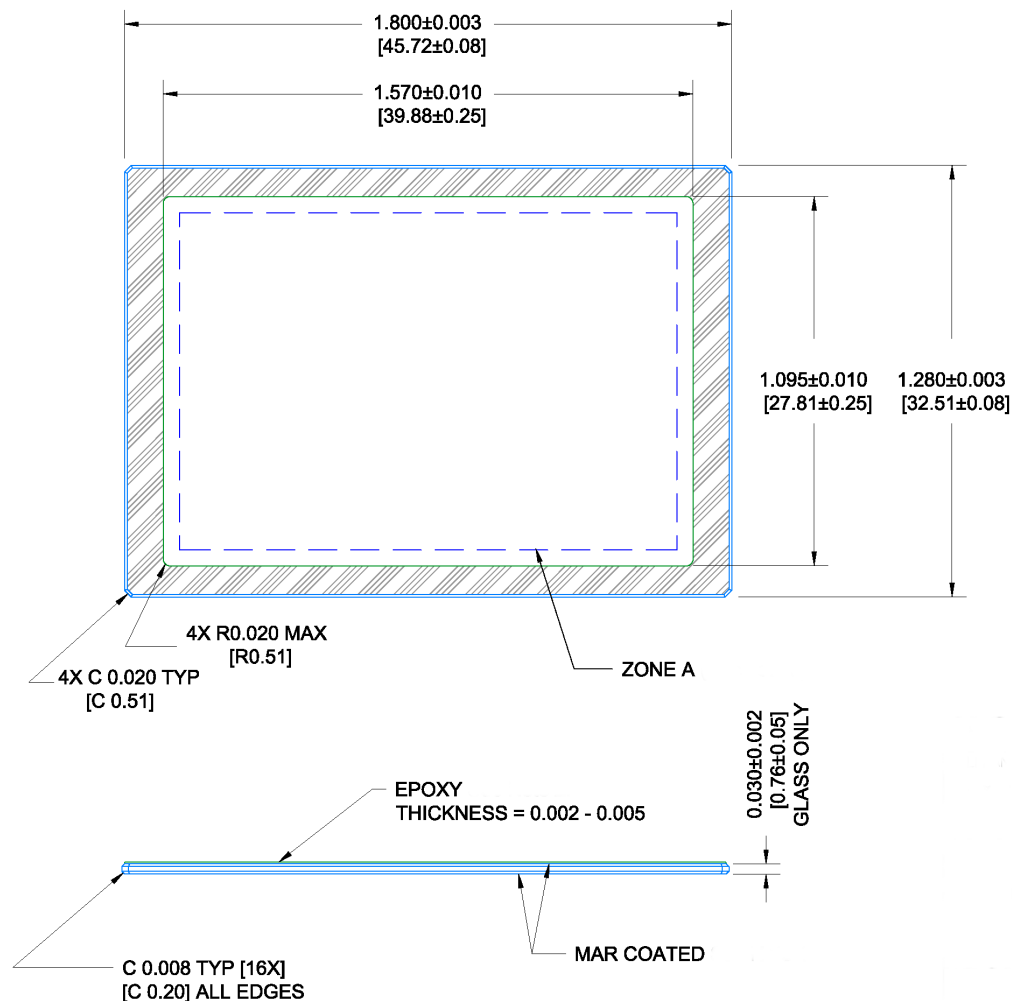


Figure 44. Completed Assembly View of Taped Cover Glass Configuration

## Cover Glass, AR Coated, 2 Sides



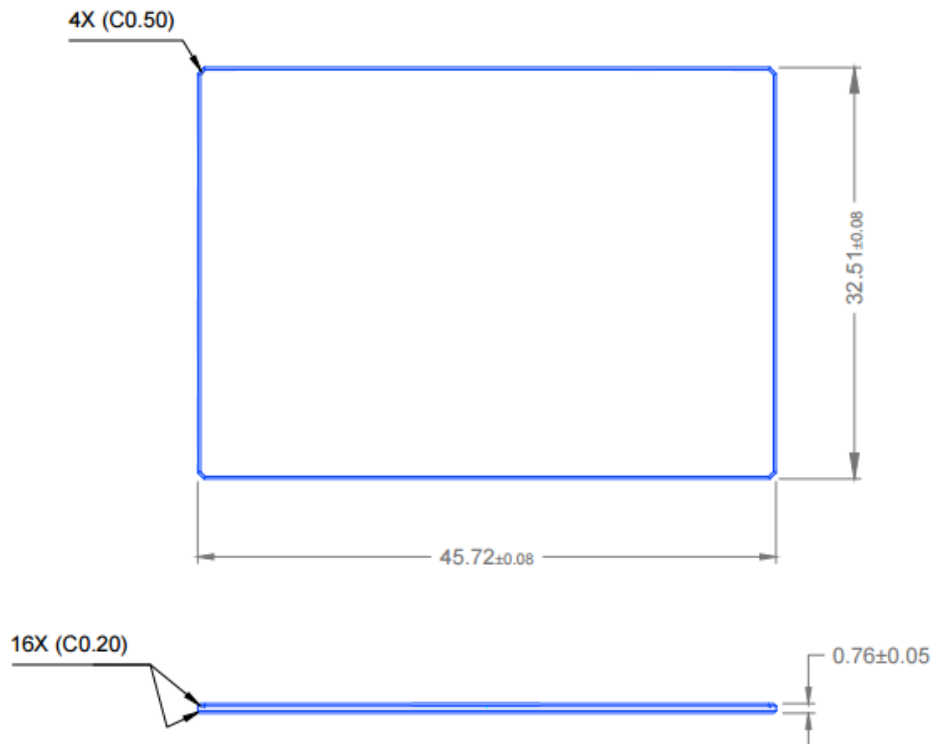
## Notes:

1. Substrate = Schott D263T eco
2. Dust, Scratch, Inclusion Specification:
  - a.) 20  $\mu\text{m}$  Max size in Zone A
  - b.) Zone A = 1.474 x 1.000 [16.43 x 10.08] Centered
3. MAR coated both sides
4. Spectral Transmission
  - a.) 350 – 365 nm: T  $\geq$  88%
  - b.) 365 – 405 nm: T  $\geq$  94%
  - c.) 405 – 450 nm: T  $\geq$  98%
  - d.) 450 – 650 nm: T  $\geq$  99%
  - e.) 650 – 690 nm: T  $\geq$  98%
  - f.) 690 – 770 nm: T  $\geq$  94%
  - g.) 770 – 870 nm: T  $\geq$  88%
5. Units: IN [MM]

Figure 45. Cover Glass, AR Coated, 2 Sides



Cover Glass, Clear No Coatings (Taped)



Notes:

1. Substrate = Schott D263T eco
2. Dust, Scratch, Inclusion Specification: None
3. No Optical Coatings on this Glass
4. Units: MM

Figure 46. Cover Glass, Clear No Coatings (Taped)

## Cover Glass Transmission

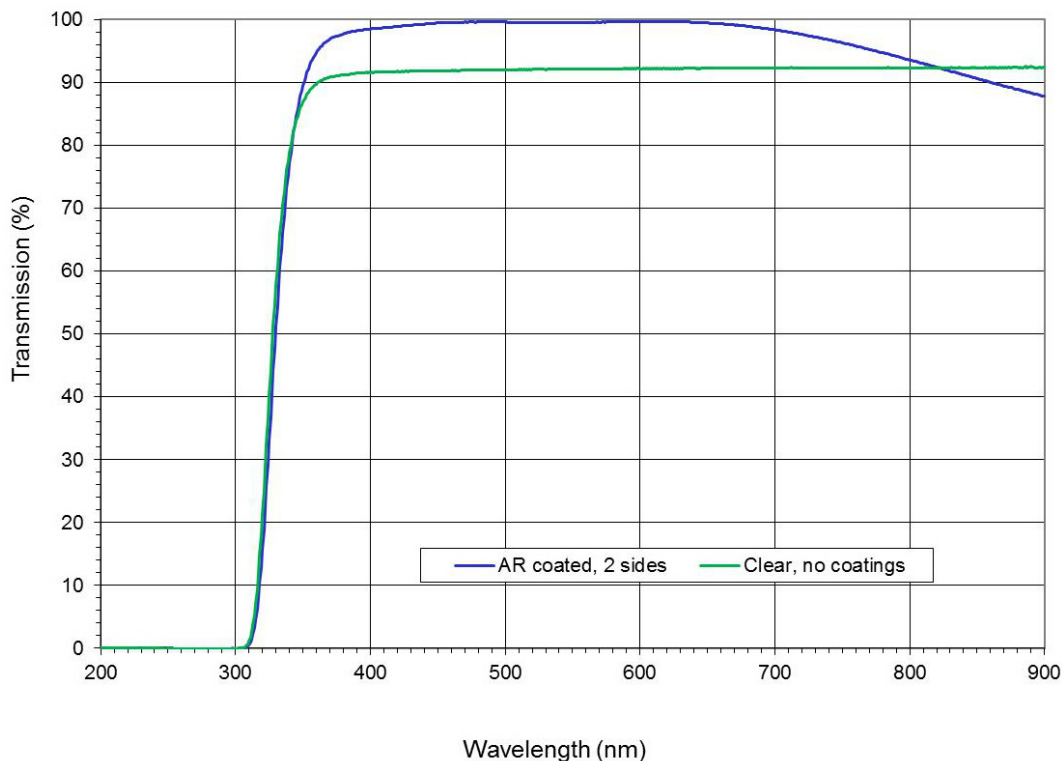


Figure 47. Cover Glass Transmission

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from [www.onsemi.com](http://www.onsemi.com).

For information on soldering recommendations, please download the *Soldering and Mounting Techniques Reference Manual* (SOLDERRM/D) from [www.onsemi.com](http://www.onsemi.com).

For quality and reliability information, please download the *Quality & Reliability Handbook* (HBD851/D) from [www.onsemi.com](http://www.onsemi.com).

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from [www.onsemi.com](http://www.onsemi.com).

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