

Features

- 32 dBm Saturated RF Power
- 41 dBm Output IP3 Linearity
- 17 dB Gain Control
- On-Chip Power Detector
- Lead-Free 4 mm 24-lead PQFN Package
- 100% RF Testing
- RoHS* Compliant and 260°C Reflow Compatible

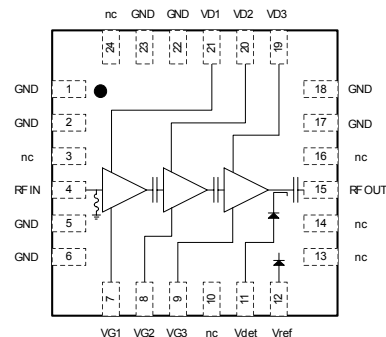
Description

The XP1043-QH is a packaged linear power amplifier that operates over the 12.0-16.0 GHz frequency band. The device provides 21.5 dB gain and 41 dBm Output Third Order Intercept Point (OIP3) across the band and is offered in an industry standard, fully molded 4x4mm QFN package. The packaged amplifier is comprised of a three stage power amplifier with an integrated, temperature compensated on-chip power detector. The device includes on-chip ESD protection structures and DC by-pass capacitors to ease the implementation and volume assembly of the packaged part. The device is manufactured in GaAs pHEMT device technology with BCB wafer coating to enhance ruggedness and repeatability of performance. This device is specially designed for use in Point-to-Point Radio systems for cellular backhaul applications, and is well suited for other telecom applications such as SATCOM and VSAT.

Ordering Information

| Part Number | Package |
|----------------|-------------------|
| XP1043-QH-0G00 | bulk quantity |
| XP1043-QH-0G0T | tape and reel |
| XP1043-QH-EV1 | evaluation module |

Functional Schematic



Pin Configuration

| Pin No. | Function | Pin No. | Function |
|---------|---------------|---------|---------------|
| 1-2 | Ground | 13-14 | Not Connected |
| 3 | Not Connected | 15 | RF Output |
| 4 | RF Input | 16 | Not Connected |
| 5-6 | Ground | 17-18 | Ground |
| 7 | Gate 1 Bias | 19 | Drain 3 Bias |
| 8 | Gate 2 Bias | 20 | Drain 2 Bias |
| 9 | Gate 3 Bias | 21 | Drain 1 Bias |
| 10 | Not Connected | 22-23 | Ground |
| 11 | Pwr Det | 24 | Not Connected |
| 12 | Pwr Det Ref | | |

Absolute Maximum Ratings^{1,2}

| Parameter | Absolute Max. |
|---------------------------------|-------------------|
| Supply Voltage (Vd1,2,3) | +8.0 V |
| Supply Current (Id1,2,3) | 1500 mA |
| Gate Bias Voltage (Vg1,2,3) | -2.4 V |
| Max Power Dissipation (Pdiss) | 5.5W |
| RF Input Power | +19 dBm |
| Operating Temperature (Ta) | -55 °C to +85 °C |
| Storage Temperature (Tstg) | -65 °C to +150 °C |
| Channel Temperature (Tch) | 165 °C |
| MSL Level (MSL) | MSL3 |
| ESD Min.-Machine Model (MM) | Class A |
| ESD Min.-Human Body Model (HBM) | Class 1A |

- (1) Minimum specifications are set under nominal (typ.) bias conditions. Bias can be adjusted higher to achieve greater linearity and power; however, maximum total power dissipated is specified at 5.5 W
- (2) Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

ADVANCED: Data Sheets contain information regarding a product M/A-COM Technology Solutions is considering for development. Performance is based on target specifications, simulated results, and/or prototype measurements. Commitment to develop is not guaranteed.
PRELIMINARY: Data Sheets contain information regarding a product M/A-COM Technology Solutions has under development. Performance is based on engineering tests. Specifications are typical. Mechanical outline has been fixed. Engineering samples and/or test data may be available. Commitment to produce in volume is not guaranteed.

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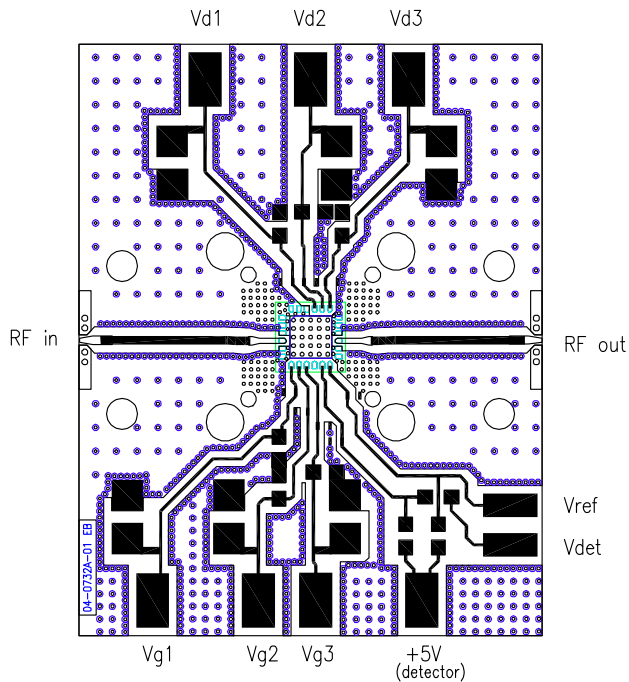
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Electrical Specifications: 12.0-16.0 GHz (Ambient Temperature T = 25°C)

| Parameter | Units | Min. ³ | Typ. | Max. |
|----------------------------------|-------|-------------------|------|------|
| Small Signal Gain (S21) | dB | 19.0 | 21.5 | |
| Input Return Loss (S11) | dB | 10.0 | 15.0 | |
| Output Return Loss (S22) | dB | 10.0 | 10.0 | |
| Reverse Isolation (S12) | dB | | 55.0 | |
| P1dB | dBm | | 30.0 | |
| Psat | dBm | 31.0 | 32.0 | |
| OIP3 at Pout = 18 dBm per Tone | dBm | 40.0 | 41.0 | |
| Power Detector Range | dB | - | 37.0 | - |
| Drain Bias Voltage (Vd1,2,3) | VDC | | 7.0 | 7.0 |
| Detector Bias Voltage (Vdet,ref) | VDC | | 5.0 | |
| Gate Bias Voltage (Vg1,2,3) | VDC | -2 | -1.0 | 0.0 |
| Supply Current (Id1) | mA | | 100 | 200 |
| Supply Current (Id2) | mA | | 200 | 400 |
| Supply Current (Id3) | mA | | 400 | 800 |

3. Minimum specifications are set under nominal (typ.) bias conditions. Bias can be adjusted higher to achieve greater linearity and power.

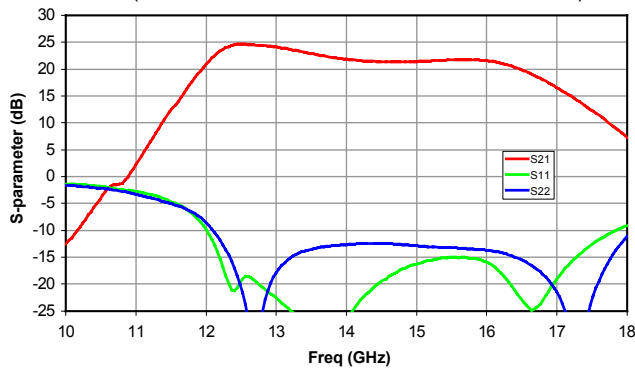
Recommended Layout



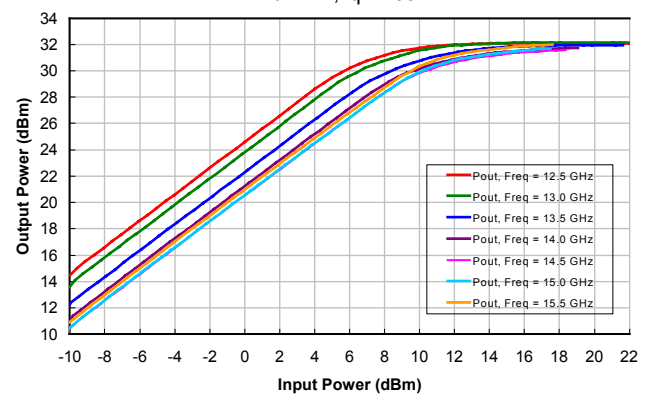
Recommended Decoupling Capacitors: 100pF 0402, 10μF 0805

Typical Performance Curves

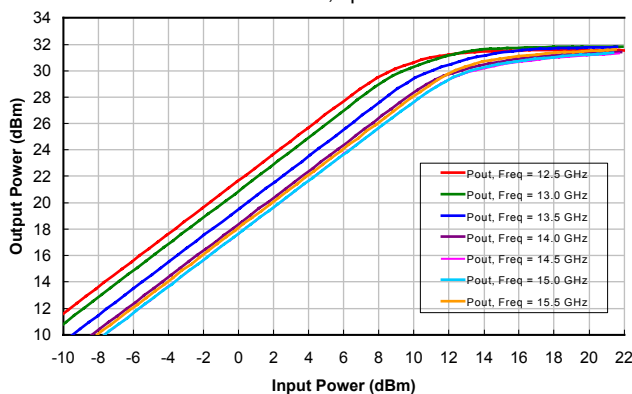
XP1043-QH: S-parameters (dB) vs. Freq (GHz),
(VDD=7V, ID1=100mA, ID2=200mA, ID3=400mA)



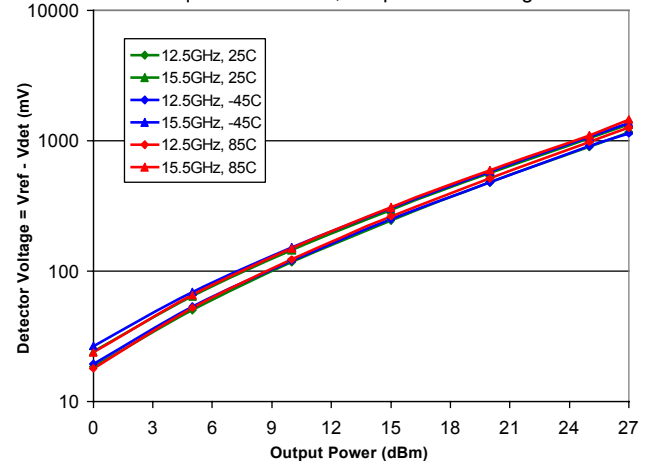
XP1043-QH: Pout (dBm) vs Pin (dBm) at Room Temp.
Vd = 7 V, Iq = 700mA



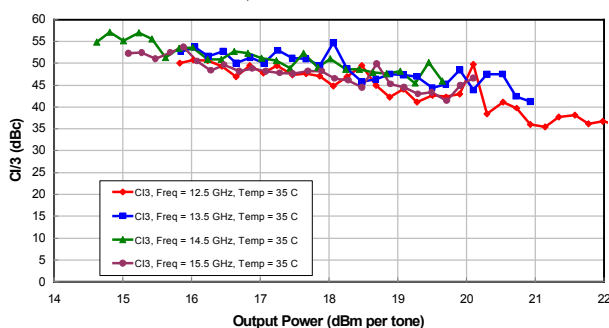
XP1043-QH: Pout (dBm) vs Pin (dBm) at +85 °C.
Vd = 7 V, Iq = 700mA



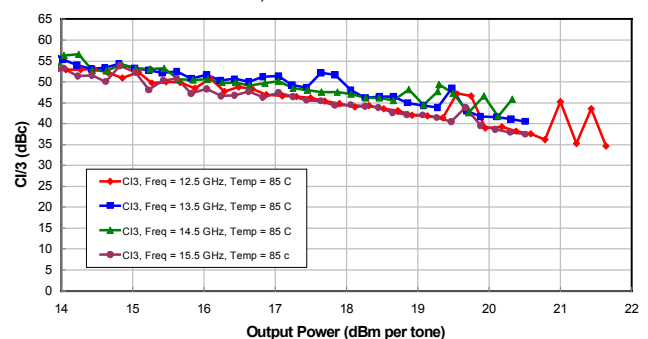
XP1043-QH: V_{Det} (mV) vs Output Power (dBm)
Freq = 12.5-15.5 GHz, Temp = -45 to 85 Degree C



XP1043-QH: C/I3 (dBc) vs Pout per Tone (dBm) at Room Temp.
Vd=7 V, Id=700 mA, 12.5 to 15.5 GHz



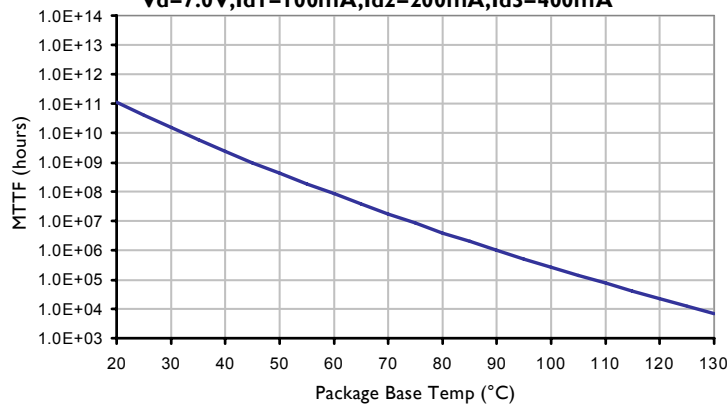
XP1043-QH: C/I3 (dBc) vs Pout per Tone (dBm) at +85 °C.
Vd=7 V, Id=700 mA, 12.5 to 15.5 GHz



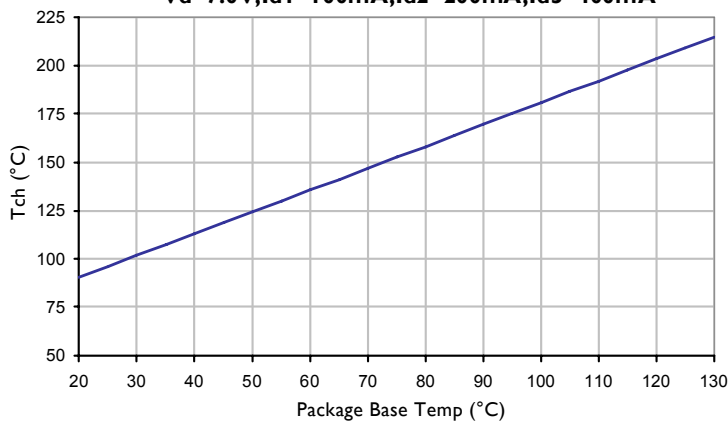
MTTF

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.

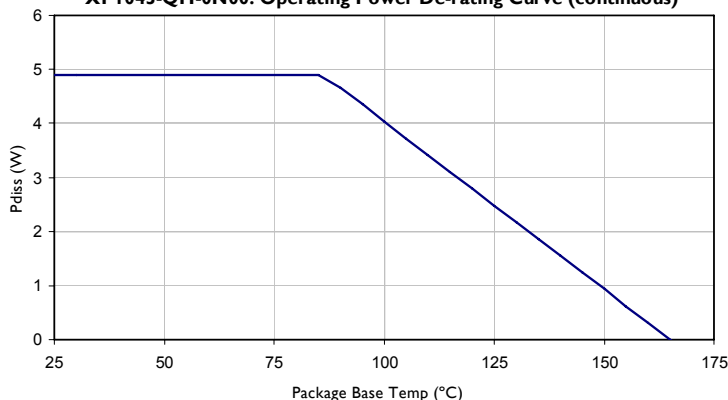
XP1043-QH-0G00: MTTF hours vs Package Base Temperature
Vd=7.0V, Id1=100mA, Id2=200mA, Id3=400mA



XP1043-QH-0G00: Tch vs Package Base Temperature
Vd=7.0V, Id1=100mA, Id2=200mA, Id3=400mA



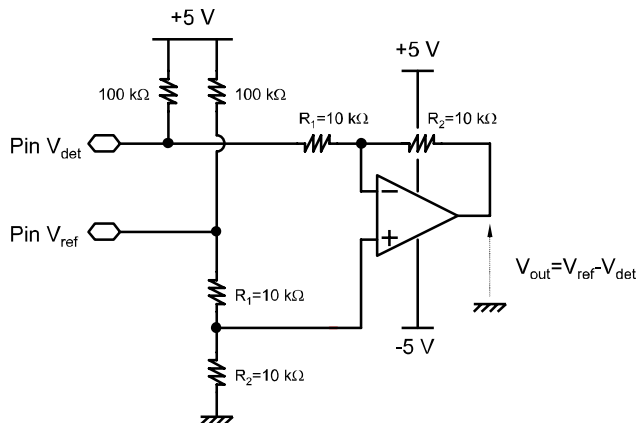
XP1043-QH-0N00: Operating Power De-rating Curve (continuous)



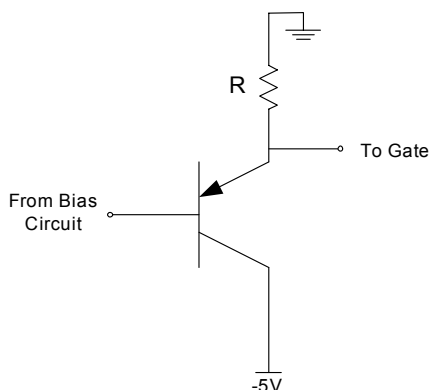
App Note [1] Biasing - As shown in the Pin Designations table, the device is operated under the nominal bias conditions of VD1,2,3 at 7.0V with 100, 200, 400mA respectively. The device can also be safely biased to a maximum of 9 V and 1.4 A to provide greater than 2 Watts of saturated RF power. It is recommended to use active bias to keep the currents constant in order to maintain the best performance over temperature. Under heavy RF saturation the device will tend to self bias and pull the desired drain current. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -1.0V. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Board Layout - As shown in the board layout, it is recommended to provide 100pF decoupling caps as close to the bias pins as possible, with additional 10μF decoupling caps.

App Note [3] Power Detector - As shown in the schematic below, the power detector is implemented by providing +5V bias and measuring the difference in output voltage with standard op-amp in a differential mode configuration.



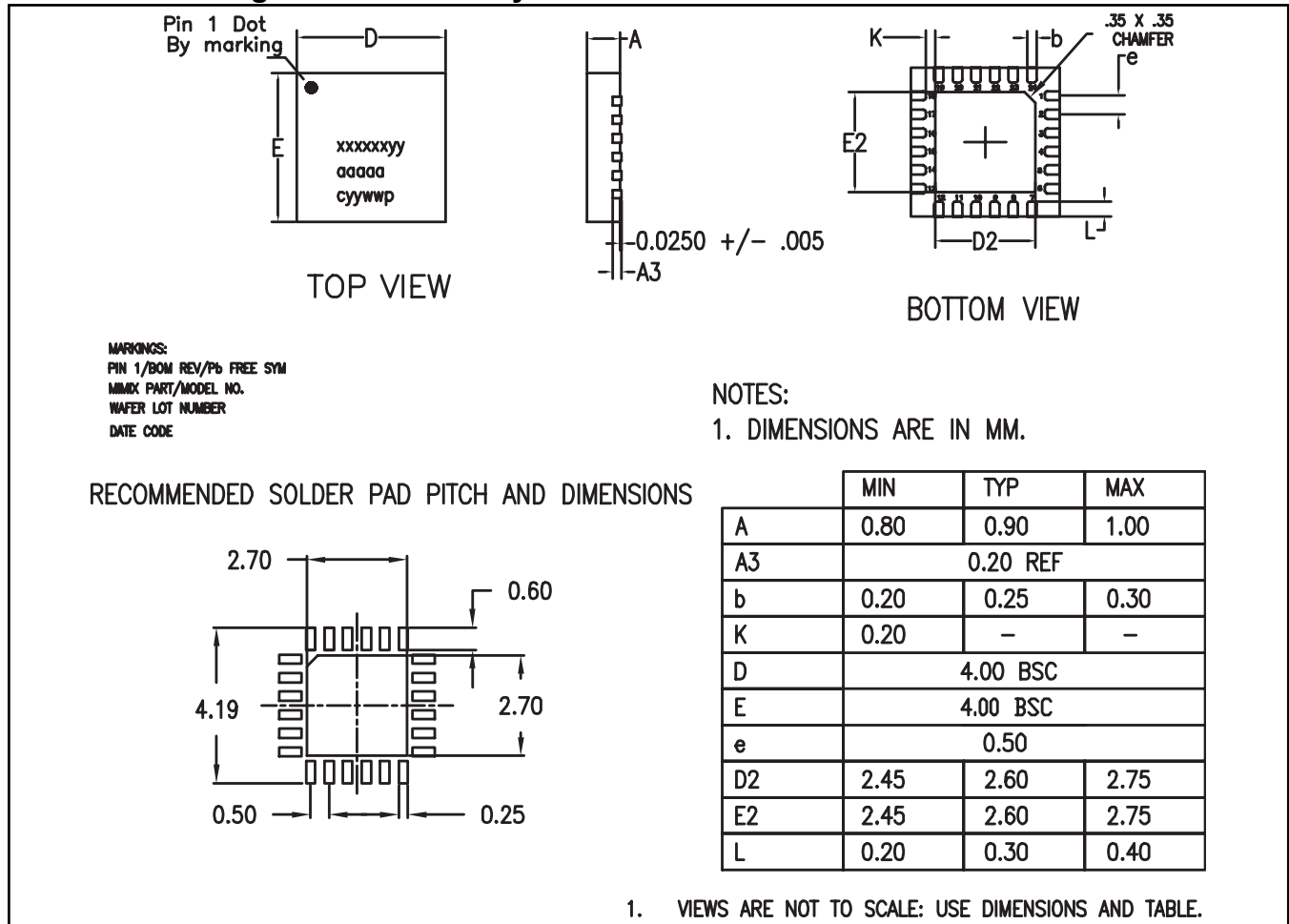
Bias Circuit



The output impedance of the bias circuit's gate output should be small. When in saturation, the gates of the XP1043-QH can draw several mA which may cause adverse affects in a gate circuit with high output impedance. It is recommended that an Emitter Follower circuit be used (shown above), which follows the bias circuit's gate output. This will result in a high-input impedance, low-output impedance buffer between the gate output of the bias circuit and the gate input of the XP1043-QH.

Emitter Follower placed between the
(gate) output of the bias circuit MMIC gate

Lead-Free Package Dimensions/Layout



Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.