TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (U-MOSⅣ)

TPCC8009

Lithium Ion Battery Applications
Notebook PC Applications
Portable Equipment Applications

- Small footprint due to a small and thin package
- Low drain-source ON-resistance:
  $R_{DS\ (ON)}$ = 5 mΩ (typ.) (V_{GS} = 10 V)
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 30 V)
- Enhancement mode: V_{th} = 2.0 to 3.0 V (V_{DS} = 10 V, I_D = 0.2 mA)

Absolute Maximum Ratings (Ta = 25°C)

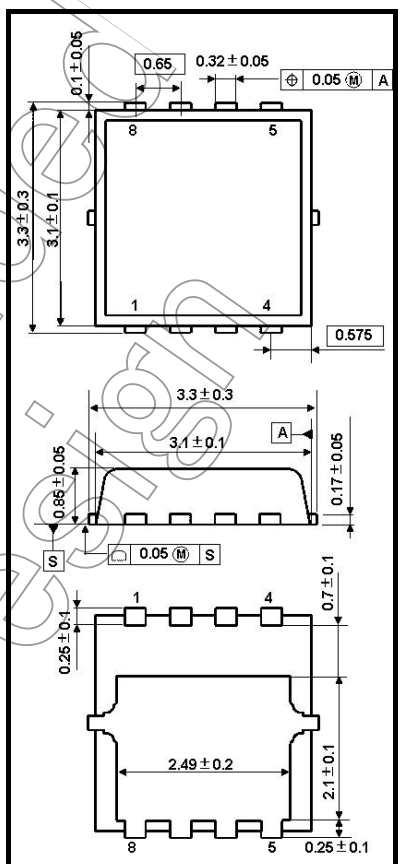
Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	30	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	24	A
	Pulsed (Note 1)	I_{DP}	72	
Drain power dissipation (Tc = 25°C)		P_D	27	W
Drain power dissipation (t = 10 s) (Note 2a)		P_D	1.9	W
Drain power dissipation (t = 10 s) (Note 2b)		P_D	0.7	W
Single-pulse avalanche energy (Note 3)		E_{AS}	75	mJ
Avalanche current		I_{AR}	24	A
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: For Notes 1 to 3, refer to the next page.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.

Unit: mm

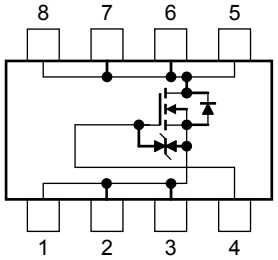


1,2,3:SOURCE 4:GATE
5,6,7,8:DRAIN

JEDEC	—
JEITA	—
TOSHIBA	2-3X1A

Weight: 0.02 g (typ.)

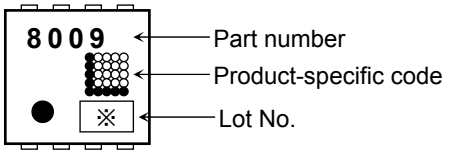
Circuit Configuration



Thermal Characteristics

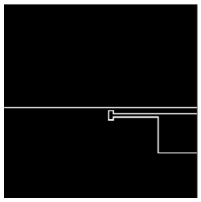
Characteristic	Symbol	Max	Unit
Thermal resistance, channel to case (Tc = 25°C)	$R_{th\ (ch\text{-}c)}$	4.7	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	$R_{th\ (ch\text{-}a)}$	66	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	$R_{th\ (ch\text{-}a)}$	180	°C/W

Marking (Note 4)



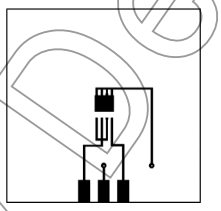
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(a)

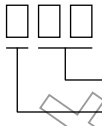


FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(b)

Note 3: V_{DD} = 24 V, T_{ch} = 25°C (initial), L = 100 μH, I_{AR} = 24 A

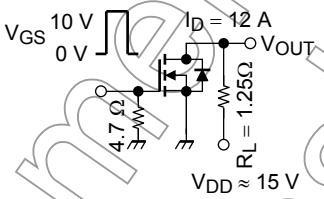
Note 4: * Weekly code: (Three digits)



Week of manufacture
(01 for the first week of the year, continuing up to 52 or 53)

Year of manufacture
(The last digit of the year)

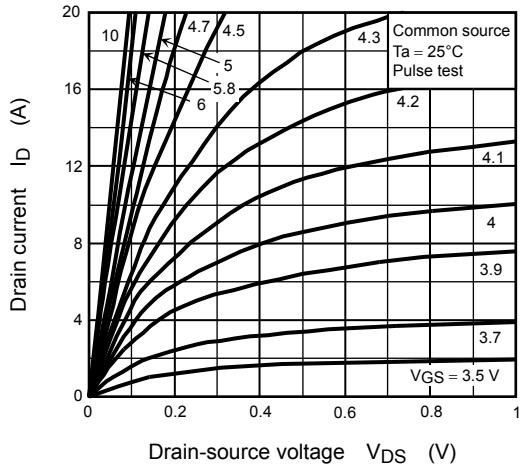
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cutoff current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	30	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −20 V	10	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 0.2 mA	2.0	—	3.0	V
Drain-source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 6 V, I_D = 12 A	—	7.2	11	mΩ
			V_{GS} = 10 V, I_D = 12 A	—	5	7	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	1270	—	pF
Reverse transfer capacitance		C_{rss}		—	230	—	
Output capacitance		C_{oss}		—	360	—	
Switching time	Rise time	t_r		—	6	—	ns
	Turn-on time	t_{on}		—	13	—	
	Fall time	t_f		—	6	—	
	Turn-off time	t_{off}		—	23	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 24 V, V_{GS} = 10 V, I_D = 24 A	—	26	—	nC
Gate-source charge 1		Q_{gs1}		—	5	—	
Gate-drain (“Miller”) charge		Q_{gd}		—	8.2	—	

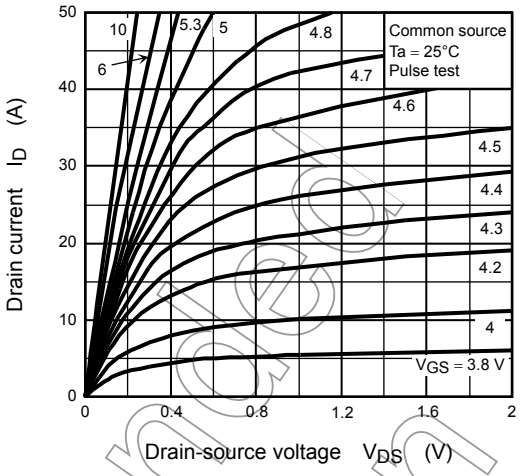
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	72	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 24 A, V_{GS} = 0 V	—	—	−1.2	V

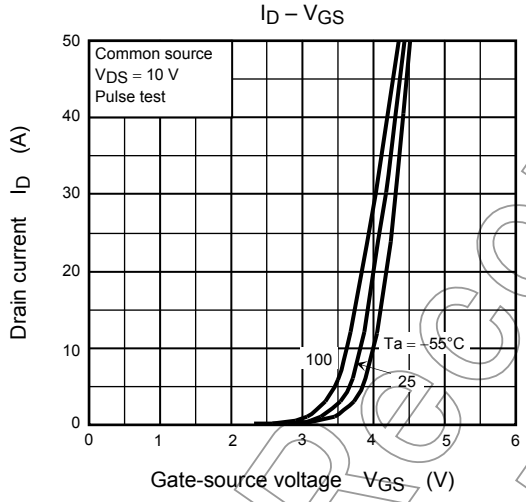
$I_D - V_{DS}$



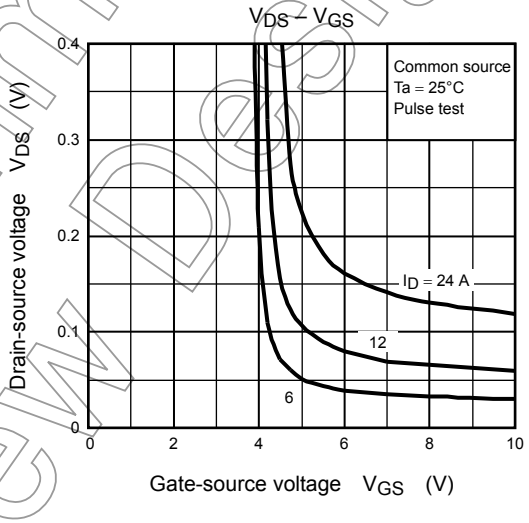
$I_D - V_{DS}$



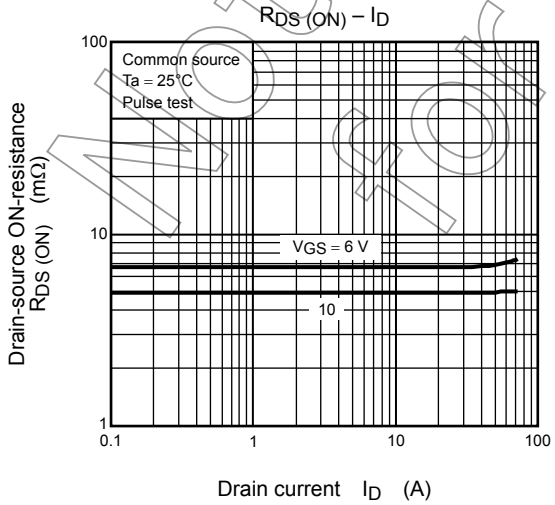
$I_D - V_{GS}$



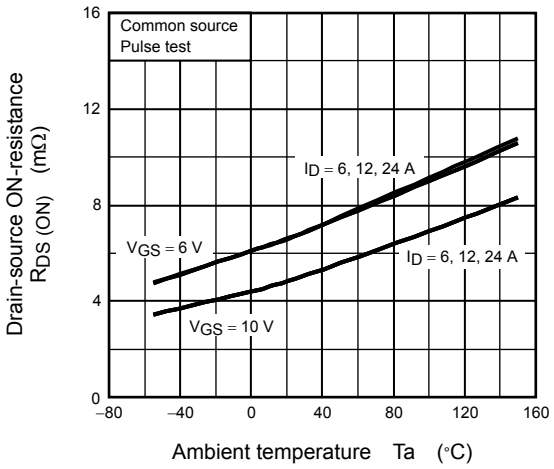
$V_{DS} - V_{GS}$



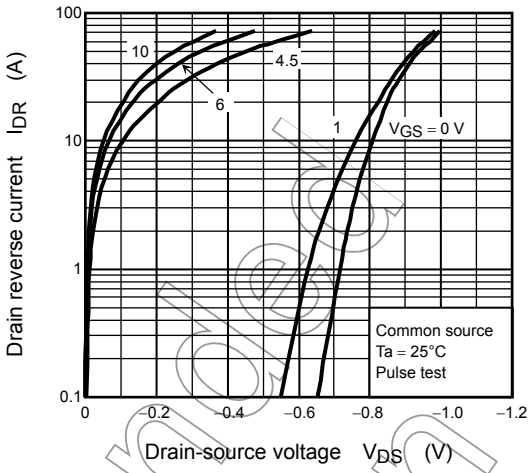
$R_{DS\ (ON)} - I_D$



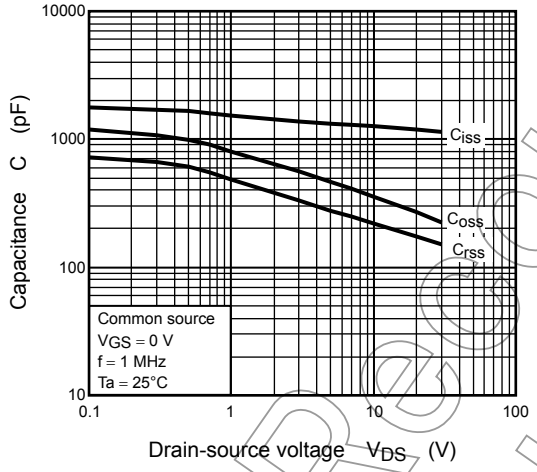
$R_{DS\ (ON)}$ – Ta



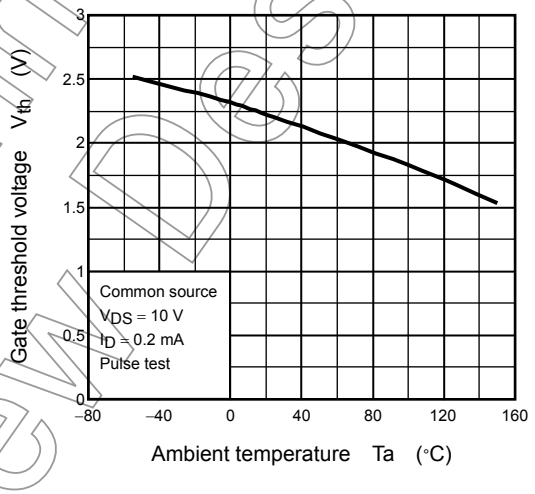
I_{DR} – V_{DS}



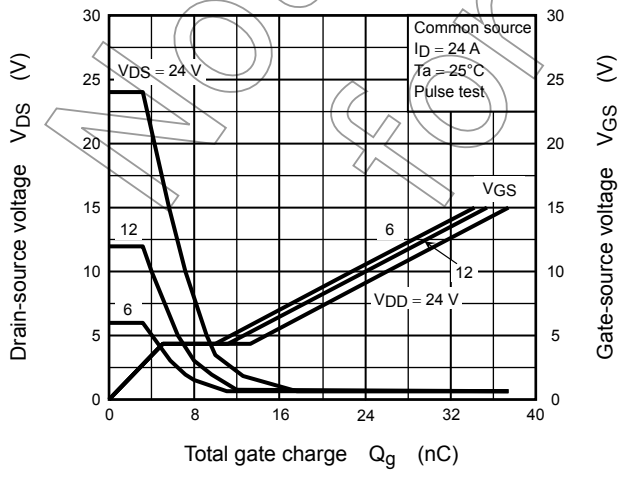
Capacitance – V_{DS}



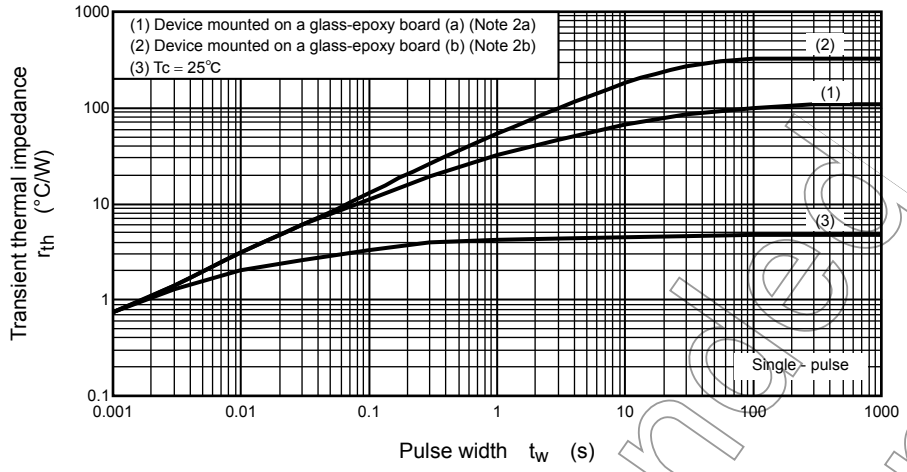
V_{th} – Ta



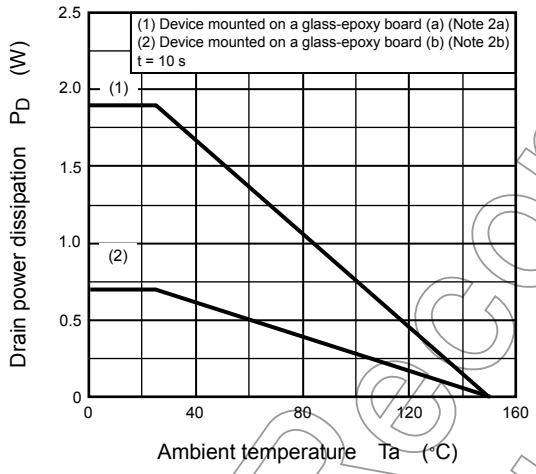
Dynamic input/output characteristics



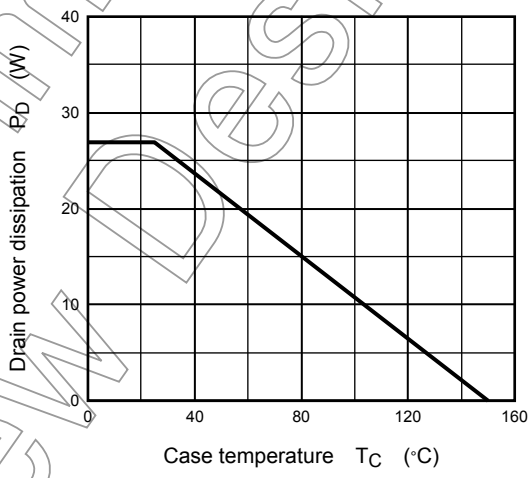
$r_{th} - t_w$



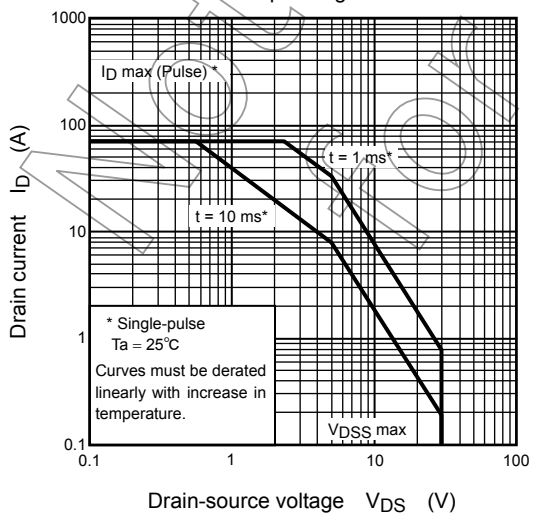
$P_D - Ta$



$P_D - Tc$



Safe operating area



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