Revision History

Revision 0.1 (28 Apr. 2006)

- Original

Revision 1.0 (07 Jun. 2006)

- Delete Preliminary at ever page

- Revise typing error of page1

Revision 1.1 (09 May. 2007)

- Modify P_D, DC specifications and MRS

Revision 1.2 (12 Jun. 2007)

- Modify tDQSS

Revision 1.3 (13 Jul. 2007)

- Add -4 speed grade

DDR SDRAM

4M x 16 Bit x 4 Banks Double Data Rate SDRAM

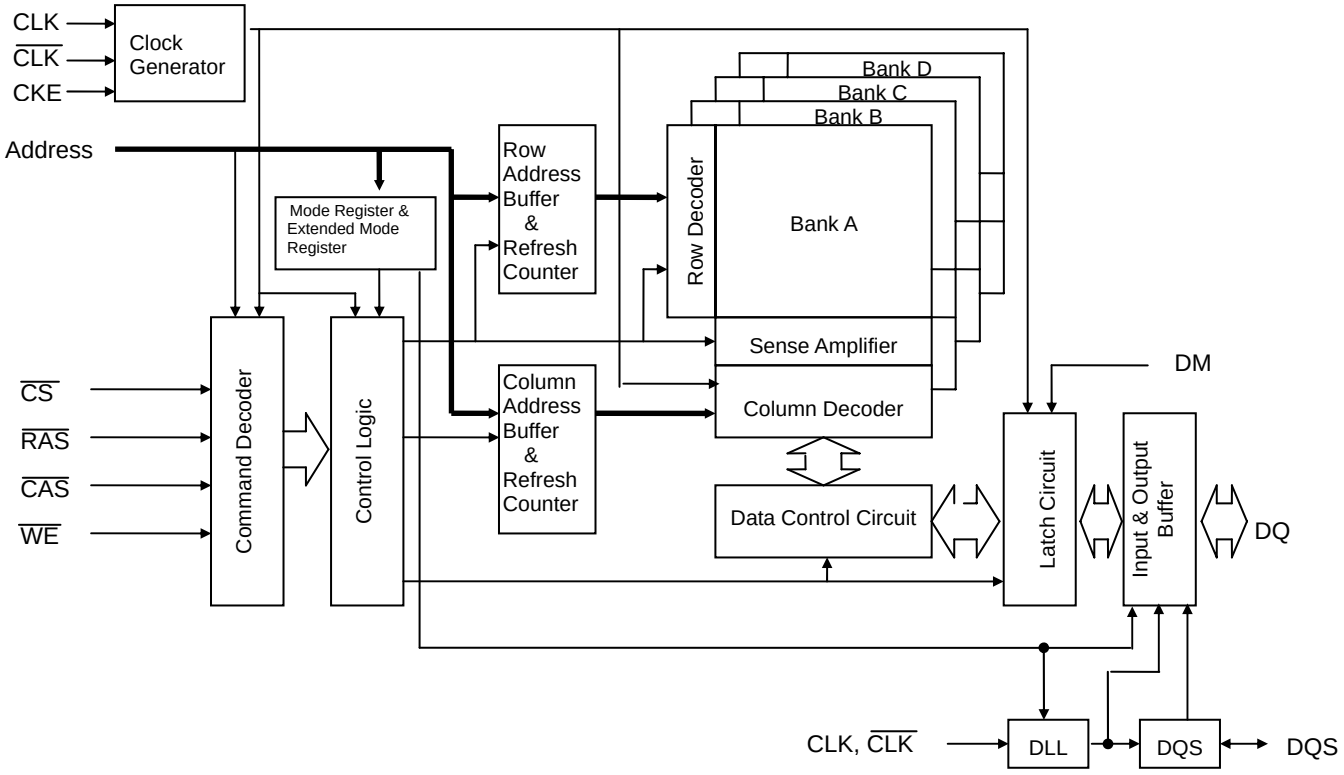
Features

- JEDEC Standard
- Internal pipelined double-data-rate architecture, two data access per clock cycle
- Bi-directional data strobe (DQS)
- On-chip DLL
- Differential clock inputs (CLK and $\overline{CLK}$)
- DLL aligns DQ and DQS transition with CLK transition
- Quad bank operation
- CAS Latency : 2; 2.5; 3
- Burst Type : Sequential and Interleave
- Burst Length : 2, 4, 8
- All inputs except data & DM are sampled at the rising edge of the system clock(CLK)
- Data I/O transitions on both edges of data strobe (DQS)
- DQS is edge-aligned with data for reads; center-aligned with data for WRITE
- Data mask (DM) for write masking only
- V_{DD} = 2.3V ~ 2.7V, V_{DDQ} = 2.3V ~ 2.7V
- V_{DD} = 2.6V ~ 2.8V, V_{DDQ} = 2.6V ~ 2.8V (only for speed -4)
- Auto & Self refresh
- 7.8us refresh interval
- SSTL-2 I/O interface
- 66pin TSOPII package

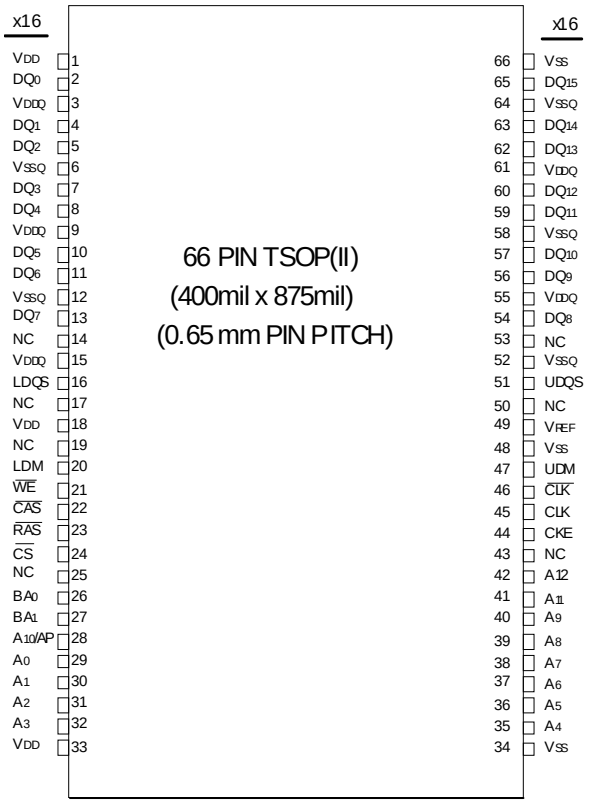
Ordering information :

PRODUCT NO.	MAX FREQ	VDD	PACKAGE	COMMENTS
M13S2561616A -4TG	250MHz	2.7V	TSOPII	Pb-free
M13S2561616A -5TG	200MHz	2.5V	TSOPII	Pb-free
M13S2561616A -6TG	166MHz			Pb-free

Functional Block Diagram



Pin Arrangement



Pin Description

Pin Name	Function	Pin Name	Function
A0~A12, BA0,BA1	Address inputs - Row address A0~A12 - Column address A0~A8 A10/AP : AUTO Precharge BA0, BA1 : Bank selects (4 Banks)	LDM, UDM	DM is an input mask signal for write data. LDM corresponds to the data on DQ0~DQ7; UDM correspond to the data on DQ8~DQ15.
DQ0~DQ15	Data-in/Data-out	CLK, $\overline{CLK}$	Clock input
$\overline{RAS}$	Row address strobe	CKE	Clock enable
$\overline{CAS}$	Column address strobe	$\overline{CS}$	Chip select
$\overline{WE}$	Write enable	V_{DDQ}	Supply Voltage for GDQ
V_{SS}	Ground	V_{SSQ}	Ground for DQ
V_{DD}	Power	V_{REF}	Reference Voltage for SSTL-2
LDQS, UDQS	Bi-directional Data Strobe. LDQS corresponds to the data on DQ0~DQ7; UDQS correspond to the data on DQ8~DQ15.	NC	No connection

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.5 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1500	mW
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operation Condition & Specifications

DC Operation Condition

Recommended operating conditions (Voltage reference to V_{SS} = 0V, T_A = 0 to 70 °C)

Parameter	Symbol	Min		Max		Unit	Note
		-4	-5/6	-4	-5/6		
Supply voltage	V_{DD}	2.6	2.3	2.8	2.7	V	
I/O Supply voltage	V_{DDQ}	2.6	2.3	2.8	2.7	V	
I/O Reference voltage	V_{REF}	0.49*V_{DDQ}		0.51*V_{DDQ}		V	1
I/O Termination voltage (system)	V_{TT}	V_{REF} - 0.04		V_{REF} + 0.04		V	2
Input logic high voltage	V_{IH} (DC)	V_{REF} + 0.15		V_{DDQ} + 0.3		V	
Input logic low voltage	V_{IL} (DC)	-0.3		V_{REF} - 0.15		V	
Input Voltage Level, CLK and $\overline{CLK}$ inputs	V_{IN} (DC)	-0.3		V_{DDQ} + 0.3		V	
Input Differential Voltage, CLK and $\overline{CLK}$ inputs	V_{ID} (DC)	0.36		V_{DDQ} + 0.6		V	
Input leakage current	I_I	-5		5		μA	3
Output leakage current	I_{OZ}	-5		5		μA	
Output High Current (Normal strength driver) (V_{OUT} =V_{DDQ}-0.373V, min V_{REF}, min V_{TT})	I_{OH}	-16.8				mA	
Output Low Current (Normal strength driver) (V_{OUT} = 0.373V)	I_{OL}	+16.8				mA	

Notes 1. V_{REF} is expected to be equal to 0.5* V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.

2. V_{TT} is not applied directly to the device. V_{TT} is system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF} .

3. V_{ID} is the magnitude of the difference between the input level on CLK and the input level on $\overline{CLK}$.

DC Specifications

Parameter	Symbol	Test Condition	Version			Unit	Note
			-4	-5	-6		
Operation Current (One Bank Active)	IDD0	$t_{RC} = t_{RC}$ (min) $t_{CK} = t_{CK}$ (min) Active – Precharge	140	130	120	mA	
Operation Current (One Bank Active)	IDD1	Burst Length = 2 $t_{RC} = t_{RC}$ (min), CL= 2.5 I_{OUT} = 0mA, Active-Read-Precharge	190	185	165	mA	
Precharge Power-down Standby Current	IDD2P	CKE ≤ V_{IL}(max), $t_{CK} = t_{CK}$ (min), All banks idle	40	30	25	mA	
Idle Standby Current	IDD2N	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), $t_{CK} = t_{CK}$ (min)	65	60	55	mA	
Active Power-down Standby Current	IDD3P	All banks ACT, CKE ≤ V_{IL}(max), $t_{CK} = t_{CK}$ (min)	55	50	45	mA	
Active Standby Current	IDD3N	One bank; Active-Precharge, $t_{RC} = t_{RAS}$(max), $t_{CK} = t_{CK}$ (min)	100	95	90	mA	
Operation Current (Read)	IDD4R	Burst Length = 2, CL= 2.5 , $t_{CK} = t_{CK}$ (min), I_{OUT} = 0Ma	300	290	250	mA	
Operation Current (Write)	IDD4W	Burst Length = 2, CL= 2.5 , $t_{CK} = t_{CK}$ (min)	300	290	250	mA	
Auto Refresh Current	IDD5	t_{RC} ≥ t_{RFC}(min)	300	270	250	mA	
Self Refresh Current	IDD6	CKE ≤ 0.2V	5	5	5	mA	1

Note 1. Enable on-chip refresh and address counters.

AC Operation Conditions & Timing Specification

AC Operation Conditions

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V_{IH}(AC)	V_{REF} + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	V_{IL}(AC)		V_{REF} - 0.31	V	
Input Different Voltage, CLK and $\overline{CLK}$ inputs	V_{ID}(AC)	0.7	V_{DDQ}+0.6	V	1
Input Crossing Point Voltage, CLK and $\overline{CLK}$ inputs	V_{IX}(AC)	0.5*V_{DDQ}-0.2	0.5*V_{DDQ}+0.2	V	2

Note1. V_{ID} is the magnitude of the difference between the input level on CLK and the input on $\overline{CLK}$.

2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Input / Output Capacitance

(V_{DD} = 2.3V~2.7V, V_{DDQ} =2.3V~2.7V, T_A = 25 °C , f = 1MHz)

(V_{DD} = 2.6V~2.8V, V_{DDQ} =2.6V~2.8V, T_A = 25 °C , f = 1MHz (only for speed -4))

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A11, BA0~BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN1}	2.0	3.0	pF
Input capacitance (CLK, $\overline{CLK}$)	C_{IN2}	2.0	3.0	pF
Data & DQS input/output capacitance	C_{OUT}	4.0	5.0	pF
Input capacitance (DM)	C_{IN3}	4.0	5.0	pF

AC Operating Test Conditions

Parameter	Value	Unit
Input reference voltage for clock (V_{REF})	0.5*V_{DDQ}	V
Input signal maximum peak swing	1.5	V
Input signal minimum slew rate	1.0	V/ns
Input levels (V_{IH}/V_{IL})	V_{REF}+0.31/V_{REF}-0.31	V
Input timing measurement reference level	V_{REF}	V
Output timing reference level	V_{TT}	V

AC Timing Parameter & Specifications

(V_{DD} = 2.3V~2.7V, V_{DDQ}=2.3V~2.7V, T_A =0℃ ~ 70℃)

(V_{DD} = 2.6V~2.8V, V_{DDQ}=2.6V~2.8V, T_A =0℃ ~70℃ (only for speed -4))

Parameter		Symbol	-4		-5		-6		
			min	max	min	max	min	max	
Clock Period	CL2	t_{CK}	7.5	10	7.5	10	7.5	12	ns
	CL2.5		5	10	5	10	6	12	
	CL3		4.0	10	5.0	10	6.0	10	
Access time from CLK/ $\overline{CLK}$		t_{AC}	-0.75	+0.75	-0.75	+0.75	+0.75	+0.75	ns
CLK high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
CLK low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
Data strobe edge to clock edge		t_{DQSCK}	-0.55	+0.55	-0.55	+0.55	-0.6	+0.6	ns
Clock to first rising edge of DQS delay		t_{DQSS}	0.9	1.1	0.85	1.15	0.85	1.15	t_{CK}
Data-in and DM setup time (to DQS)		t_{DS}	0.6	-	0.6	-	0.6	-	ns
Data-in and DM hold time (to DQS)		t_{DH}	0.45	-	0.45	-	0.45	-	ns
DQ and DM input pulse width (for each input)		t_{DIPW}	1.75	-	1.75	-	1.75	-	ns
Input setup time (fast slew rate)		t_{IS}	0.75	-	0.75	-	0.75	-	ns
Input hold time (fast slew rate)		t_{IH}	0.75	-	0.75	-	0.75	-	ns
Input setup time (slow slew rate)		t_{IS}	0.8	-	0.8	-	0.8	-	ns
Input hold time (slow slew rate)		t_{IH}	0.8	-	0.8	-	0.8	-	ns
Control and Address input pulse width		t_{IPW}	2.2	-	2.2	-	2.2	-	ns
DQS input high pulse width		t_{DQSH}	0.35	-	0.35	-	0.35	-	t_{CK}
DQS input low pulse width		t_{DQSL}	0.35	-	0.35	-	0.35	-	t_{CK}
DQS falling edge to CLK rising-setup time		t_{DSS}	0.2	-	0.2	-	0.2	-	t_{CK}
DQS falling edge from CLK rising-hold time		t_{DSH}	0.2	-	0.2	-	0.2		t_{CK}
Data strobe edge to output data edge		t_{DQSQ}	-	0.40	-	0.40	-	0.45	ns
Data-out high-impedance window from CLK/ $\overline{CLK}$		t_{HZ}	-0.7	+0.7	-0.7	+0.7	-0.7	+0.7	ns
Data-out low-impedance window from CLK/ $\overline{CLK}$		t_{LZ}	-0.7	+0.7	-0.7	+0.7	-0.7	+0.7	ns

AC Timing Parameter & Specifications-continued

Parameter	Symbol	-4		-5		-6		
		min	max	min	max	min	max	ns
Half Clock Period	t_{HP}	t_{CL}min or t_{CH}min	-	t_{CL}min or t_{CH}min	-	t_{CL}min or t_{CH}min	-	ns
DQ-DQS output hold time	t_{QH}	t_{HP}-t_{QHS}	-	t_{HP}-t_{QHS}	-	t_{HP}-t_{QHS}	-	ns
ACTIVE to PRECHARGE command	t_{RAS}	40	70K	40	70K	42	70K	ns
Row Cycle Time	t_{RC}	52	-	55	-	60	-	ns
AUTO REFRESH Row Cycle Time	t_{RFC}	52	-	70	-	72	-	ns
ACTIVE to READ,WRITE delay	t_{RCD}	15	-	15	-	18	-	ns
PRECHARGE command period	t_{RP}	15	-	15	-	18	-	ns
ACTIVE to READ with AUTOPRECHARGE command	t_{RAP}	18	120K	18	120K	18	120K	ns
ACTIVE bank A to ACTIVE bank B command	t_{RRD}	8	-	10	-	12	-	ns
Write recovery time	t_{WR}	15	-	15	-	15	-	t_{CK}
Write data in to READ command delay	t_{WTR}	2	-	2	-	1	-	t_{CK}
Col. Address to Col. Address delay	t_{CCD}	1	-	1	-	1	-	t_{CK}
Average periodic refresh interval	t_{REFI}	-	7.8	-	7.8	-	7.8	us
Write preamble	t_{WPRE}	0.25	-	0.25	-	0.25	-	t_{CK}
Write postamble	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
Clock to DQS write preamble setup time	t_{WPRES}	0	-	0	-	0	-	ns
Load Mode Register / Extended Mode register cycle time	t_{MRD}	2	-	2	-	1	-	t_{CK}
Exit self refresh to READ command	t_{XSRD}	200	-	200	-	200	-	t_{CK}
Exit self refresh to non-READ command	t_{XSNR}	75	-	75	-	75	-	ns
Autoprecharge write recovery+Precharge time	t_{DAL}	30	-	30	-	-	30	ns

Command Truth Table

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	BA0,1	A10/AP	A11,A12, A9~A0	Note
Register	Extended MRS		H	X	L	L	L	L	X	OP CODE			1,2
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address	4
	Auto Precharge Enable										H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address	4
	Auto Precharge Enable										H		4,6
Burst Stop			H	X	L	H	H	L	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DM			H	X					V	X			8
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

1. OP Code: Operand Code. A0~A12 & BA0~BA1 : Program keys. (@EMRS/MRS)
2. EMRS/MRS can be issued only at all banks precharge state.
   A new command can be issued 1 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto"..
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0~BA1 : Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampling at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

Basic Functionality

Power-Up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE at a low state (all other inputs may be undefined.)
   - Apply VDD before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as V_{TT} & V_{REF}).
2. Start clock and maintain stable condition for a minimun of 200us.
3. The minimun of 200us after stable power and clock (CLK, $\overline{CLK}$), apply NOP & take CKE high.
4. Issue precharge commands for all banks of the device.

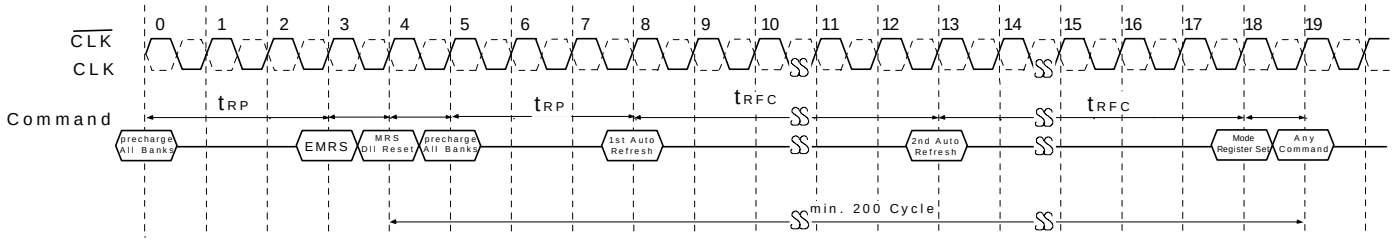
*1 5. Issue EMRS to enable DLL. (To issue “DLL Enable” command, provide “Low” to A0, “High” to BA0 and “Low” to all of the rest address pins, A1~A12 and BA1)

*1 6. Issue a mode register set command for “DLL reset”. The additional 200 cycles of clock input is required to lock the DLL. (To issue DLL reset command, provide “High” to A8 and “Low” to BA0)

*2 7. Issue precharge commands for all banks of the device.
8. Issue 2 or more auto-refresh commands.
9. Issue a mode register set command with low to A8 to initialize device operation.

*1 Every “DLL enable” command resets DLL. Therefore sequence 6 can be skipped during power up. Instead of it, the additional 200 cycles of clock input is required to lock the DLL after enabling DLL.
*2 Sequence of 6 & 7 is regardless of the order.

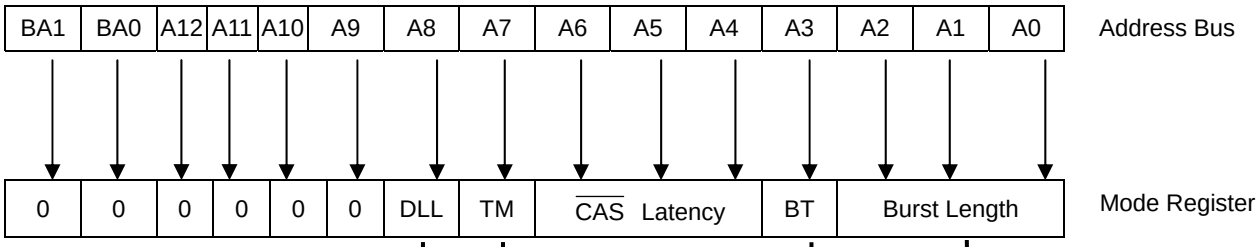
Power up & Initialization Sequence



Mode Register Definition

Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs $\overline{CAS}$ latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the register is not defined, therefore the mode register must be written after EMRS setting for proper DDR SDRAM operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA0 (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register). The state of address pins A0~A12 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA0 going low is written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0~A2, addressing mode uses A3, $\overline{CAS}$ latency (read latency from column address) uses A4~A6. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and $\overline{CAS}$ latencies.



A8	DLL Reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

A3	Burst Type
0	Sequential
1	Interleave

BA1	BA0	Operating Mode
0	0	MRS Cycle
0	1	EMRS Cycle

$\overline{CAS}$ Latency

A6	A5	A4	Latency
0	0	0	Reserve
0	0	1	Reserve
0	1	0	2
0	1	1	3
1	0	0	Reserve
1	0	1	Reserve
1	1	0	2.5
1	1	1	Reserve

Burst Length

A2	A1	A0	Latency	
			Sequential	Interleave
0	0	0	Reserve	Reserve
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Reserve	Reserve

Burst Address Ordering for Burst Length

Burst Length	Starting Address (A2, A1,A0)	Sequential Mode	Interleave Mode
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

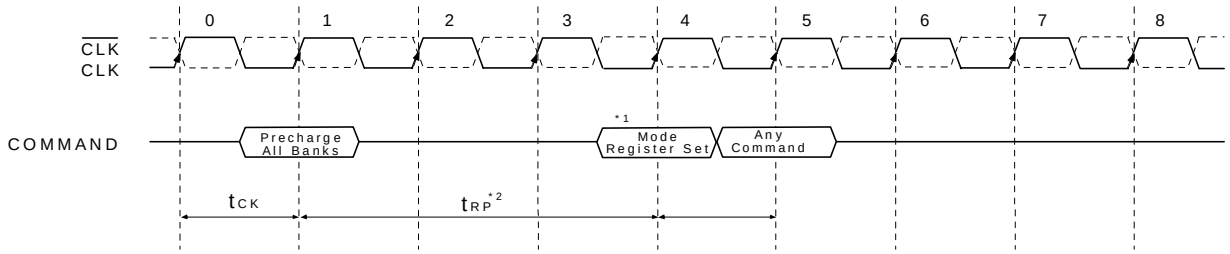
DLL Enable / Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enable automatically). Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. M13S2561616A also support a weak drive strength option, intended for lighter load and/or point-to-point environments.

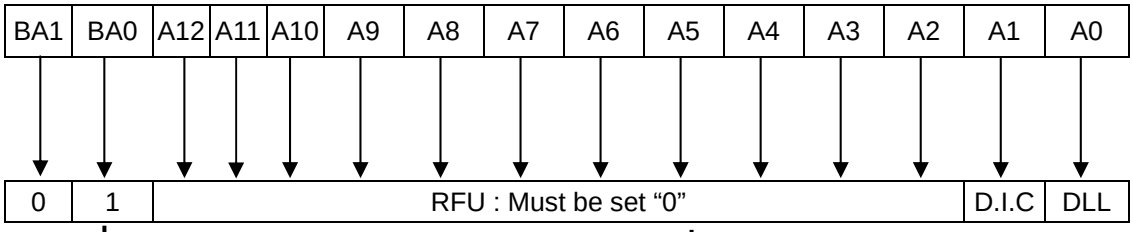
Mode Register Set



*1 : MRS can be issued only at all banks precharge state.
*2 : Minimum t_{RP} is required to issue MRS command.

Extended Mode Register Set (EMRS)

The extended mode register stores the data enabling or disabling DLL. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA0 (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0~A12 and BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. All the other address pins except A0 and BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



BA1	BA0	Operaing Mode
0	0	MRS Cycle
0	1	EMRS Cycle

Output Driver Strength Control	
0	Normal
1	Weak

A0	DLL Enable
0	Enable
1	Disable

*QFC is not used; don't care.

Precharge

The precharge command is used to precharge or close a bank that has activated. The precharge command is issued when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The bank select addresses (BA0, BA1) are used to define which bank is precharged when the command is initiated. For write cycle, t_{WR}(min.) must be satisfied until the precharge command can be issued. After t_{RP} from the precharge, an active command to the same bank can be initiated.

Burst Selection for Precharge by Bank address bits

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

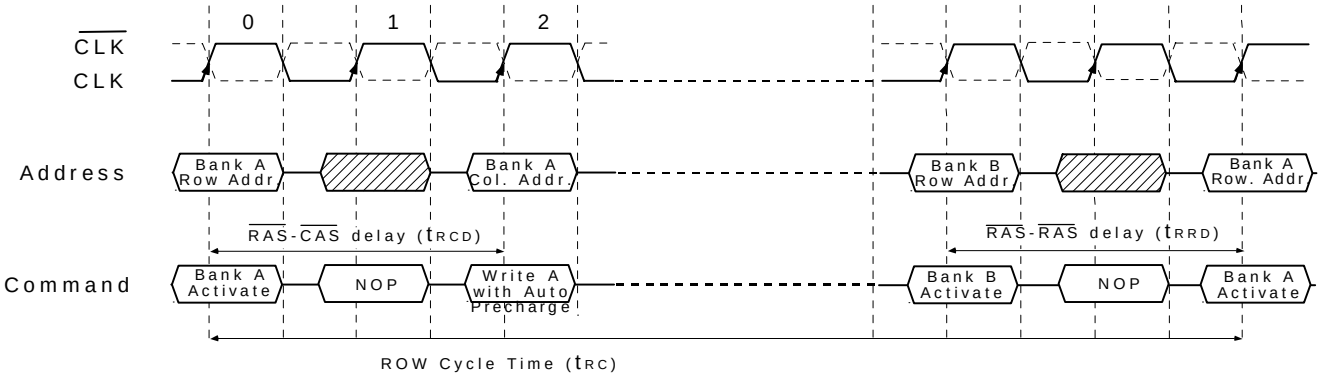
NOP & Device Deselect

The device should be deselected by deactivating the $\overline{CS}$ signal. In this mode DDR SDRAM should ignore all the control inputs. The DDR SDRAMs are put in NOP mode when $\overline{CS}$ is active and by deactivating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. For both Deselect and NOP the device should finish the current operation when this command is issued.

Row Active

The Bank Activation command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock (CLK). The DDR SDRAM has four independent banks, so two Bank Select addresses (BA0, BA1) are required. The Bank Activation command to the first read or write command must meet or exceed the minimum of $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD} min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation command (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD} min).

Bank Activation Command Cycle ($\overline{CAS}$ Latency = 3)



Read Bank

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating $\overline{CS}$, $\overline{CAS}$, and deasserting $\overline{WE}$ at the same clock sampling (rising) edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS command.

Write Bank

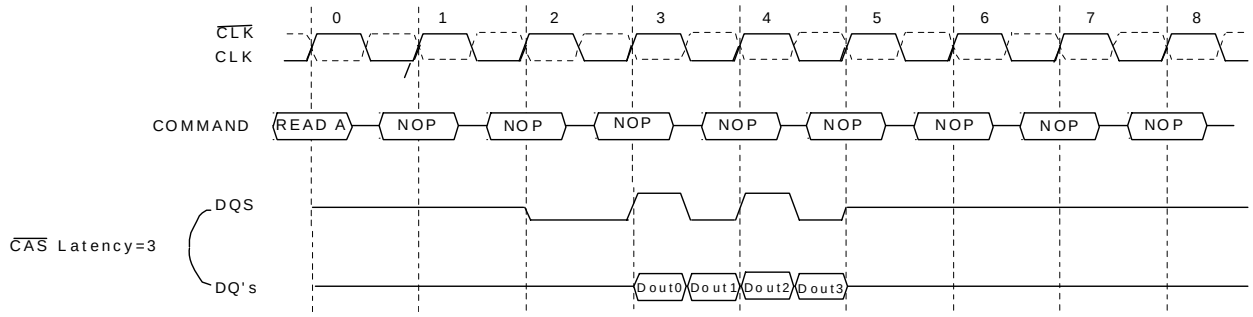
This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ at the same clock sampling (rising) edge as describe in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

Essential Functionality for DDR SDRAM

Burst Read Operation

Burst Read operation in DDR SDRAM is in the same manner as the current SDRAM such that the Burst read command is issued by asserting $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock (CLK) after t_{RCD} from the bank activation. The address inputs determine the starting address for the Burst, The Mode Register sets type of burst (Sequential or interleave) and burst length (2, 4, 8). The first output data is available after the $\overline{CAS}$ Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe (DQS) adopted by DDR SDRAM until the burst length is completed.

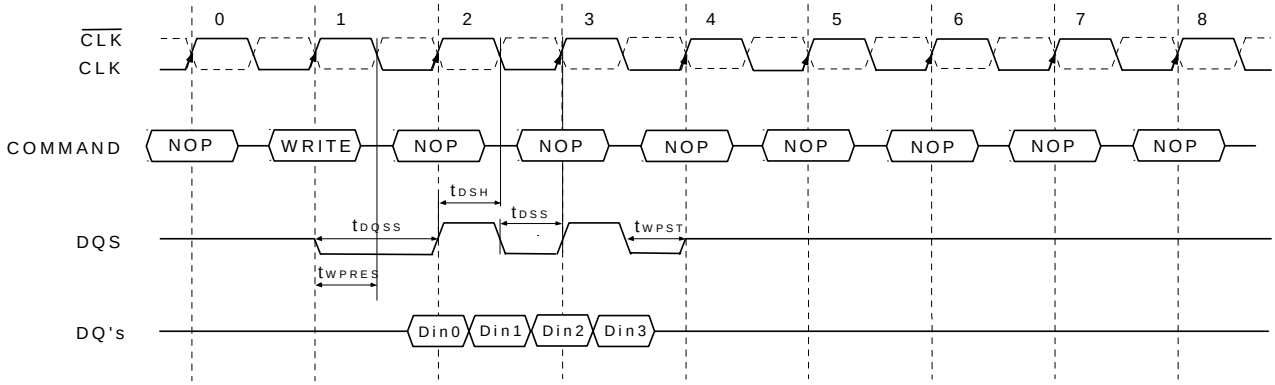
<Burst Length = 4, $\overline{CAS}$ Latency = 3>



Burst Write Operation

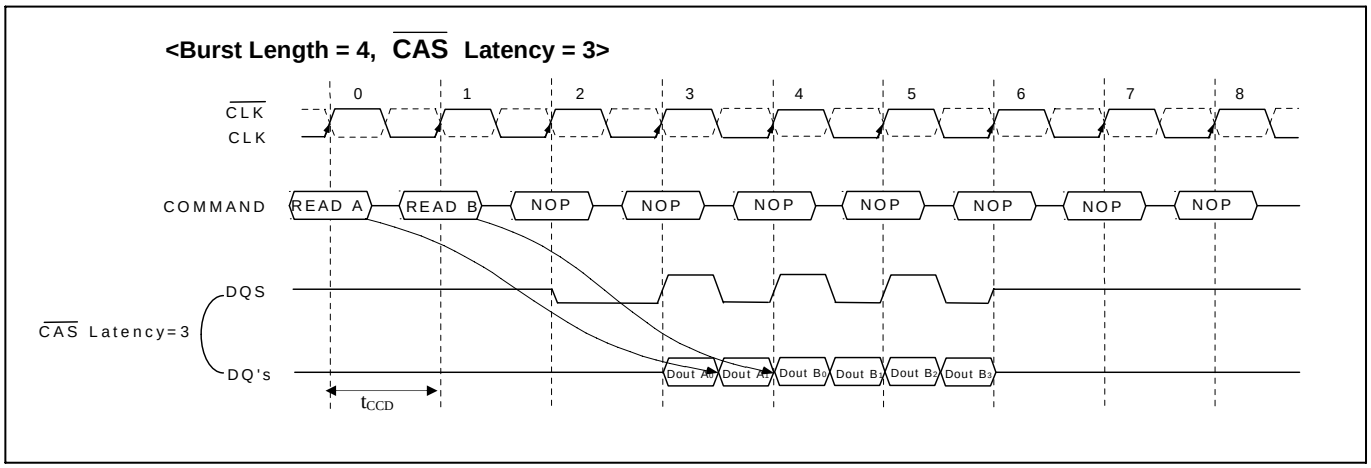
The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock (CLK). The address inputs determine the starting column address. There is no write latency relative to DQS required for burst write cycle. The first data of a burst write cycle must be applied on the DQ pins t_{DS} (Data-in setup time) prior to data strobe edge enabled after t_{DQSS} from the rising edge of the clock (CLK) that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

<Burst Length = 4>



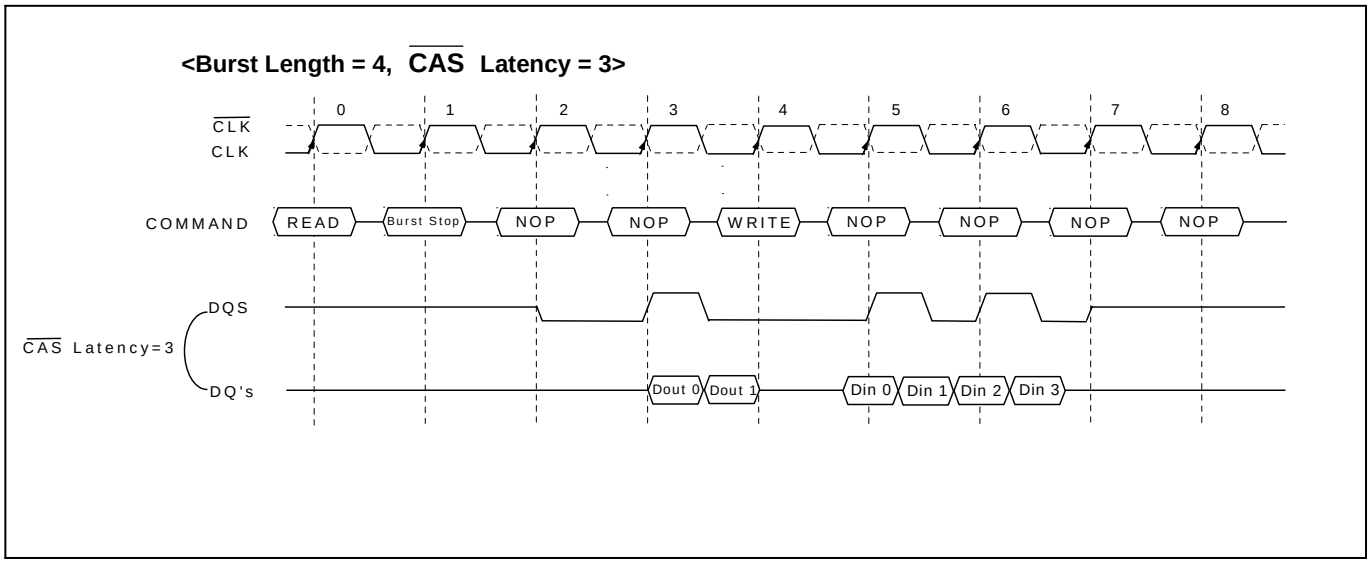
Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by new Read command of any bank. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the $\overline{CAS}$ latency from the interrupting Read command is satisfied. At this point the data from the interrupting Read command appears. Read to Read interval is minimum 1 Clock.



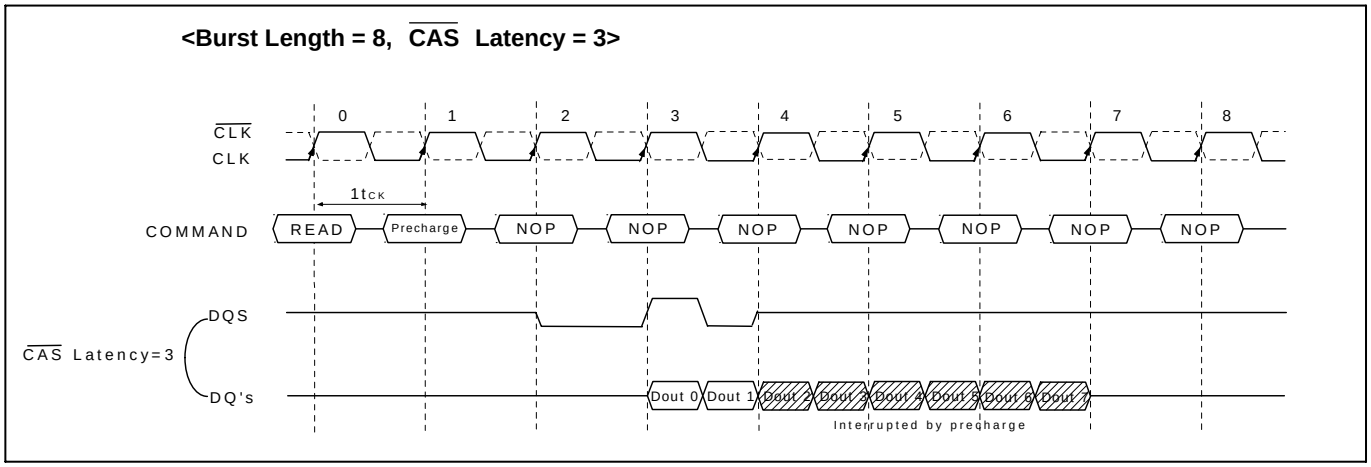
Read Interrupted by a Write & Burst Stop

To interrupt a burst read with a write command, Burst Stop command must be asserted to avoid data contention on the I/O bus by placing the DQ's(Output drivers) in a high impedance state. To insure the DQ's are tri-stated one cycle before the beginning the write operation, Burt stop command must be applied at least RU(CL) clocks 〔RU means round up to the nearest integer〕 before the Write command.



Read Interrupted by a Precharge

A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock is required for the read to precharge intervals. A precharge command to output disable latency is equivalent to the $\overline{CAS}$ latency.



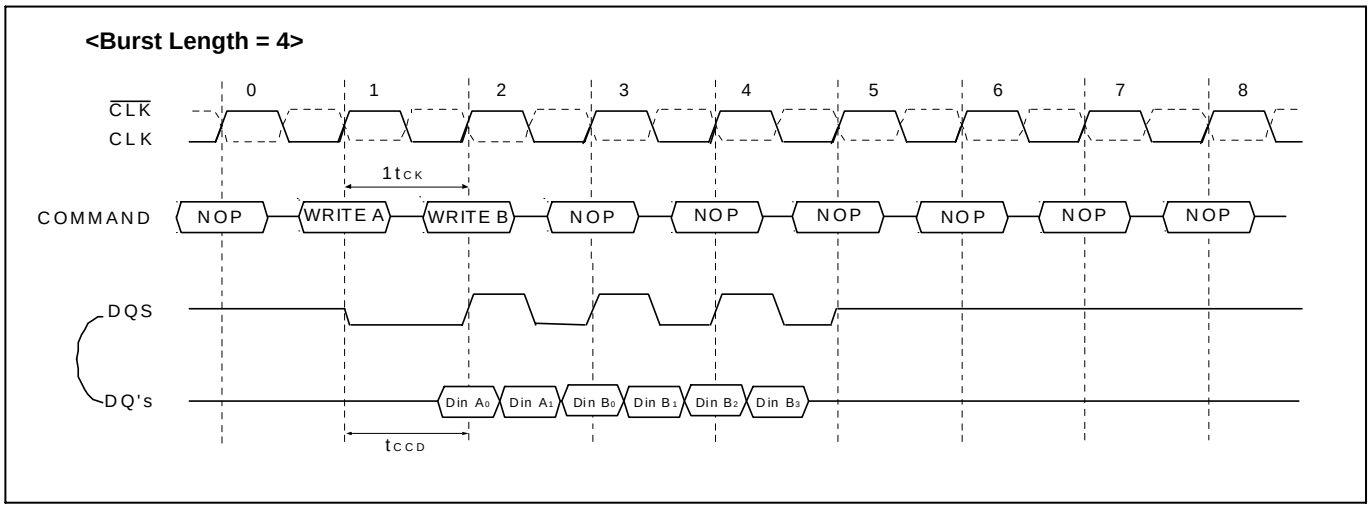
When a burst Read command is issued to a DDR SDRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{CAS}$ Latency. A new Bank Activate command may be issued to the same bank after t_{RP} (RAS precharge time).
2. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the $\overline{CAS}$ Latency. Once the last data word has been output, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after t_{RP}.
3. For a Read with autoprecharge command, a new Bank Activate command may be issued to the same bank after t_{RP} where t_{RP} begins on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{CAS}$ Latency. During Read with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above.
4. For all cases above, t_{RP} is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals t_{RP} / t_{CK} (where t_{CK} is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles.

In all cases, a Precharge operation cannot be initiated unless t_{RAS}(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with autoprecharge commands where t_{RAS}(min) must still be satisfied such that a Read with autoprecharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.

Write Interrupted by a Write

A Burst Write can be interrupted before completion of the burst by a new Write command, with the only restriction that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

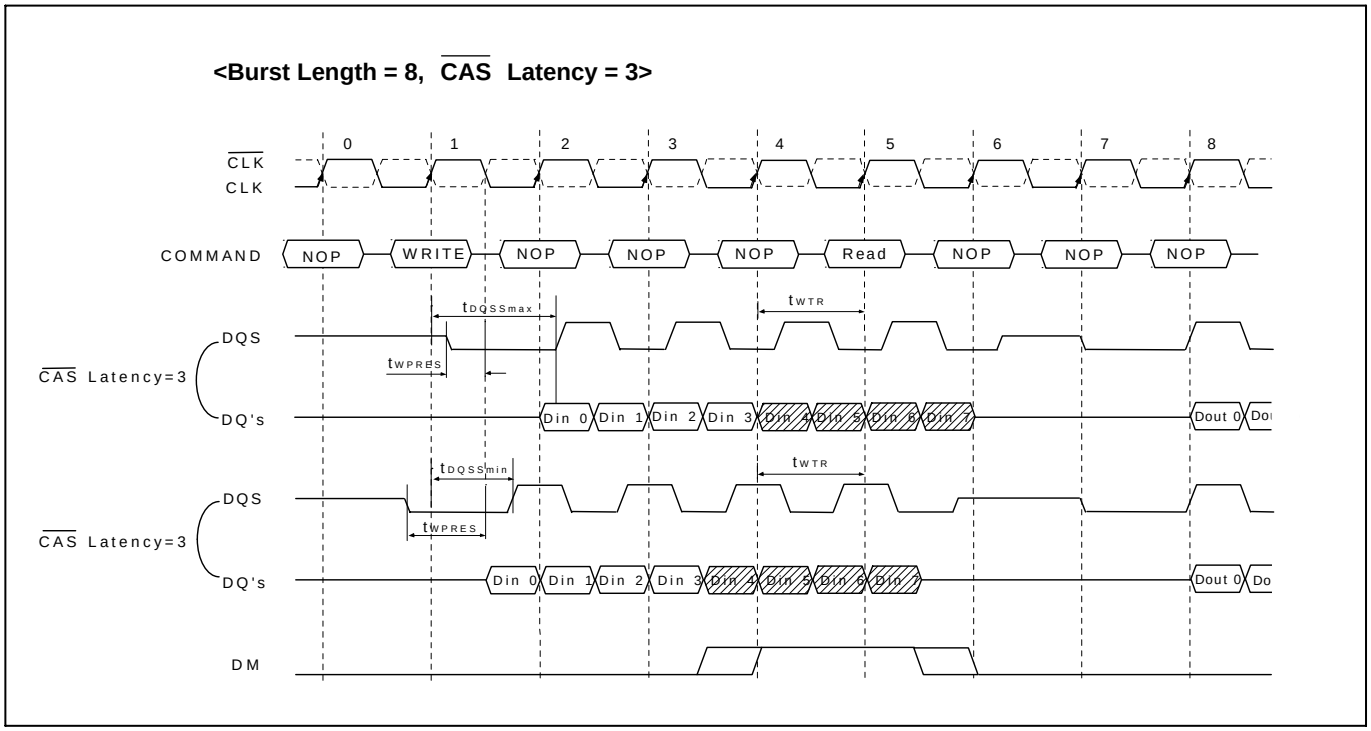


The following functionality establishes how a Write command may interrupt a Read burst.

1. For Write commands interrupting a Read burst, a Read burst, a Burst Terminate command is required to stop the read burst and tristate the DQ bus prior to valid input write data. Once the Burst Terminate command has been issued, the minimum delay to a Write command = RU(CL) [CL is the $\overline{CAS}$ Latency and RU means round up to the nearest integer].
2. It is illegal for a Write command to interrupt a Read with autoprecharge command.

Write Interrupted by a Read & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (t_{WTR}) is required to avoid the data contention DRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.

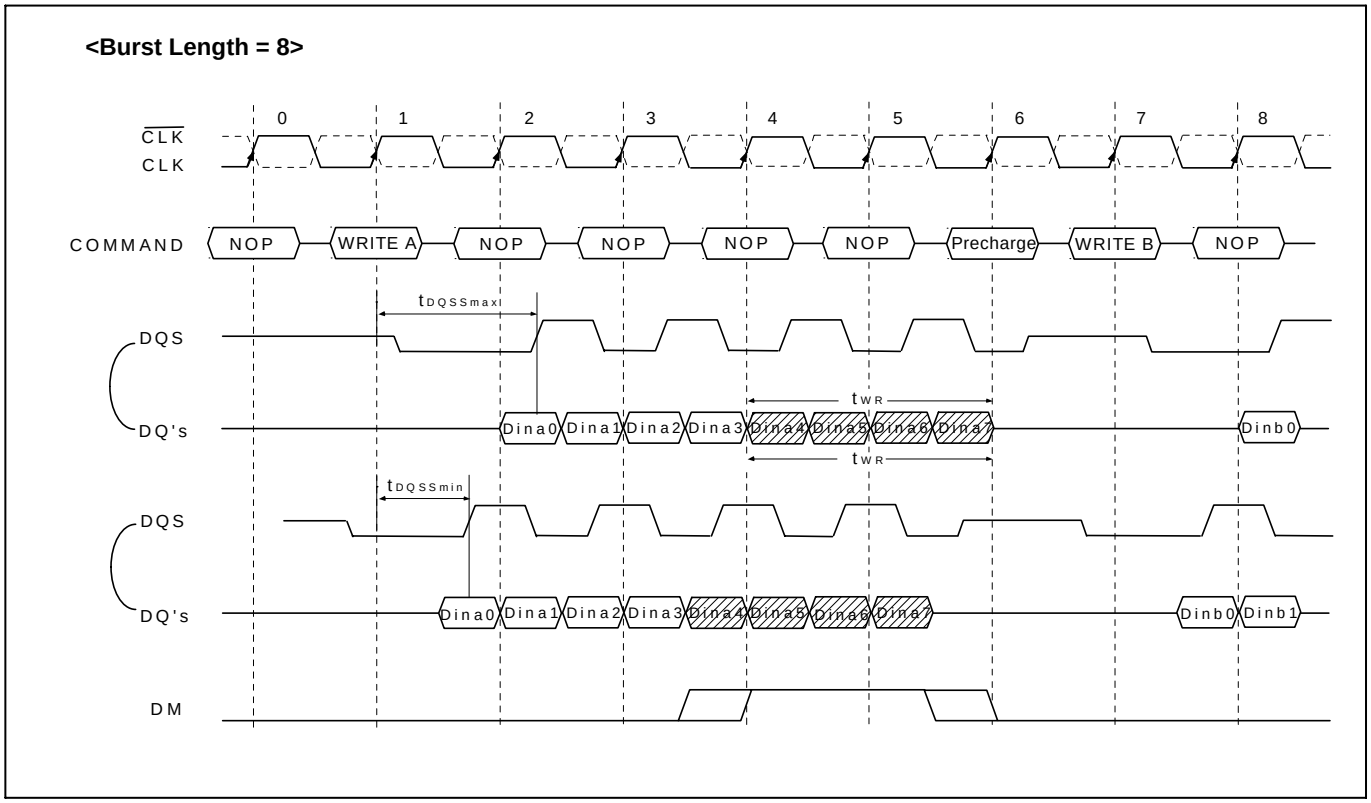


The following functionality established how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed.
2. For read commands interrupting a Write burst, the DM pin must be used to mask the input data words which immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation.
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the SDRAM drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS inputs is ignored by the SDRAM.
5. It is illegal for a Read command interrupt a Write with autoprecharge command.

Write Interrupted by a Precharge & DM

A burst write operation can be interrupted before completion of the burst by a precharge of the same bank. Random column access is allowed. A write recovery time (t_{WR}) is required from the last data to precharge command. When precharge command is asserted, any residual data from the burst write cycle must be masked by DM.



Precharge timing for Write operations in DRAMs requires enough time to allow “Write recovery” which is the time required by a DRAM core to properly store a full “0” or “1” level before a Precharge operation. For DDR SDRAM, a timing parameter, t_{WR}, is used to indicate the required of time between the last valid write operation and a Precharge command to the same bank.

The precharge timing for writes is a complex definition since the write data is sampled by the data strobe and the address is sampled by the input clock. Inside the SDRAM, the data path is eventually synchronizes with the address path by switching clock domains from the data strobe clock domain to the input clock domain.

This makes the definition of when a precharge operation can be initiated after a write very complex since the write recovery parameter must reference only the clock domain that is used to time the internal write operation i.e., the input clock domain.

t_{WR} starts on the rising clock edge after the last possible DQS edge that strobed in the last valid and ends on the rising clock edge that strobes in the precharge command.

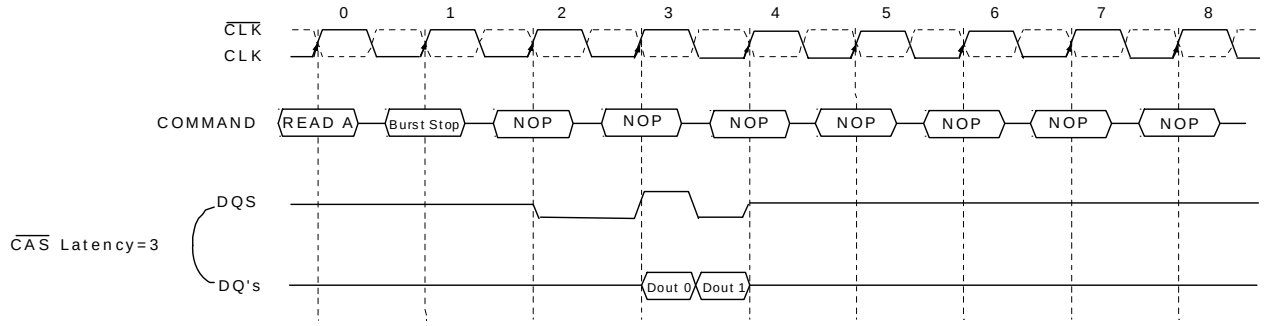
1. For the earliest possible Precharge command following a Write burst without interrupting the burst, the minimum time for write recovery is defined by t_{WR}.

2. When a precharge command interrupts a Write burst operation, the data mask pin, DQ, is used to mask input data during the time between the last valid write data and the rising clock edge in which the Precharge command is given. During this time, the DQS input is still required to strobe in the state of DM.
   The minimum time for write recovery is defined by t_{WR}.
3. For a Write with autoprecharge command, a new Bank Activate command may be issued to the same bank after $t_{WR} + t_{RP}$ where $t_{WR} + t_{RP}$ starts on the falling DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the Bank Activate commands. During write with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command without interrupting the Write burst as described in 1 above.
4. In all cases, a Precharge operation cannot be initiated unless t_{RAS}(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Write with autoprecharge commands where t_{RAS}(min) must still be satisfied such that a Write with autoprecharge command has the same timing as a Write command followed by the earliest possible Precharge command which does not interrupt the burst.

Burst Stop

The burst stop command is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock (CLK). The burst stop command has the fewest restriction making it the easiest method to use when terminating a burst read operation before it has been completed. When the burst stop command is issued during a burst read cycle, the pair of data and DQS (Data Strobe) go to a high impedance state after a delay which is equal to the $\overline{CAS}$ latency set in the mode register. The burst stop command, however, is not supported during a write burst operation.

<Burst Length = 4, $\overline{CAS}$ Latency = 3 >



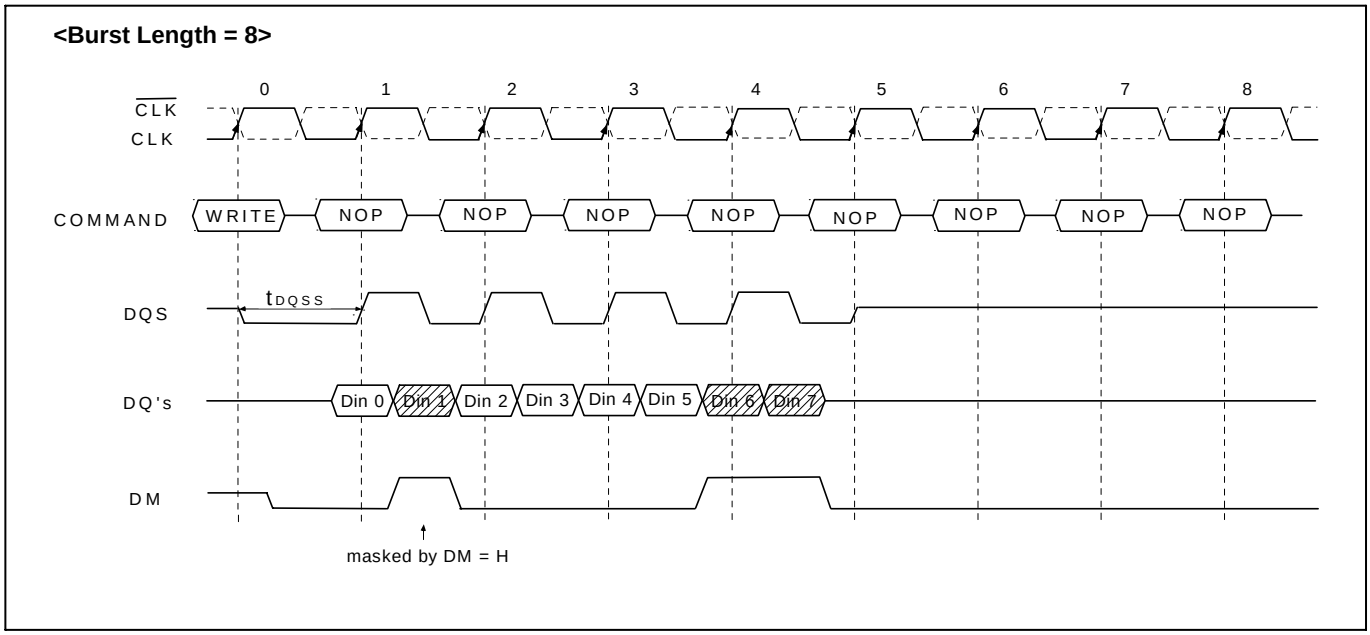
The Burst Stop command is a mandatory feature for DDR SDRAMs. The following functionality is required.

1. The BST command may only be issued on the rising edge of the input clock, CLK.
2. BST is only a valid command during Read burst.
3. BST during a Write burst is undefined and shall not be used.
4. BST applies to all burst lengths.
5. BST is an undefined command during Read with autoprecharge and shall not be used.
6. When terminating a burst Read command, the BST command must be issued L_{BST} (“BST Latency”) clock cycles before the clock edge at which the output buffers are tristated, where L_{BST} equals the $\overline{CAS}$ latency for read operations.
7. When the burst terminates, the DQ and DQS pins are tristated.

The BST command is not byte controllable and applies to all bits in the DQ data word and the (all) DQS pin(s).

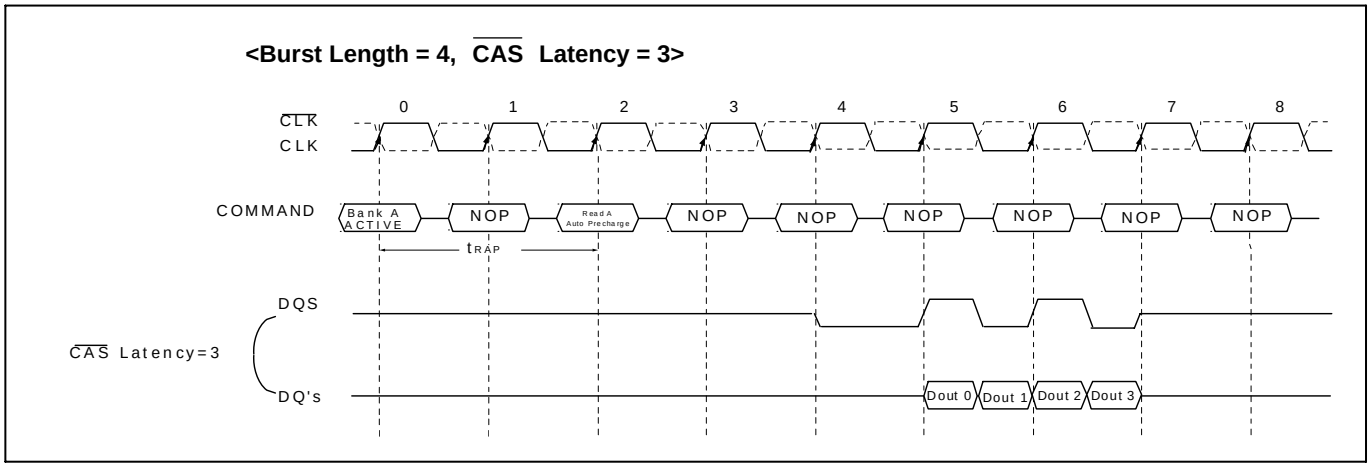
DM masking

The DDR SDRAM has a data mask function that can be used in conjunction with data write cycle. Not read cycle. When the data mask is activated (DM high) during write operation, DDR SDRAM does not accept the corresponding data. (DM to data-mask latency is zero) DM must be issued at the rising or falling edge of data strobe.



Read With Auto Precharge

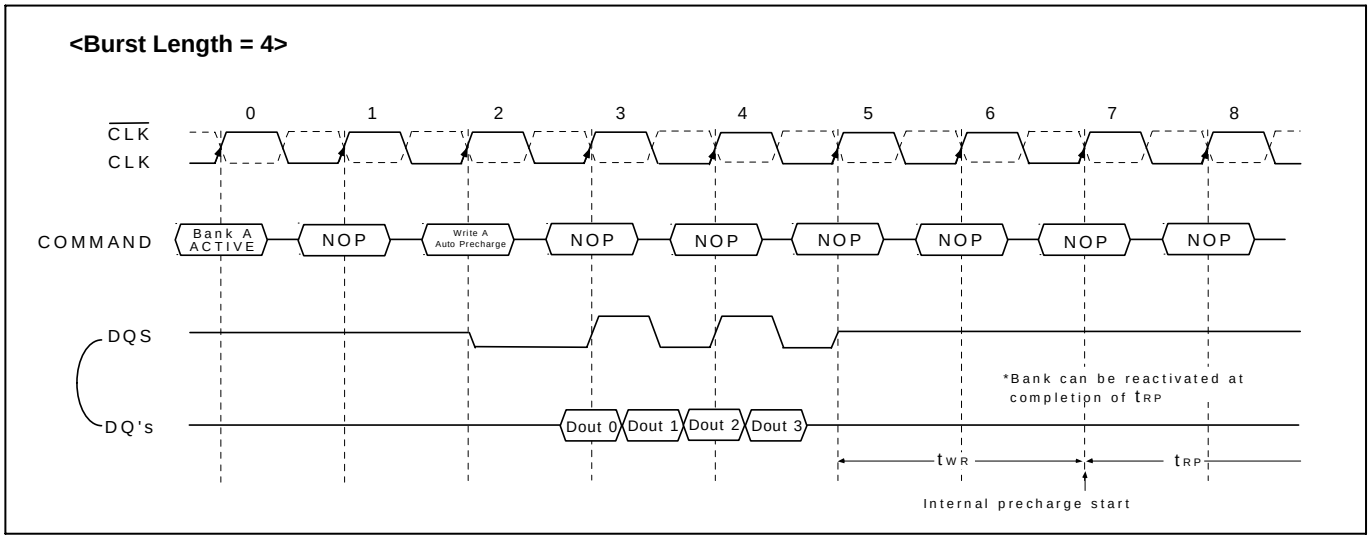
If a read with auto-precharge command is initiated, the DDR SDRAM automatically enters the precharge operation BL/2 clock later from a read with auto-precharge command when t_{RAS}(min) is satisfied. If not, the start point of precharge operation will be delayed until t_{RAS}(min) is satisfied. Once the precharge operation has started the bank cannot be reactivated and the new command can not be asserted until the precharge time (t_{RP}) has been satisfied



At burst read / write with auto precharge, $\overline{CAS}$ interrupt of the same bank is illegal.

Write with Auto Precharge

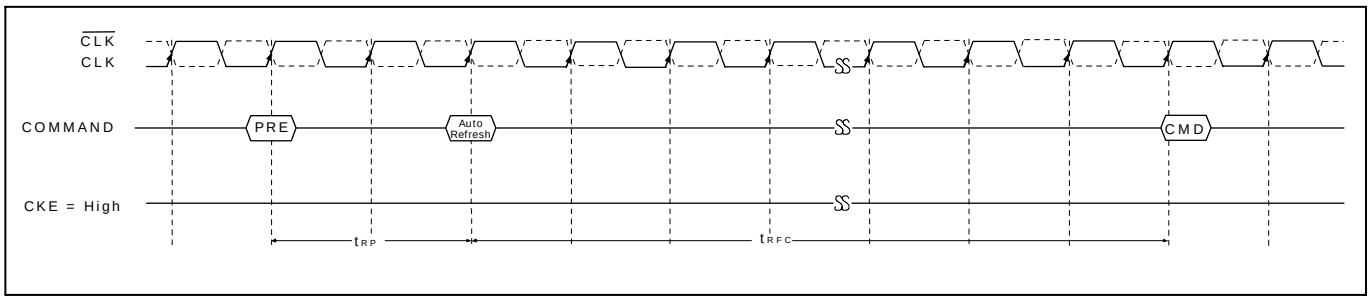
If A10 is high when write command is issued, the write with auto-precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping t_{WR}(min).



Auto Refresh & Self Refresh

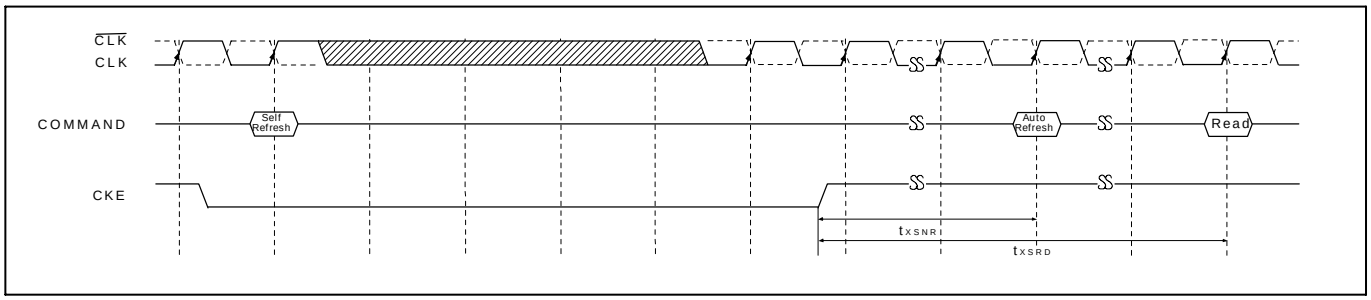
Auto Refresh

An auto refresh command is issued by having $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock(CLK). All banks must be precharged and idle for t_{RP}(min) before the auto refresh command is applied. No control of the external address pins is requires once this cycle has started because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the t_{RFC}(min).



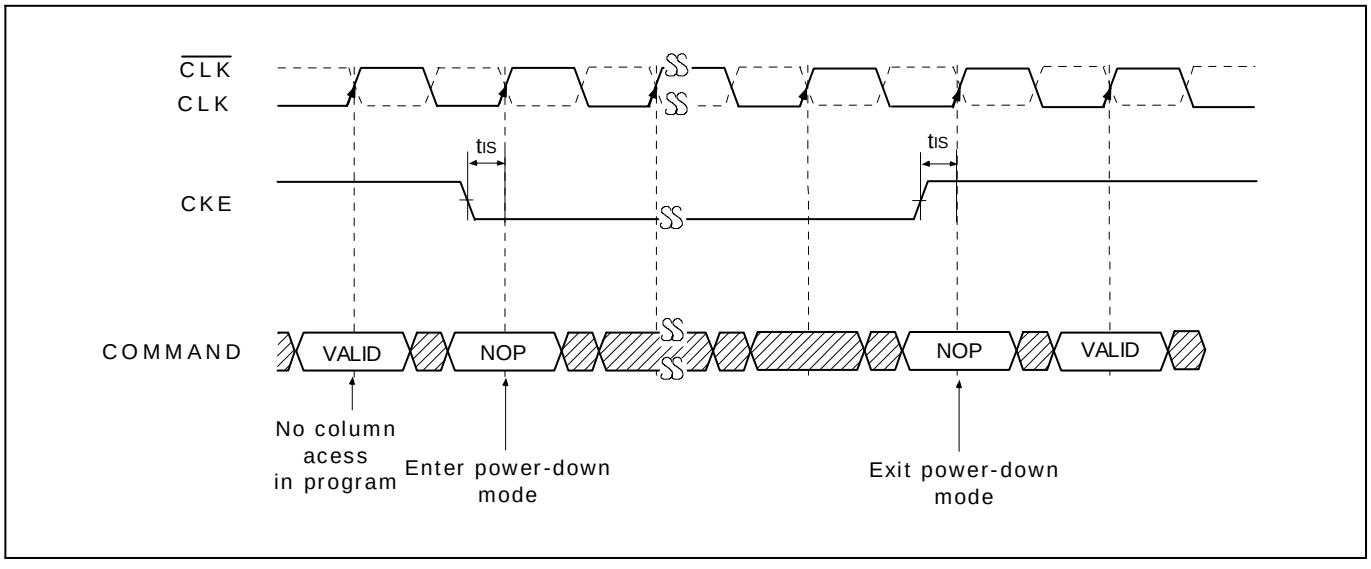
Self Refresh

A self refresh command is defines by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock (CLK). Once the self refresh command is initiated, CKE must be held low to keep the device in self refresh mode. During the self refresh operation, all inputs except CKE are ignored. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning CKE high, asserting deselect or NOP command and then asserting CKE high for longer than t_{XSRD} for locking of DLL.



Power down

Power down is entered when CKE is registered low (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CLK, $\overline{CLK}$ and CKE. For maximum power savings, the user has the option of disabling the DLL prior to entering power-down. In that case, the DLL must be enabled after exiting power-down, and 200 clock cycles must occur before a READ command can be issued. However, power-down duration is limited by the refresh requirements of the device, so in most applications, the self-refresh mode is preferred over the DLL disable power-down mode. In the power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are “Don’t Care”. The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESELECT command). A valid executable command may be applied one clock cycle later.



Functional Truth Table.

Current	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	Bank Active, Latch RA
	L	L	H	L	BA, A10	PRE / PREA	NOP*4
	L	L	L	H	X	Refresh	AUTO-Refresh*5
	L	L	L	L	Op-Code Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	Burst Stop	NOP
	L	H	L	H	BA, CA, A10	READ / READA	Begin Read, Latch CA, Determine Auto -precharge
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto -precharge
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Precharge/Precharge All
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	Burst Stop	Terminate Burst
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
WRITE	H	X	X	X	X	DESEL	NOP (Continue Burst to end)
	L	H	H	H	X	NOP	NOP (Continue Burst to end)
	L	H	H	L	BA	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	Terminate Burst With DM=High, Latch CA, Begin Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	Terminate Burst, Latch CA, Begin new Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Terminal Burst With DM=High, Precharge
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to end)
	L	H	H	H	X	NOP	NOP (Continue Burst to end)
	L	H	H	L	BA	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ	READ*7
	L	H	L	L	BA, CA, A10	WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ	ILLEGAL
	L	H	L	L	BA, CA, A10	WRITE	Write
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
PRE-CHARGING	H	X	X	X	X	DESEL	NOP (Idle after t_{RP})
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})
	L	H	H	L	BA	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	NOP*4 (Idle after t_{RP})
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (ROW Active after t_{RCD})
	L	H	H	H	X	NOP	NOP (ROW Active after t_{RCD})
	L	H	H	L	BA	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL
WRITE RECOVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	Burst Stop	ILLEGAL*2
	L	H	L	H	BA, CA, A10	READ	ILLEGAL*2
	L	H	L	L	BA, CA, A10	WRITE	WRITE
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
RE-FRESHING	H	X	X	X	X	DESEL	NOP (Idle after t_{RP})
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})
	L	H	H	L	BA	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after t_{RP})
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})
	L	H	H	L	BA	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL

ABBREVIATIONS :

H = High Level, L = Low level, V = Valid, X = Don't Care

BA = Bank Address, RA =Row Address, CA = Column Address, NOP = No Operation

Note :

1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of the bank.
3. Must satisfy bus contention, bus turn around and write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL of any bank is not idle.
6. Same bank's previous auto precharg will not be performed. But if the bank is different, previous auto precharge will be performed.
7. Refer to "Read with Auto Precharge: for more detailed information.
   ILLEGAL = Device operation and / or data integrity are not guaranteed.

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Action
SELF-REFRESHING*1	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh
	L	H	L	H	H	H	X	Exit Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down (Idle after t_{PDEX})
	L	L	X	X	X	X	X	NOP (Maintain Power Down)
ALL BANKS IDLE*2	H	H	X	X	X	X	X	Refer to Function True Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Exit Power Down
	H	L	L	H	H	H	X	Exit Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	L	L	X	X	X	X	Refer to Current State = Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function True Table

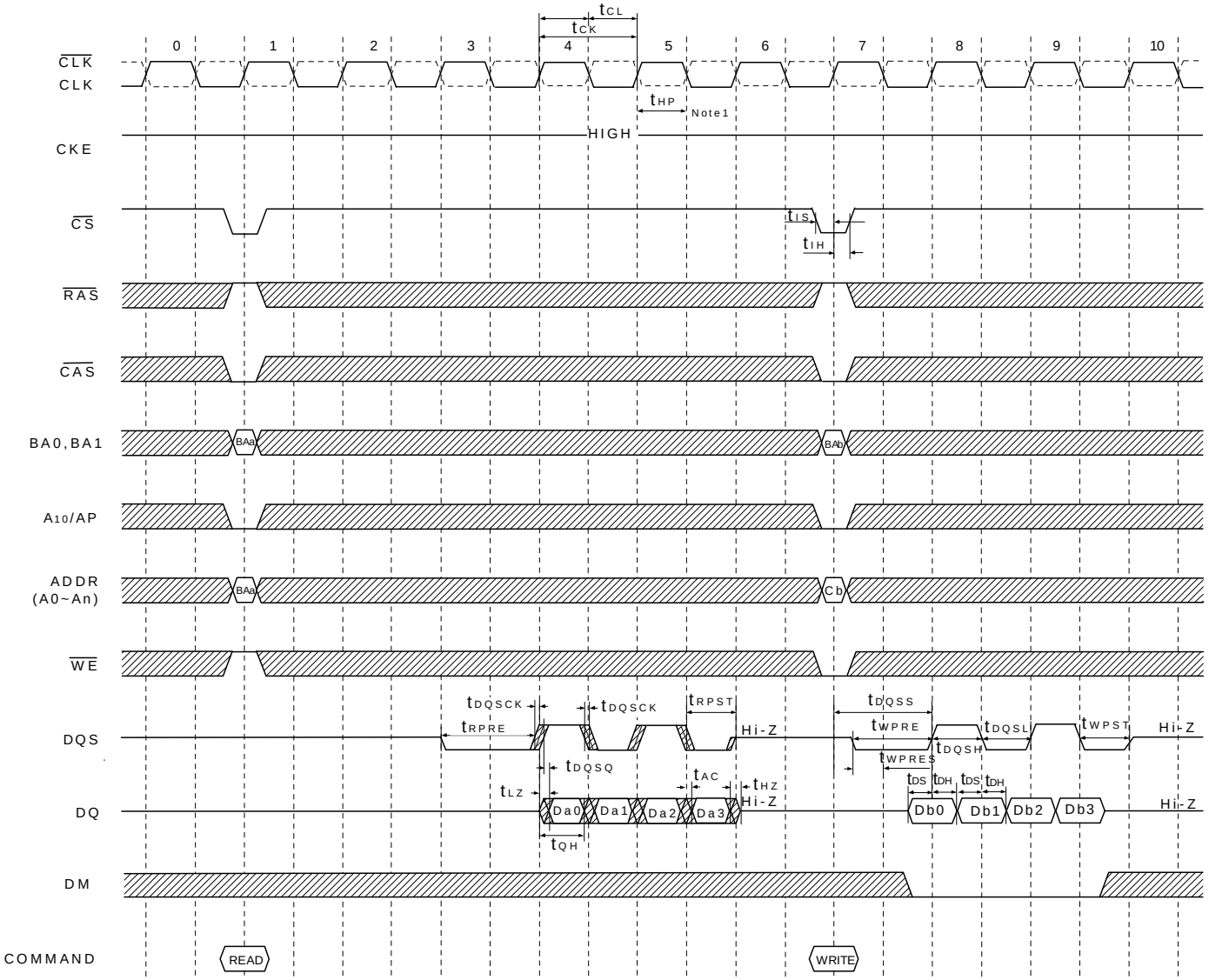
ABBREVIATIONS :

H = High Level, L = Low level, V = Valid, X = Don't Care

Note :

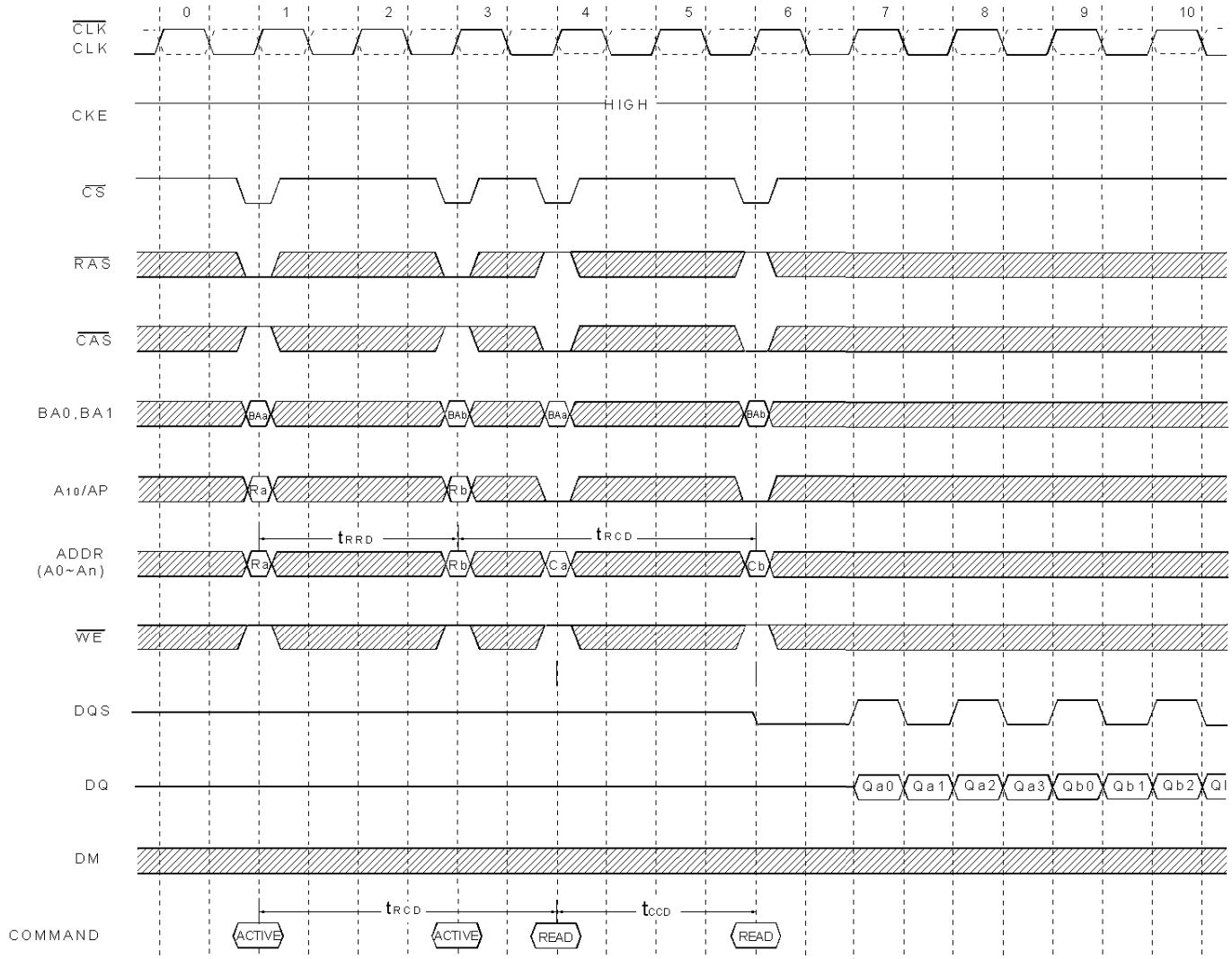
1. CKE Low to High transition will re-enable CLK, $\overline{CLK}$ and other inputs asynchronously. A minimum setup time must be satisfied before issuing any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from All Bank Idle state.

Basic Timing (Setup, Hold and Access Time @ BL=4, CL=3)

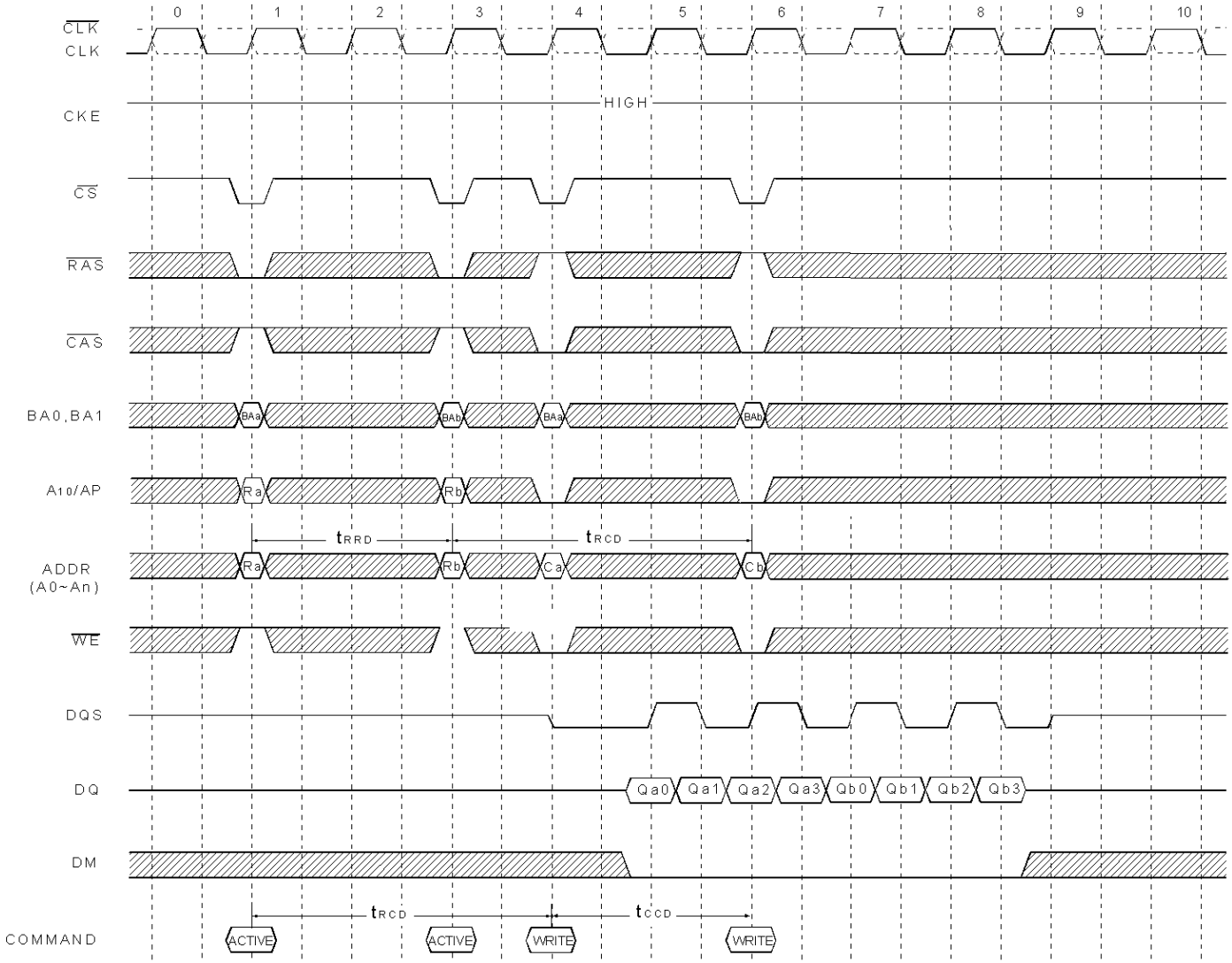


Note 1. t_{HP} is lesser of t_{CL} or t_{CH} clock transition collectively when a bank is active.

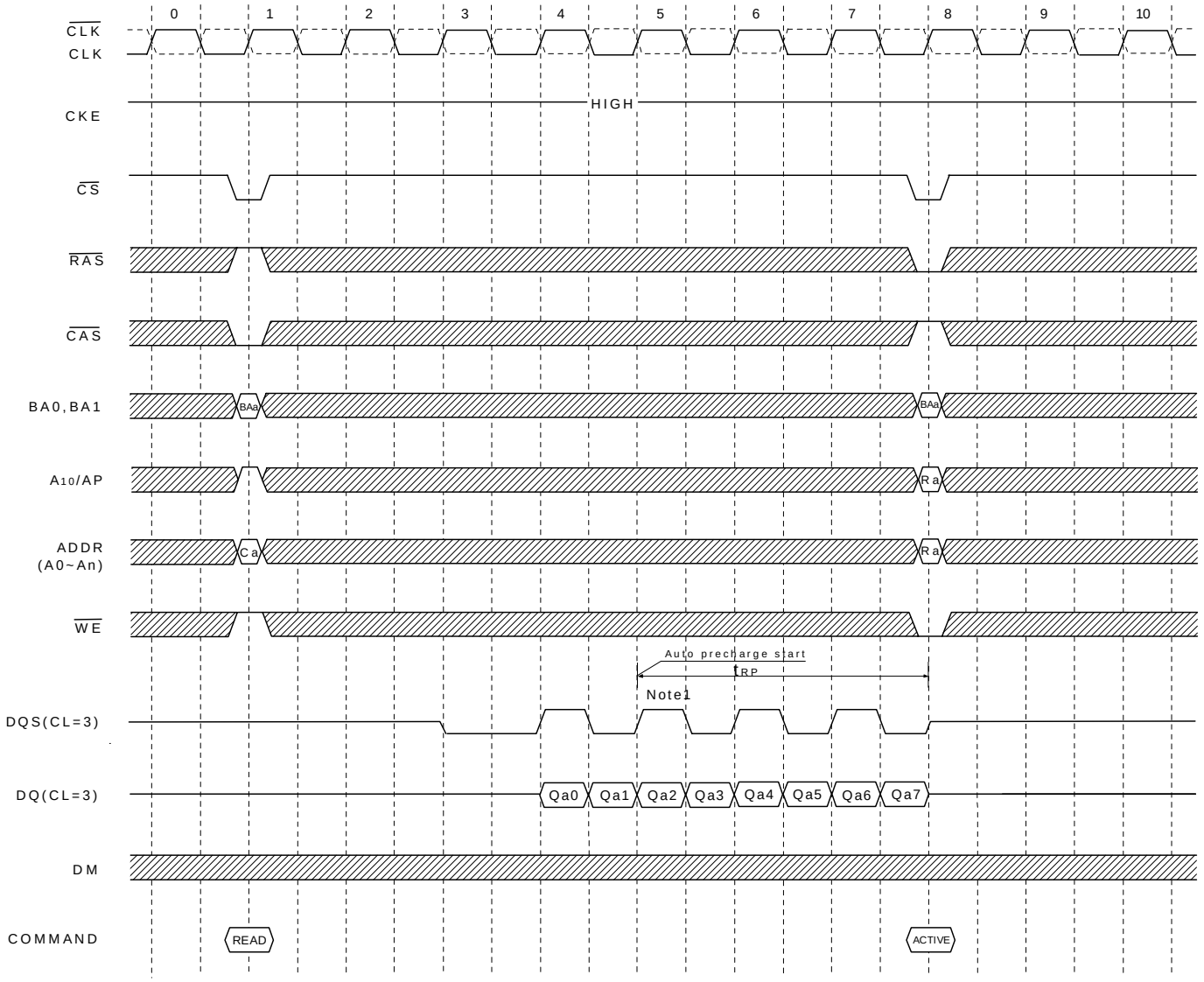
Multi Bank Interleaving READ (@BL=4, CL=3)



Multi Bank Interleaving WRITE (@BL=4)

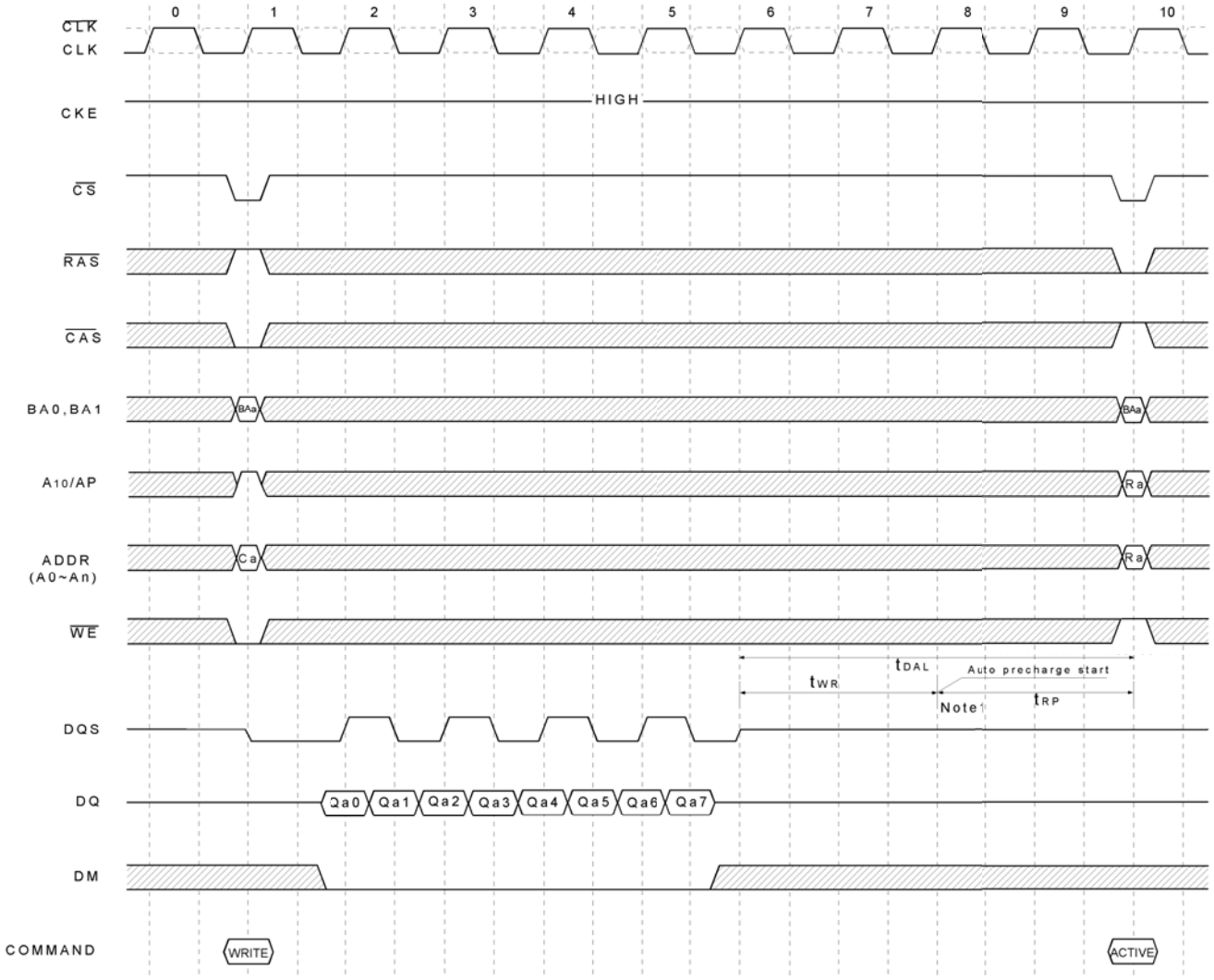


Read with Auto Precharge (@BL=8)



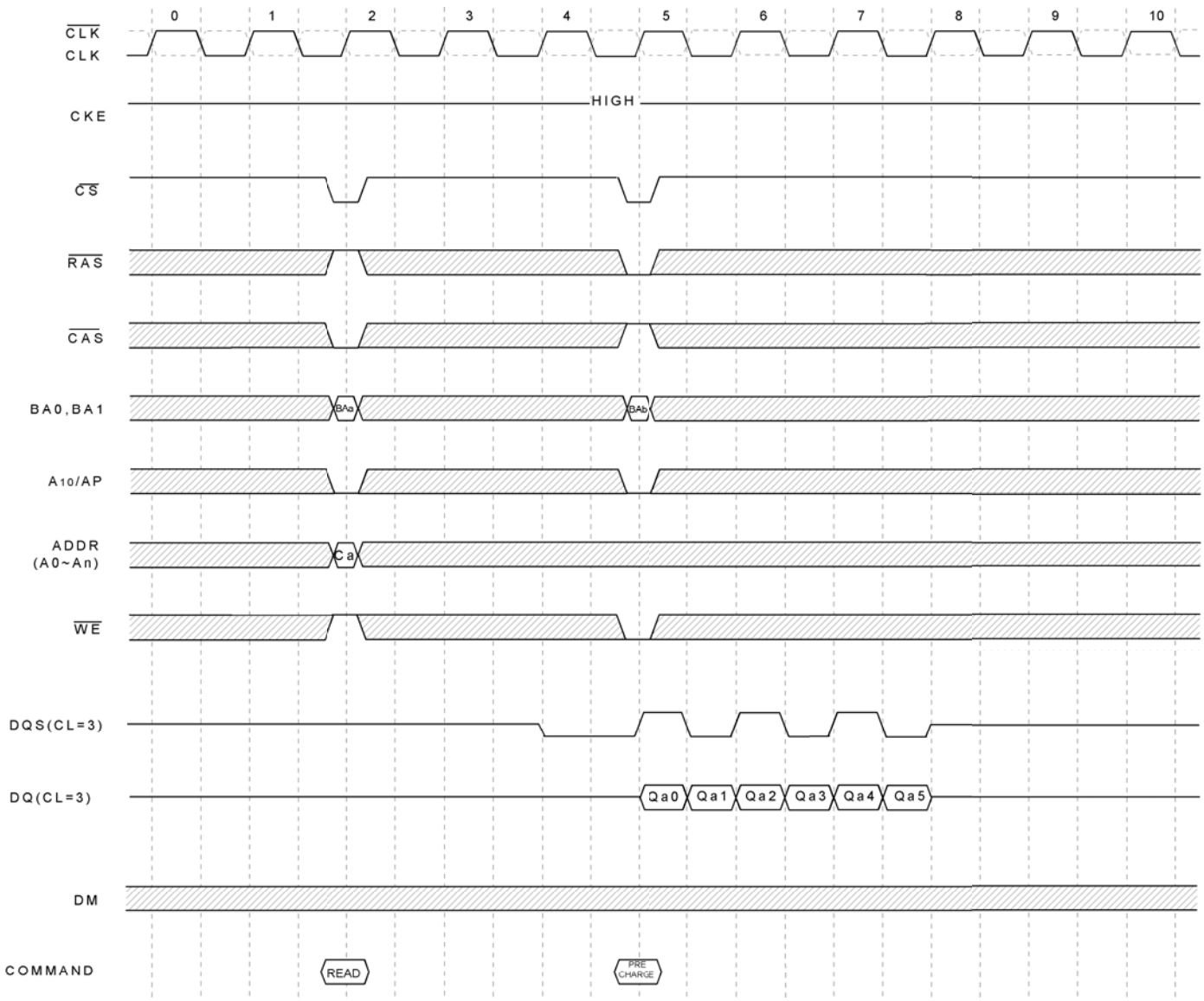
Note 1. The row active command of the precharge bank can be issued after t_{RP} from this point.
The new read/write command of another activated bank can be issued from this point.
At burst read/write with auto precharge, $\overline{CAS}$ interrupt of the same bank is illegal.

Write with Auto Precharge (@BL=8)



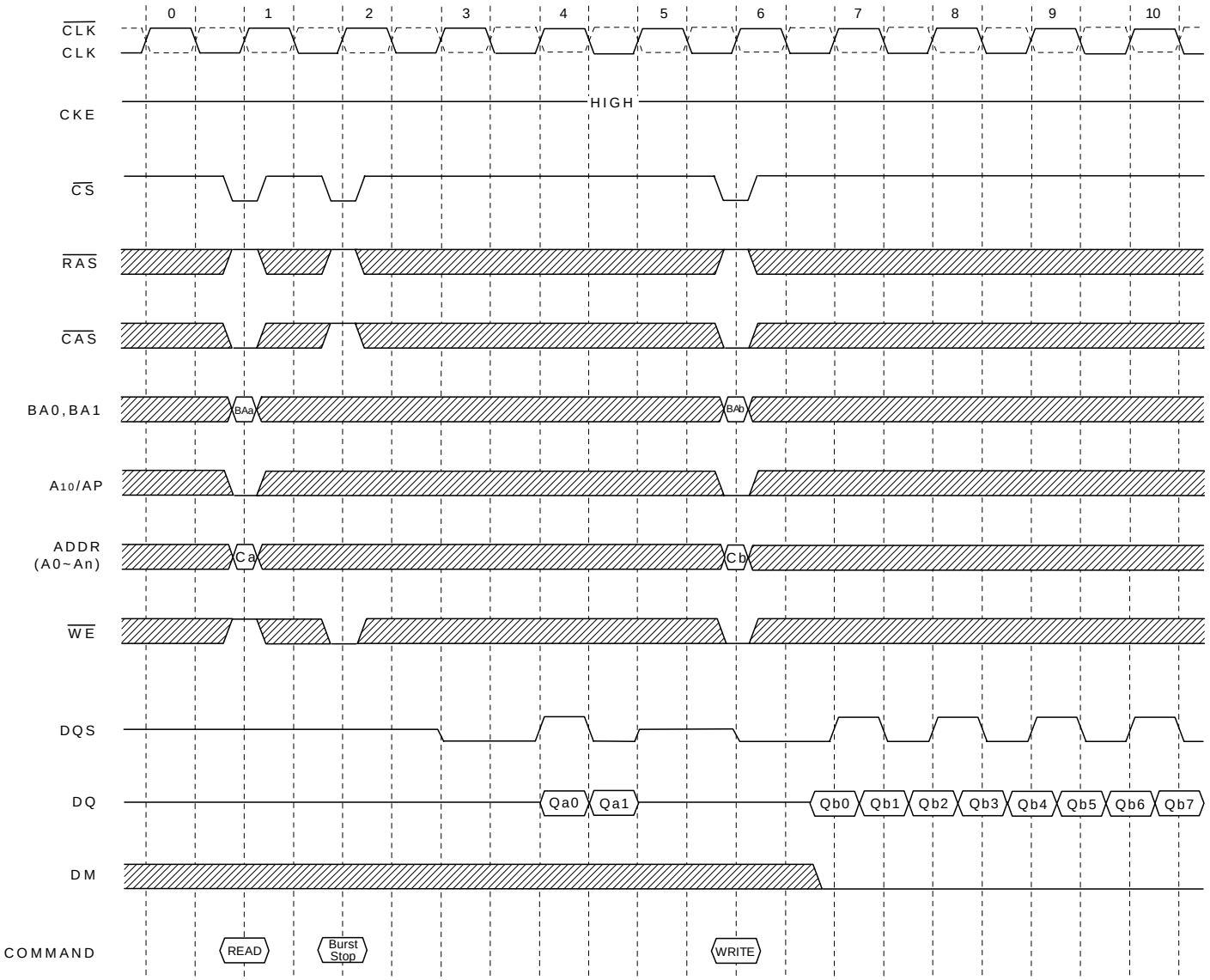
Note 1. The row active command of the precharge bank can be issued after t_{RP} from this point.
The new read/write command of another activated bank can be issued from this point.
At burst read/write with auto precharge, $\overline{CAS}$ interrupt of the same/another bank is illegal.

Read Interrupted by Precharge (@BL=8)

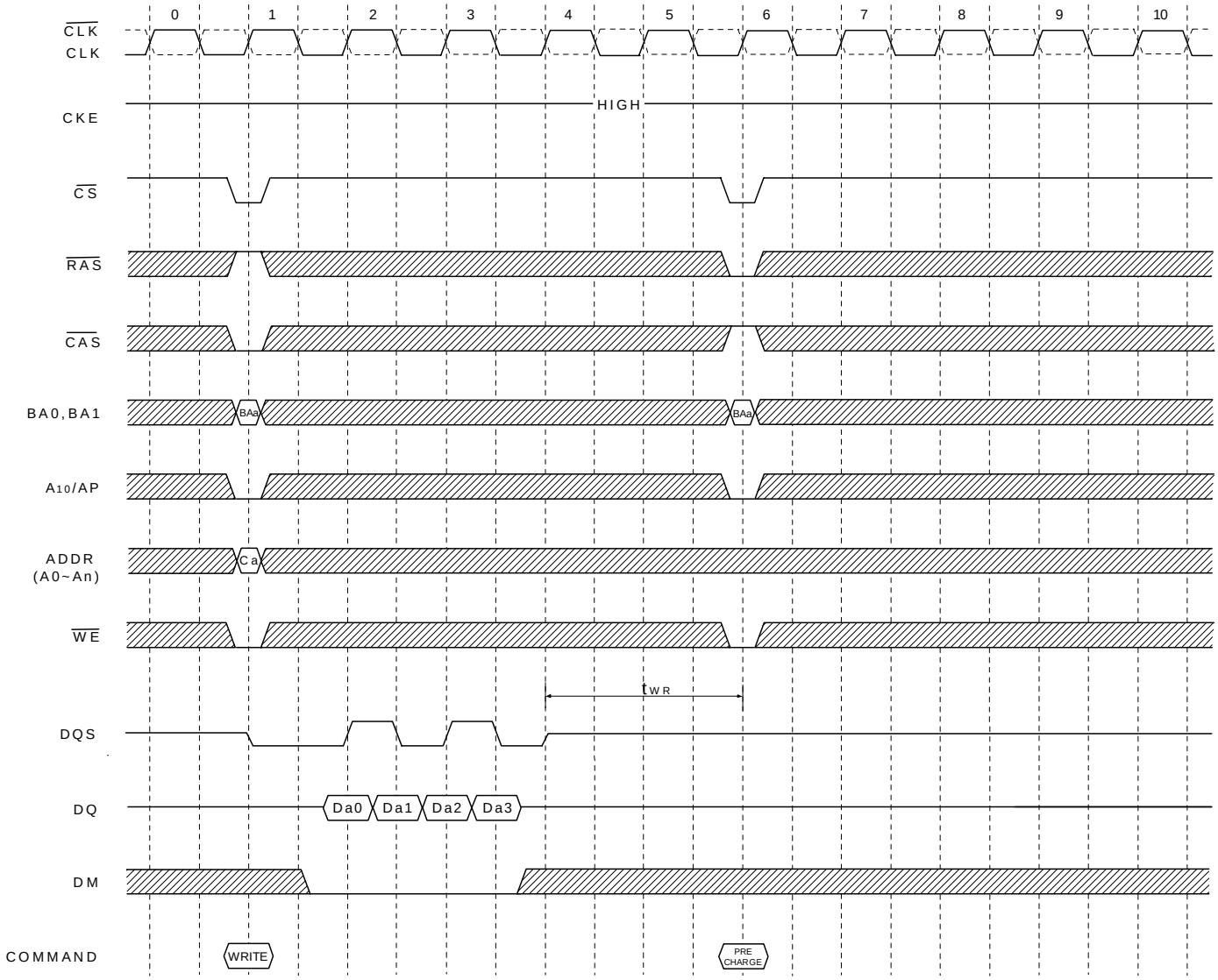


Read Interrupted by a Read (@BL=8, CL=3)

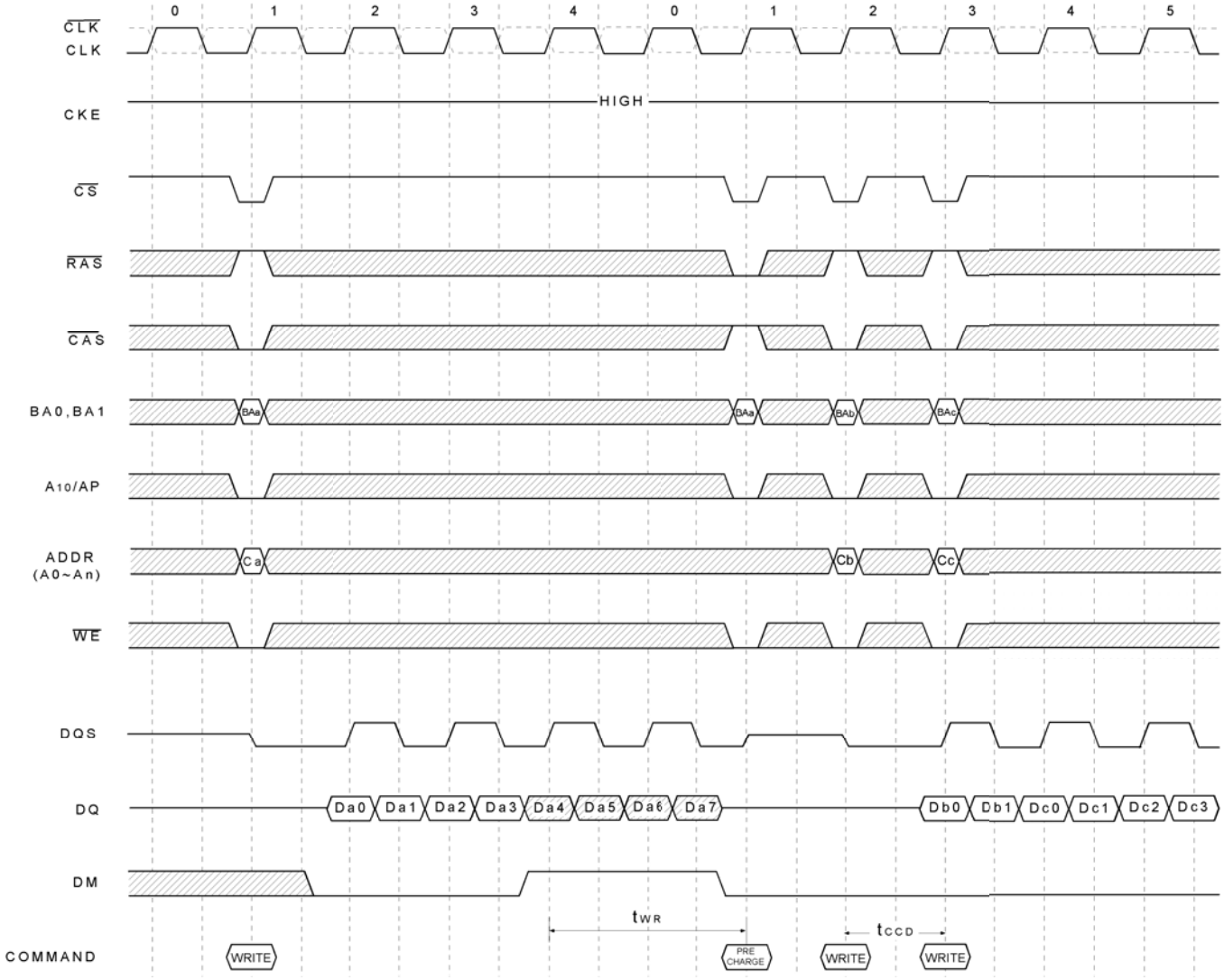
Read Interrupted by a Write & Burst stop (@BL=8, CL=3)



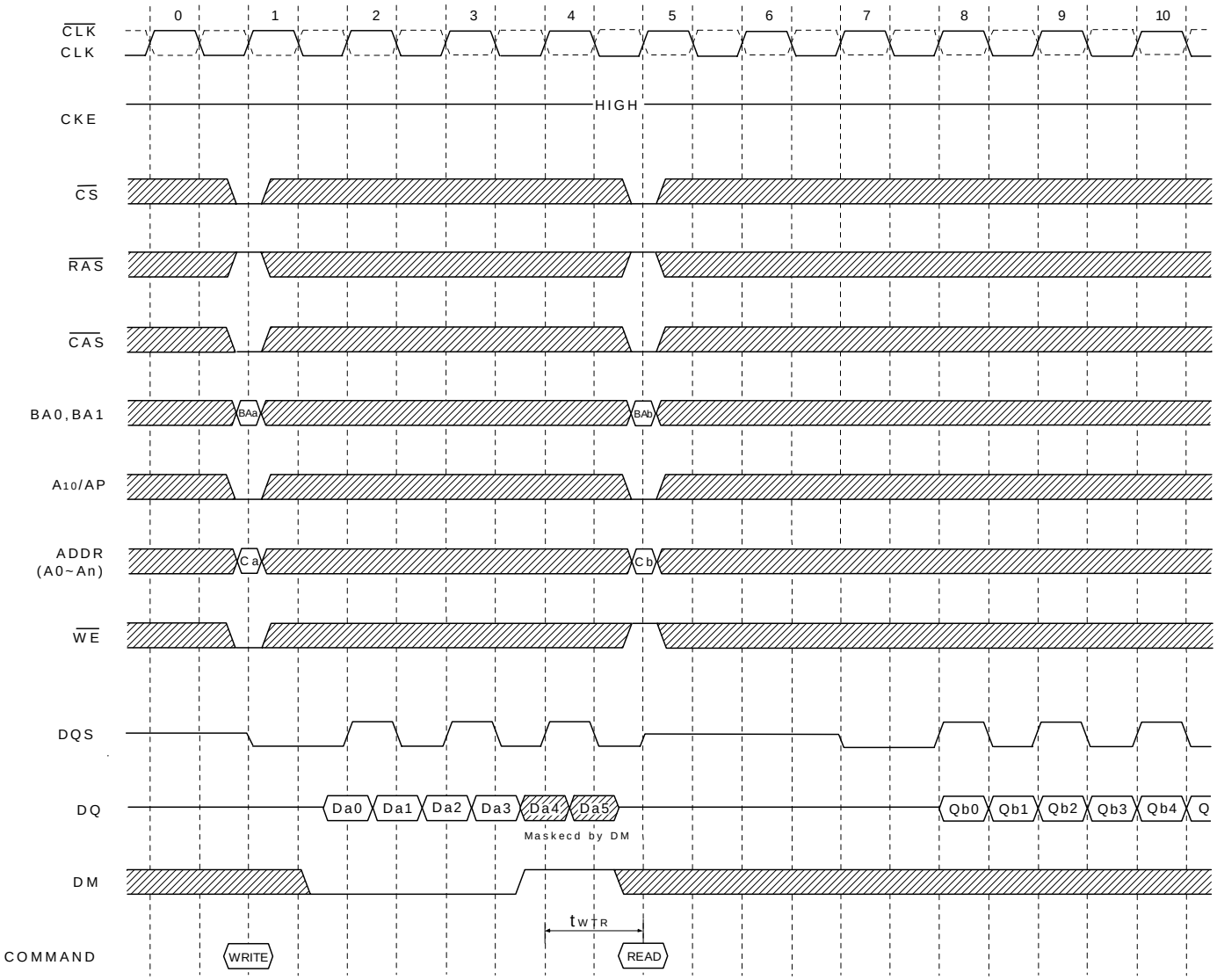
Write followed by Precharge (@BL=4)



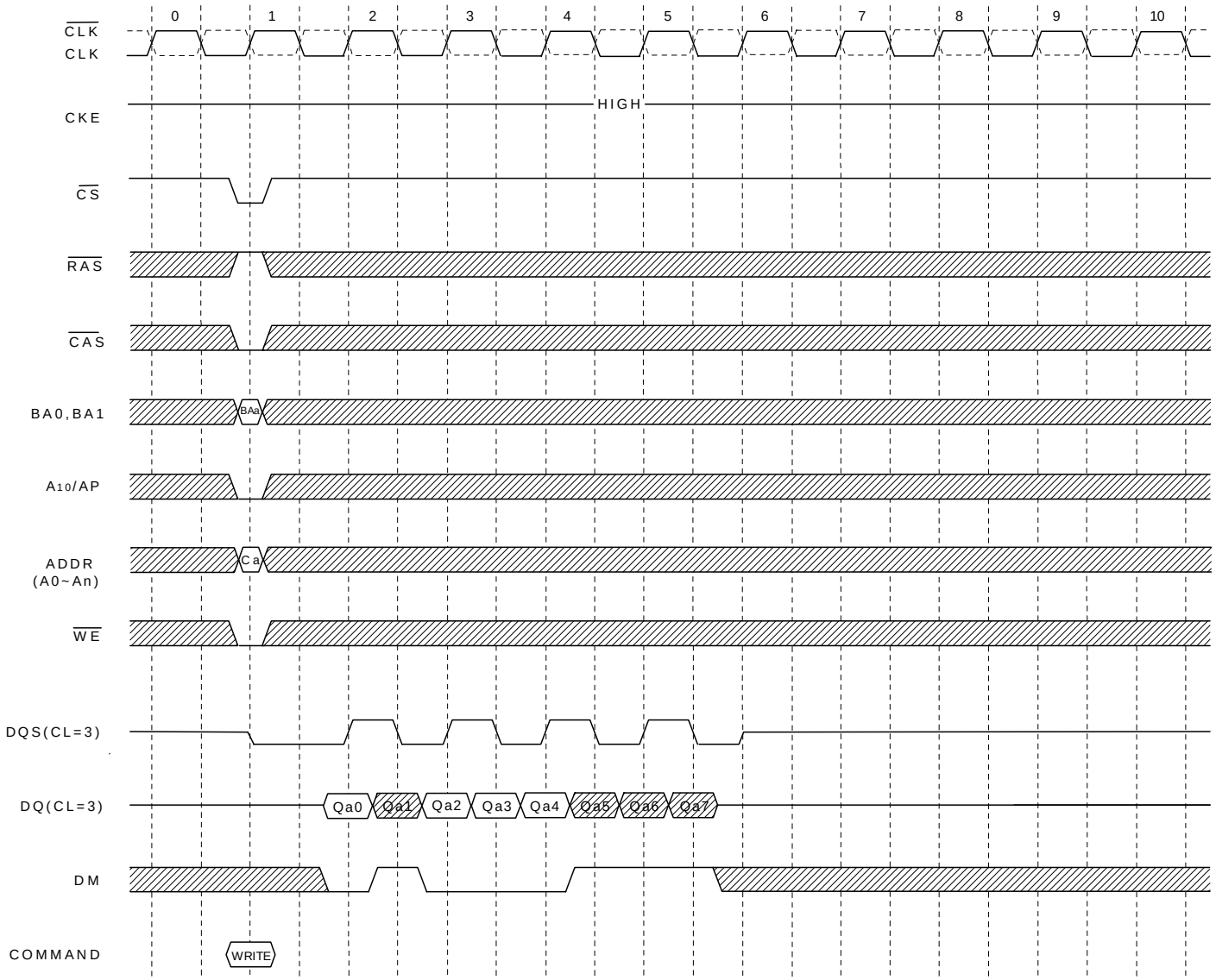
Write Interrupted by Precharge & DM (@BL=8)



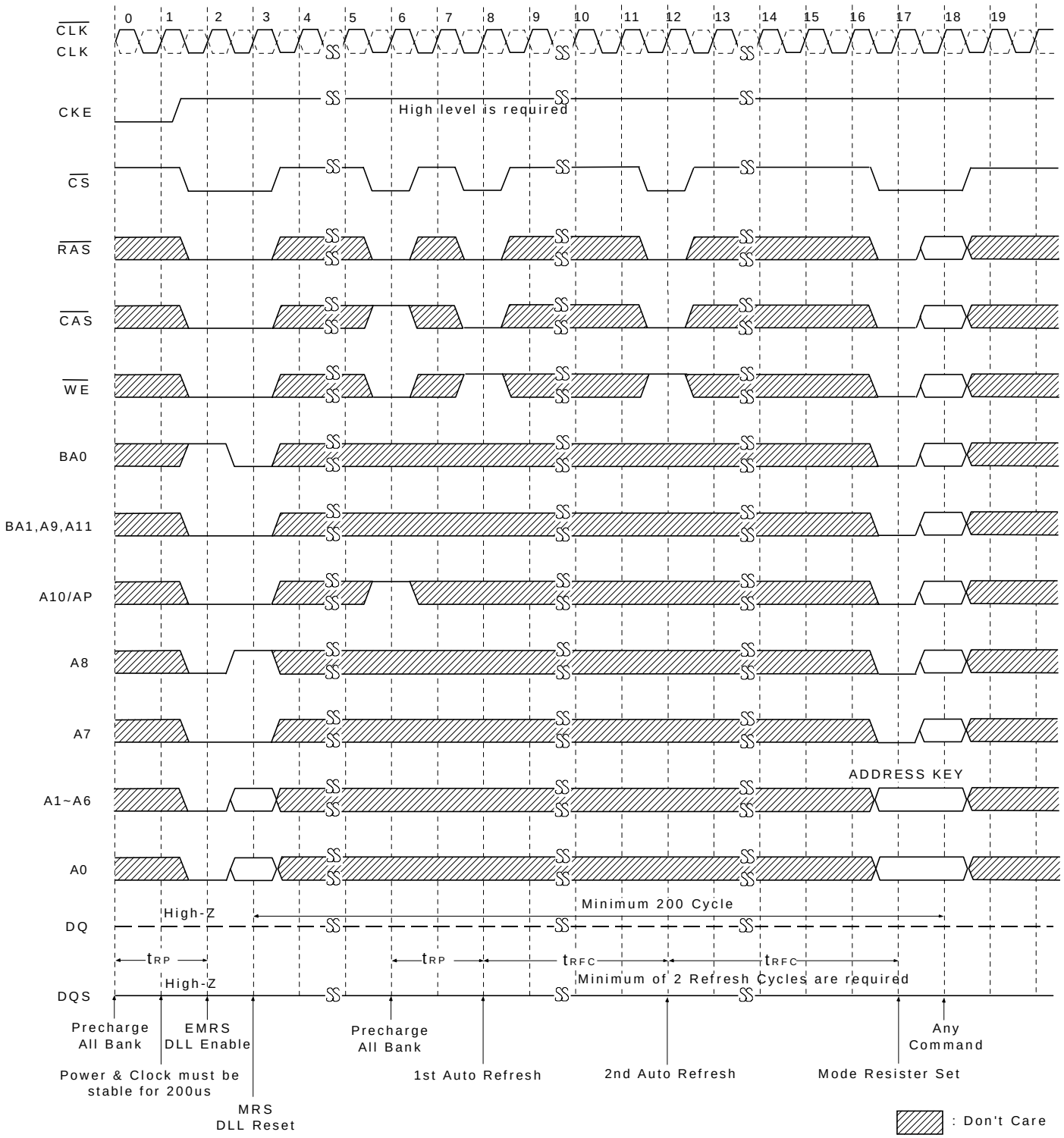
Write Interrupted by a Read (@BL=8, CL=3)



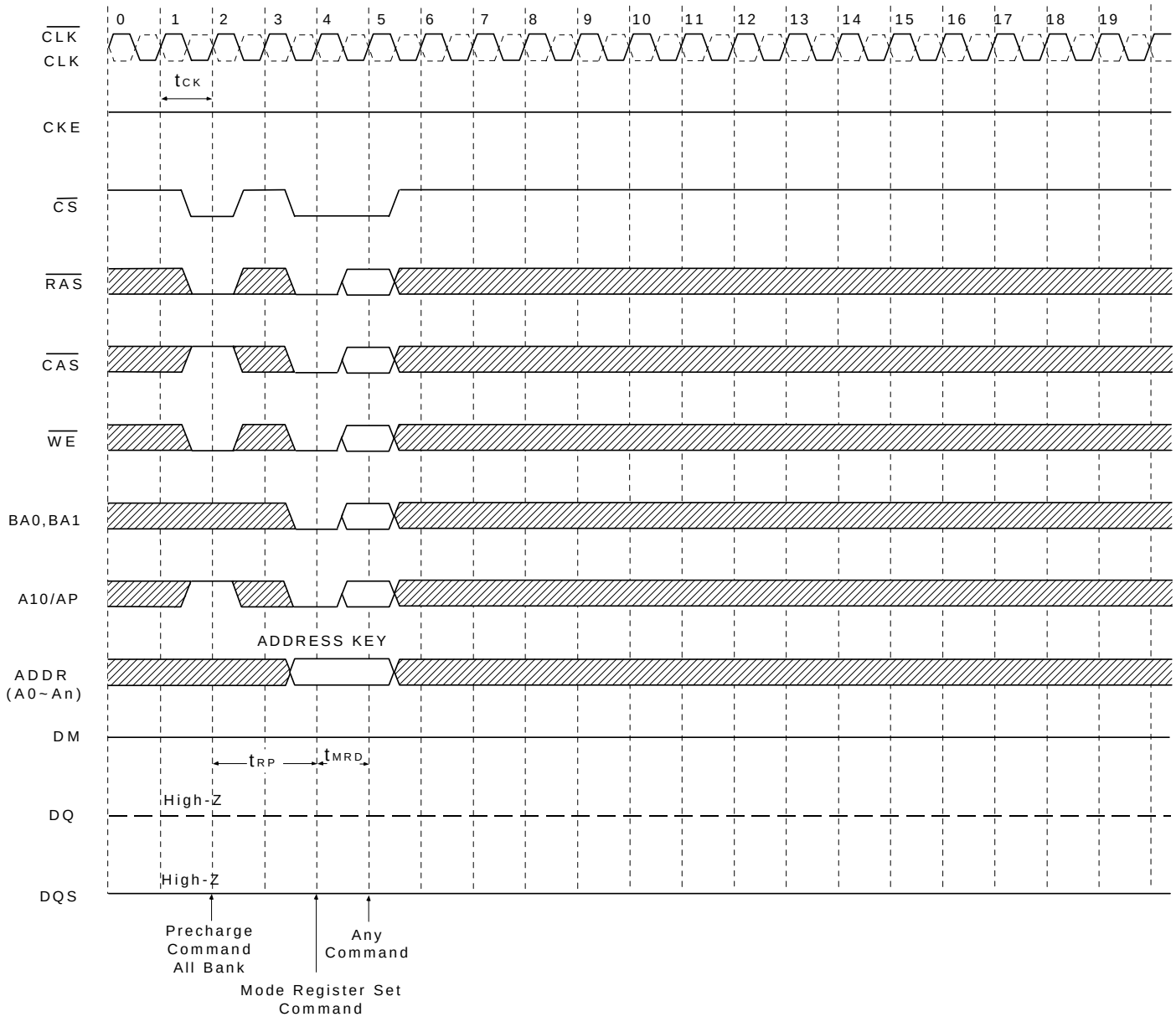
DM Function (@BL=8) only for write



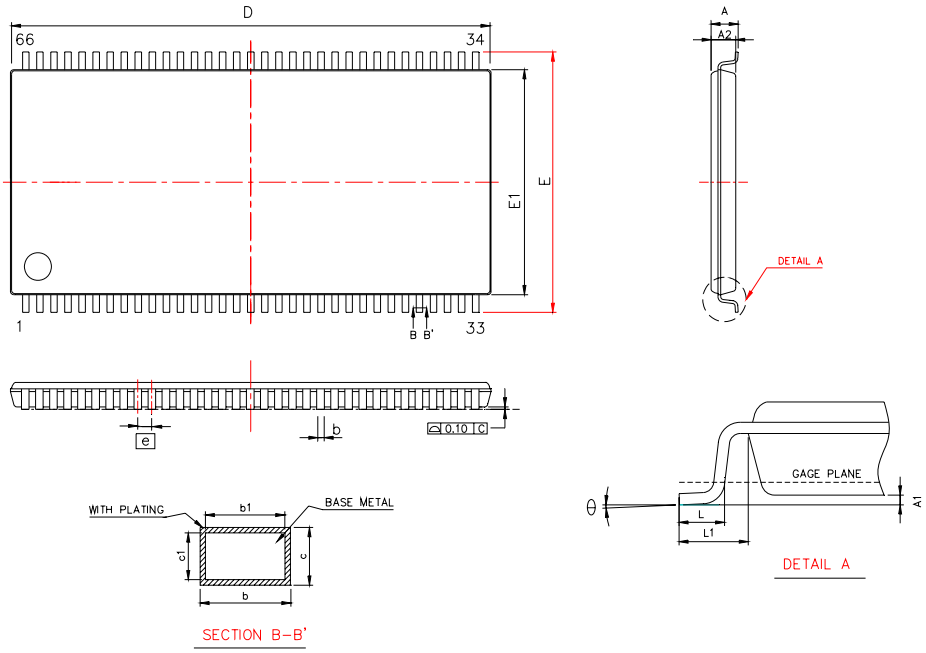
Power up & Initialization Sequence



Mode Register Set



PACKING DIMENSIONS
66-LEAD TSOP(II) DRAM(400mil)



Symbol	Dimension in inch			Dimension in mm		
	Min	Norm	Max	Min	Norm	Max
A	——	——	0.047	——	——	1.2
A1	0.002	0.004	0.006	0.05	0.1	0.15
A2	0.037	0.039	0.041	0.95	1	1.05
b	0.009	——	0.015	0.22	——	0.38
b1	0.009	0.012	0.013	0.22	0.3	0.33
c	0.005	——	0.008	0.12	——	0.21
c1	0.0047	0.005	0.006	0.12	0.127	0.16
D	0.875 BSC			22.22 BSC		
ZD	0.028 REF			0.71 REF		
E	0.455	0.463	0.471	11.56	11.76	11.96
E1	0.400 BSC			10.16 BSC		
e	0.026 BSC			0.65 BSC		
L	0.016	0.02	0.024	0.4	0.5	0.6
L1	0.031 REF			0.80 REF		
θ°	10°	15°	20°	10°	15°	20°
θ1°	10°	15°	20°	10°	15°	20°

Important Notice

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express , implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.