FAIRCHILD SEMICONDUCTOR®

September 2008

FDY1002PZ

Dual P-Channel (–1.5 V) Specified PowerTrench® MOSFET

–20 V, –0.83 A, 0.5 Ω

Features

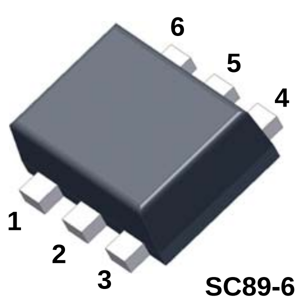
- Max $r_{DS(on)}$ = 0.5 Ω at V_{GS} = –4.5 V, I_D = –0.83 A
- Max $r_{DS(on)}$ = 0.7 Ω at V_{GS} = –2.5 V, I_D = –0.70 A
- Max $r_{DS(on)}$ = 1.2 Ω at V_{GS} = –1.8 V, I_D = –0.43 A
- Max $r_{DS(on)}$ = 1.8 Ω at V_{GS} = –1.5 V, I_D = –0.36 A
- HBM ESD protection level = 1400 V (Note 3)
- RoHS Compliant

General Description

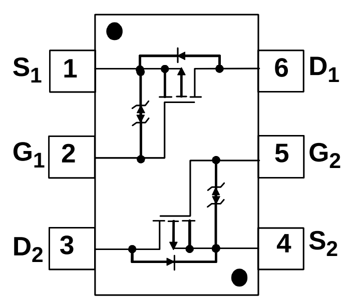
This Dual P-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the $r_{DS(on)}$@V_{GS} = –1.5 V.

Application

- Li-Ion Battery Pack



SC89-6



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		–20	V
V_{GS}	Gate to Source Voltage		±8	V
I_D	Drain Current -Continuous	(Note 1a)	–0.83	A
	-Pulsed		–1.0	
P_D	Power Dissipation	(Note 1a)	0.625	W
	Power Dissipation	(Note 1b)	0.446	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	200	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	280	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
G	FDY1002PZ	SC89-6	7 ”	8 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = –250 μA, V_{GS} = 0 V	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, referenced to 25 °C		11		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V			–1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±10	μA

On Characteristics (Note 2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = –250 μA	–0.4	–0.7	–1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = –250 μA, referenced to 25 °C		–3		mV/°C
$r_{DS(on)}$	Static Drain to Source On-Resistance	V_{GS} = –4.5 V, I_D = –0.83 A		0.28	0.5	Ω
		V_{GS} = –2.5 V, I_D = –0.70 A		0.36	0.7	
		V_{GS} = –1.8 V, I_D = –0.43 A		0.47	1.2	
		V_{GS} = –1.5 V, I_D = –0.36 A		0.62	1.8	
		V_{GS} = –4.5 V, I_D = –0.83 A, T_J =125 °C		0.39	0.85	
g_{FS}	Forward Transconductance	V_{DD} = –5 V, I_D = –0.83 A		2		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = –10 V, V_{GS} = 0 V, f = 1 MHz		100	135	pF
C_{oss}	Output Capacitance			23	35	pF
C_{rss}	Reverse Transfer Capacitance			18	30	pF

Switching Characteristics (Note 2)

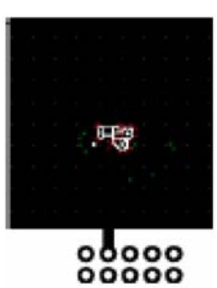
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = –10 V, I_D = –0.83 A V_{GS} = –4.5 V, R_{GEN} = 6 Ω		3.5	10	ns
t_r	Rise Time			2.9	10	ns
$t_{d(off)}$	Turn-Off Delay Time			23	37	ns
t_f	Fall Time			13	23	ns
Q_g	Total Gate Charge	V_{DD} = –10 V, I_D = –0.83 A V_{GS} = –4.5 V		2.2	3.1	nC
Q_{gs}	Gate to Source Charge			0.3		nC
Q_{gd}	Gate to Drain “Miller” Charge			0.6		nC

Drain-Source Diode Characteristics and Maximum Rating

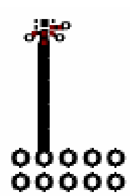
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_S	Maximum Continuous Drain-Source Diode Forward Current				–0.52	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = –0.52 A (Note 2)		–1.0	–1.2	V
t_{rr}	Reverse Recovery Time	I_F = –0.83 A, dI_F/dt = 100 A/μs		18	31	ns
Q_{rr}	Reverse Recovery Charge			3.8	10	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 200 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 280 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0%
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

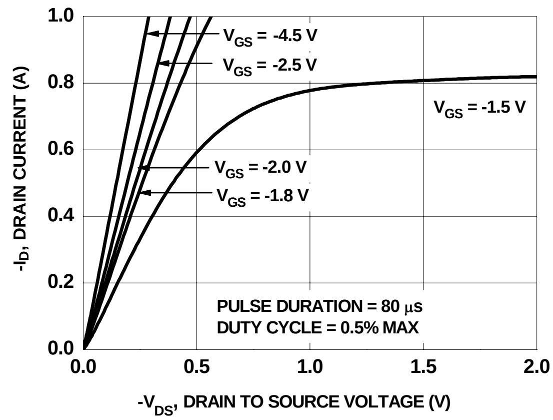


Figure 1. On Region Characteristics

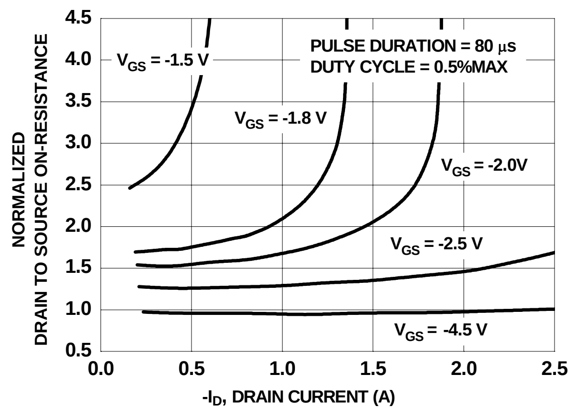


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

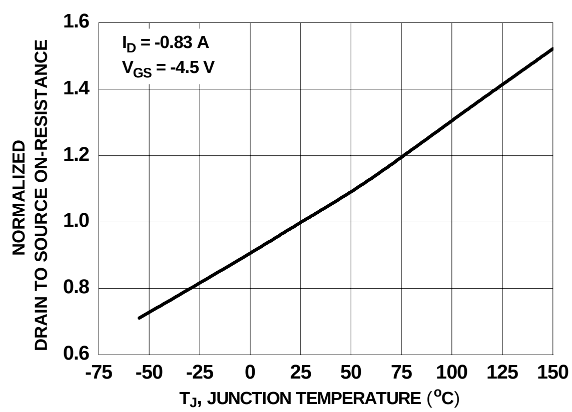


Figure 3. Normalized On Resistance vs Junction Temperature

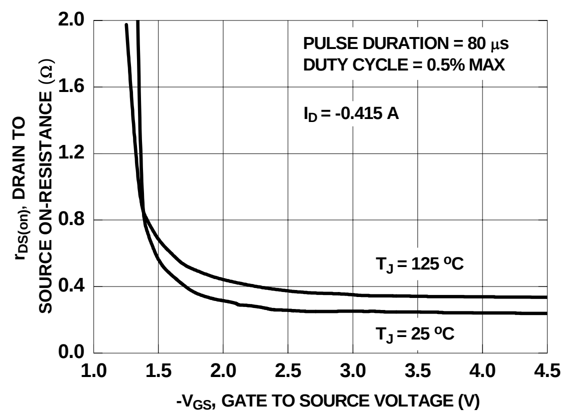


Figure 4. On-Resistance vs Gate to Source Voltage

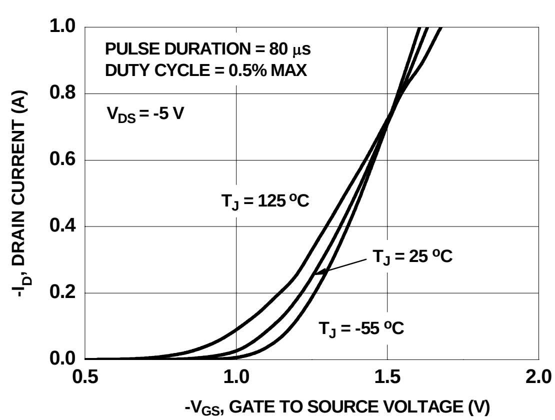


Figure 5. Transfer Characteristics

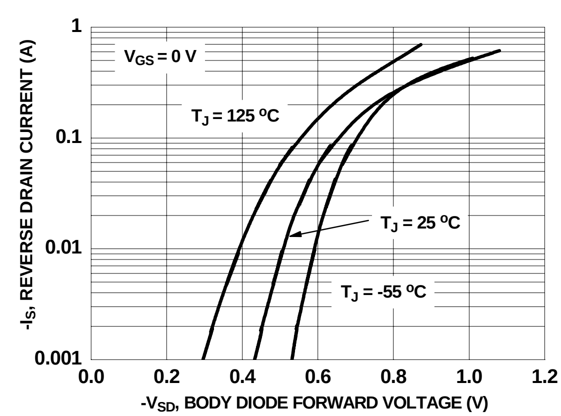


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

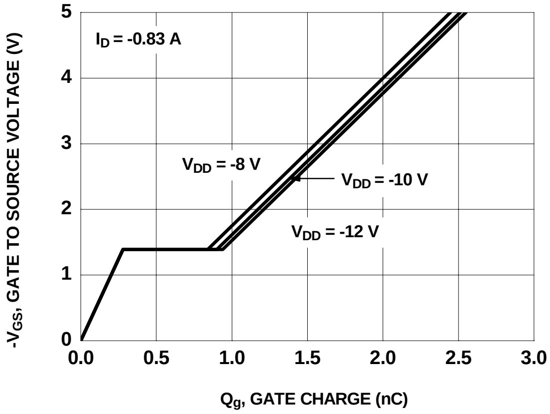


Figure 7. Gate Charge Characteristics

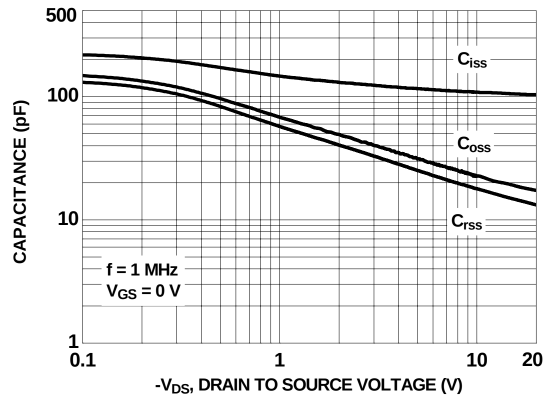


Figure 8. Capacitance vs Drain to Source Voltage

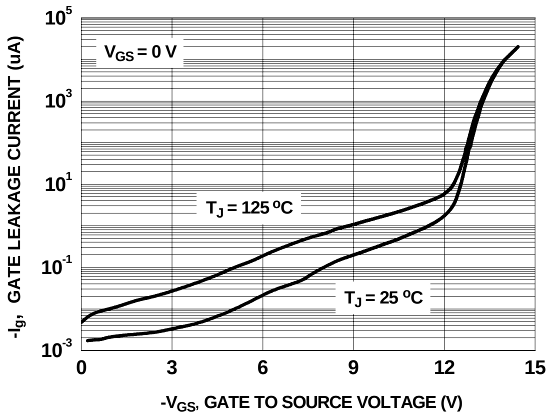


Figure 9. Gate Leakage Current vs Gate to Source Voltage

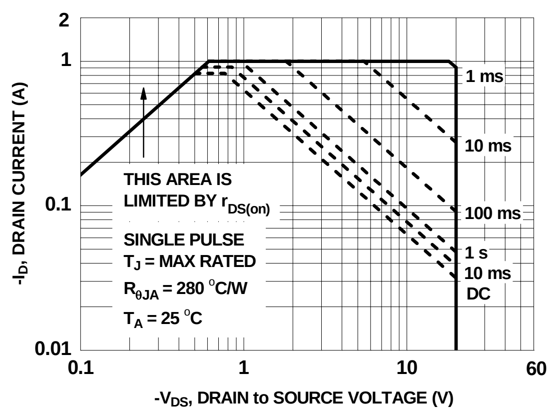


Figure 10. Forward Bias Safe Operating Area

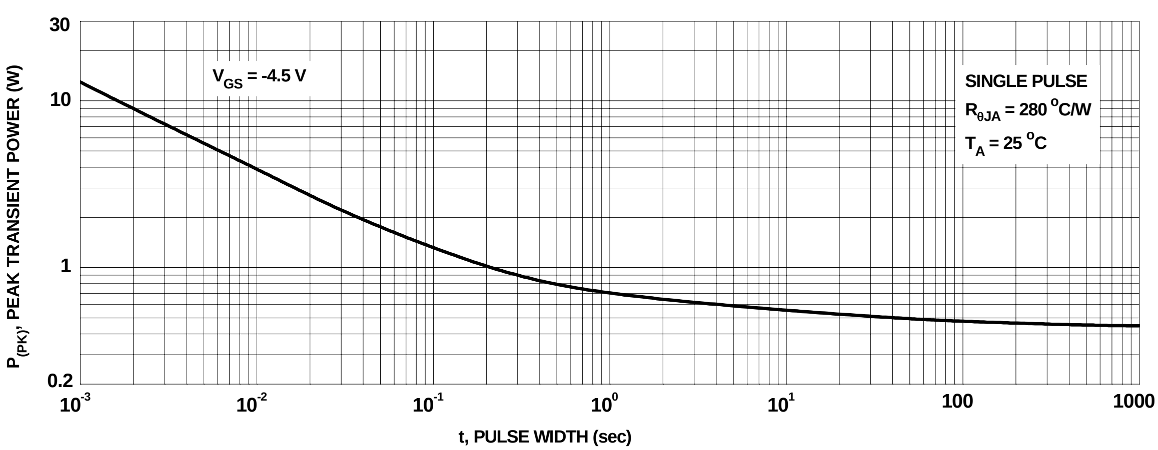


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

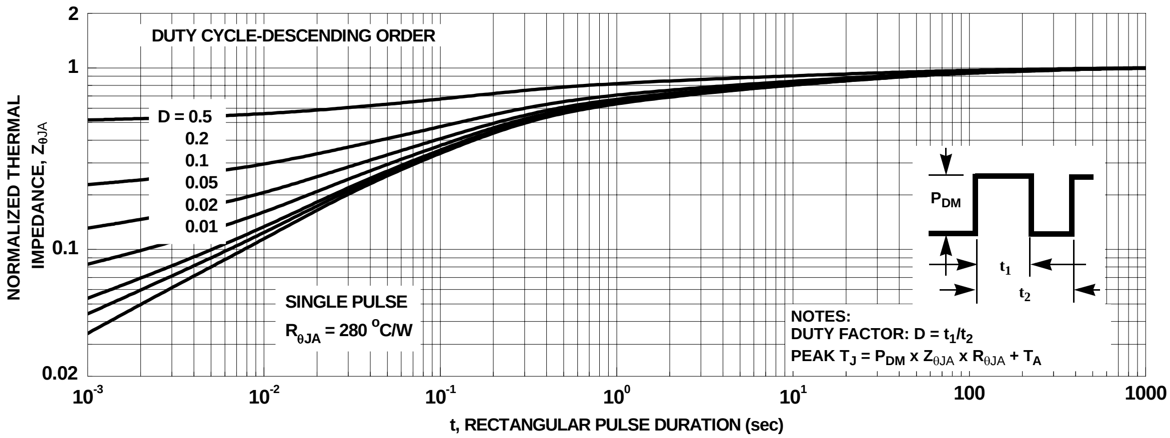
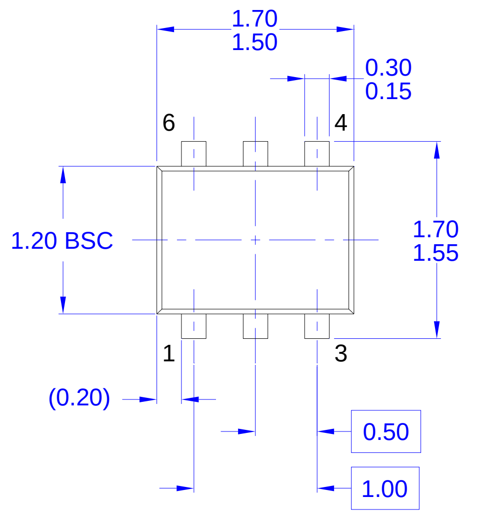
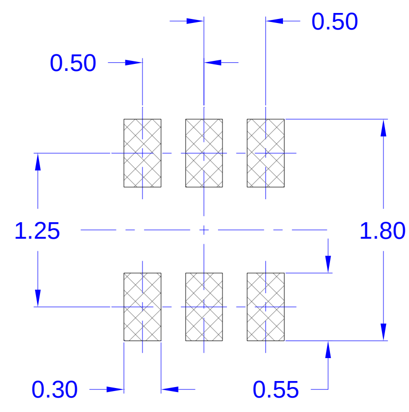


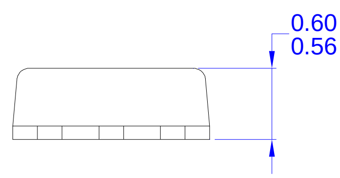
Figure 12. Junction-to-Ambient Transient Thermal Response Curve

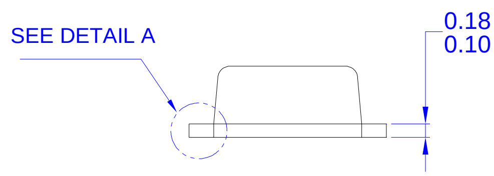
Dimensional Outline and Pad Layout

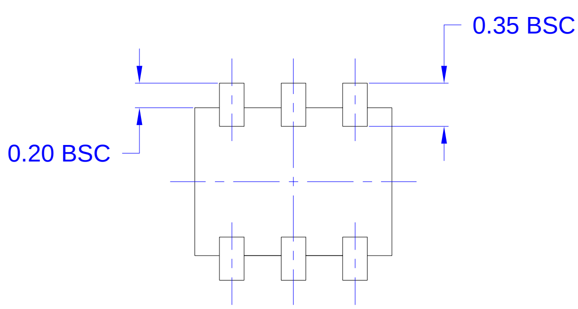


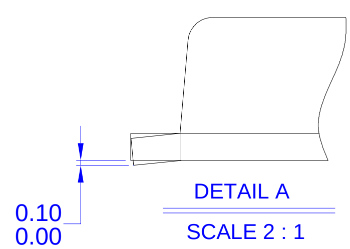


LAND PATTERN RECOMMENDATION









DETAIL A

SCALE 2 : 1

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I36