

IRFS4321PbF IRFSL4321PbF

Applications

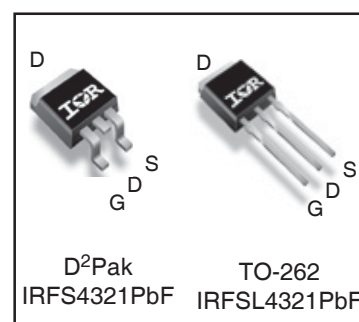
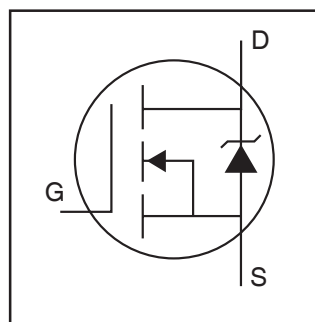
- Motion Control Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- Hard Switched and High Frequency Circuits

Benefits

- Low $R_{DS(on)}$ Reduces Losses
- Low Gate Charge Improves the Switching Performance
- Improved Diode Recovery Improves Switching & EMI Performance
- 30V Gate Voltage Rating Improves Robustness
- Fully Characterized Avalanche SOA

HEXFET® Power MOSFET

V_{DSS}	150V
$R_{DS(on)}$ typ. max.	12mΩ
	15mΩ
I_D	85A ①



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	85 ①	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	60	
I _{DM}	Pulsed Drain Current ②	330	
P _D @T _C = 25°C	Maximum Power Dissipation	350	W
	Linear Derating Factor	2.3	W/°C
V _{GS}	Gate-to-Source Voltage	±30	V
E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	120	mJ
T _J	Operating Junction and	-55 to + 175	
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	0.43*	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	40	

* $R_{\theta JC}$ (end of life) for D²Pak and TO-262 = 0.65°C/W. This is the maximum measured value after 1000 temperature cycles from -55 to 150°C and is accounted for by the physical wearout of the die attach medium.

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	150	—	mV/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	12	15	m Ω	$V_{GS} = 10V, I_D = 33A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = 150V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$
$R_{G(int)}$	Internal Gate Resistance	—	0.8	—	Ω	

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	130	—	—	S	$V_{DS} = 25V, I_D = 50A$
Q_g	Total Gate Charge	—	71	110	nC	$I_D = 50A$
Q_{gs}	Gate-to-Source Charge	—	24	—	nC	$V_{DS} = 75V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	21	—	nC	$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 98V$
t_r	Rise Time	—	60	—	ns	$I_D = 50A$
$t_{d(off)}$	Turn-Off Delay Time	—	25	—	ns	$R_G = 2.5\Omega$
t_f	Fall Time	—	35	—	ns	$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	4460	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	390	—	pF	$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	—	82	—	pF	$f = 1.0MHz$

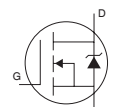
Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	85	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	330	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 50A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	89	130	ns	$I_D = 50A$
Q_{rr}	Reverse Recovery Charge	—	300	450	nC	$V_R = 128V,$
I_{RRM}	Reverse Recovery Current	—	6.5	—	A	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.096mH$
 $R_G = 25\Omega$, $I_{AS} = 50A$, $V_{GS} = 10V$. Part not recommended for use above this value.

- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑤ R_θ is measured at T_J approximately 90°C



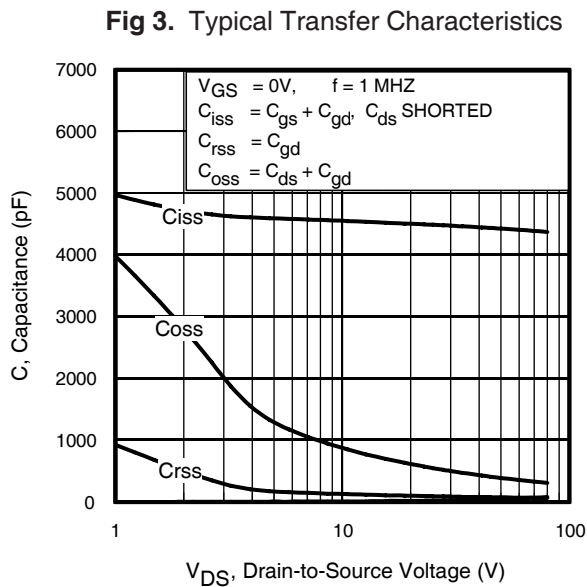
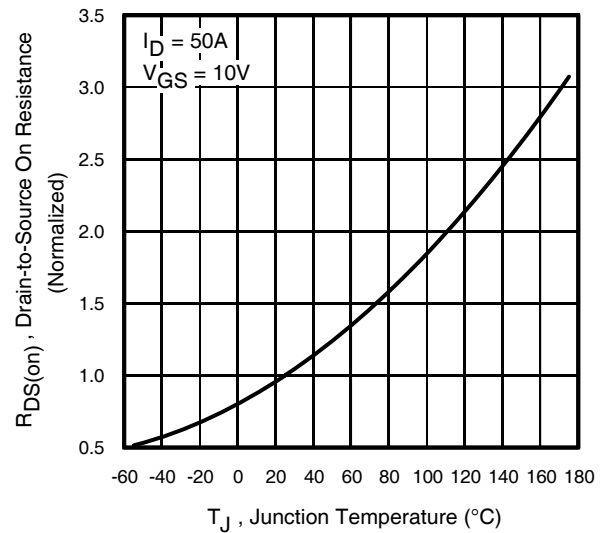
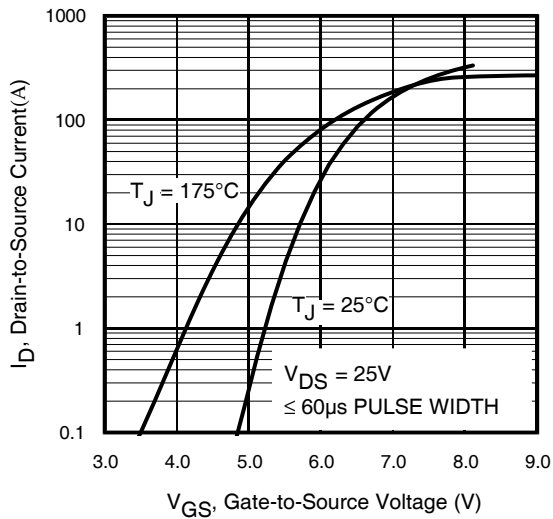
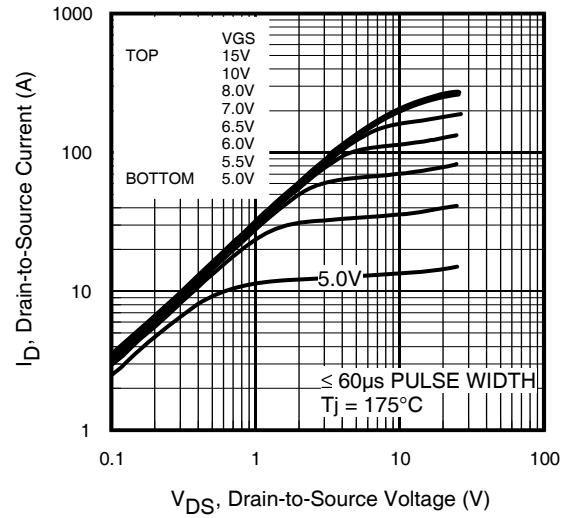
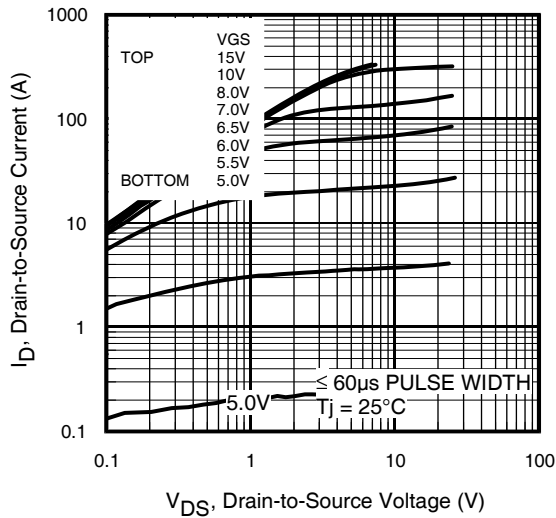
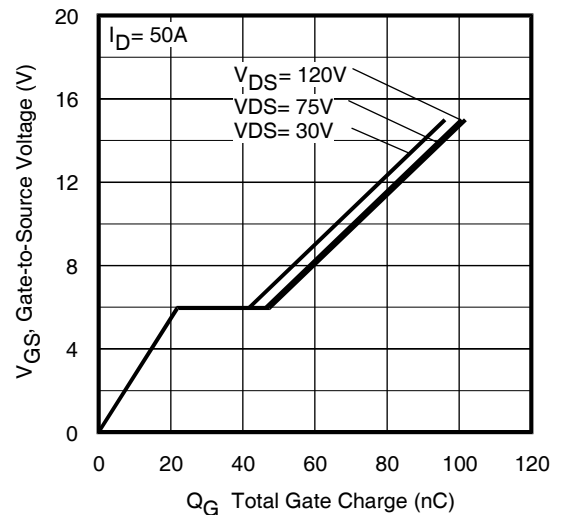


Fig 4. Normalized On-Resistance vs. Temperature



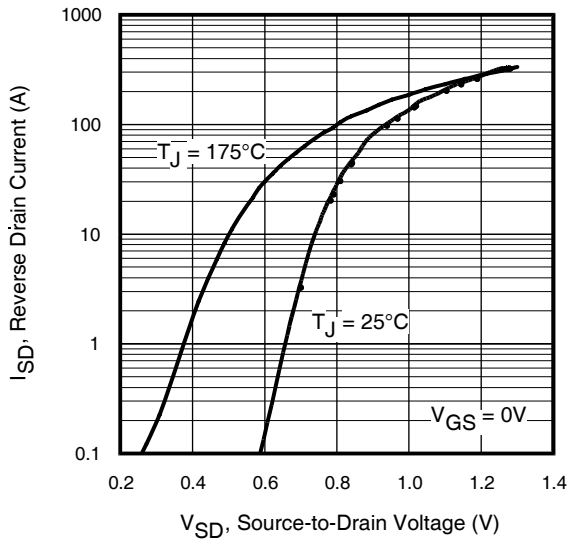


Fig 7. Typical Source-Drain Diode Forward Voltage

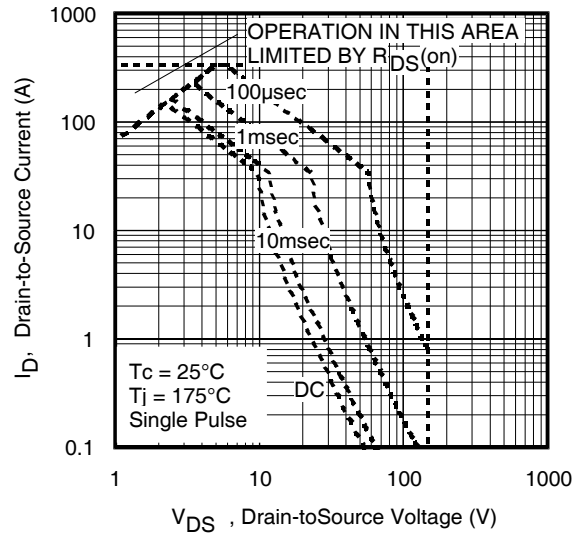


Fig 8. Maximum Safe Operating Area

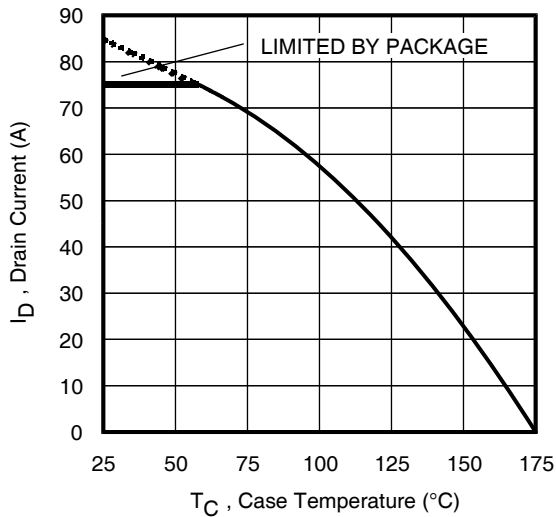


Fig 9. Maximum Drain Current vs. Case Temperature

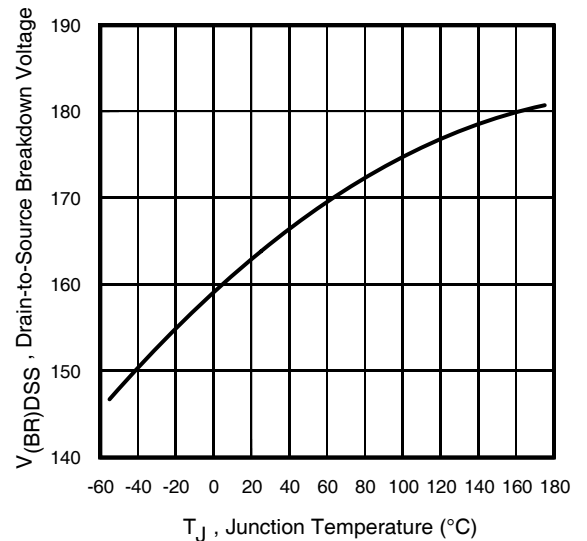


Fig 10. Drain-to-Source Breakdown Voltage

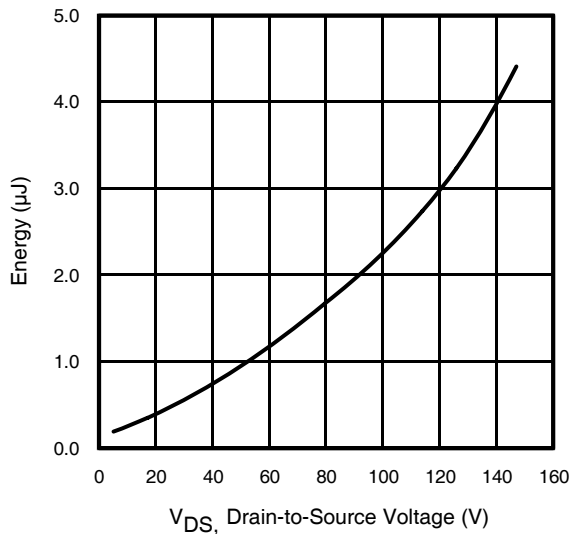


Fig 11. Typical C_{OSS} Stored Energy

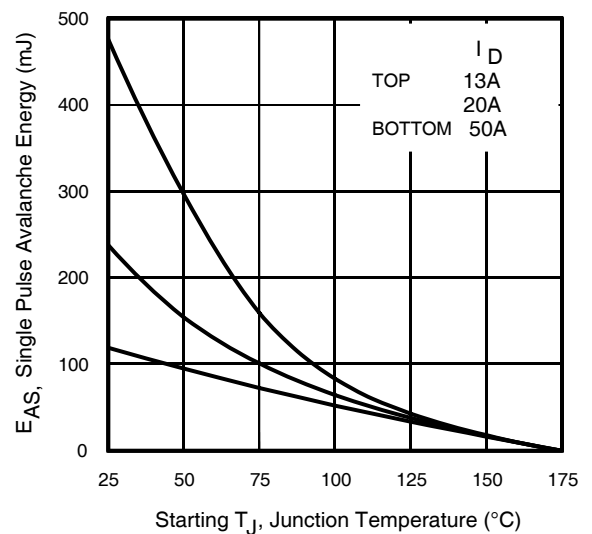


Fig 12. Maximum Avalanche Energy Vs. Drain Current
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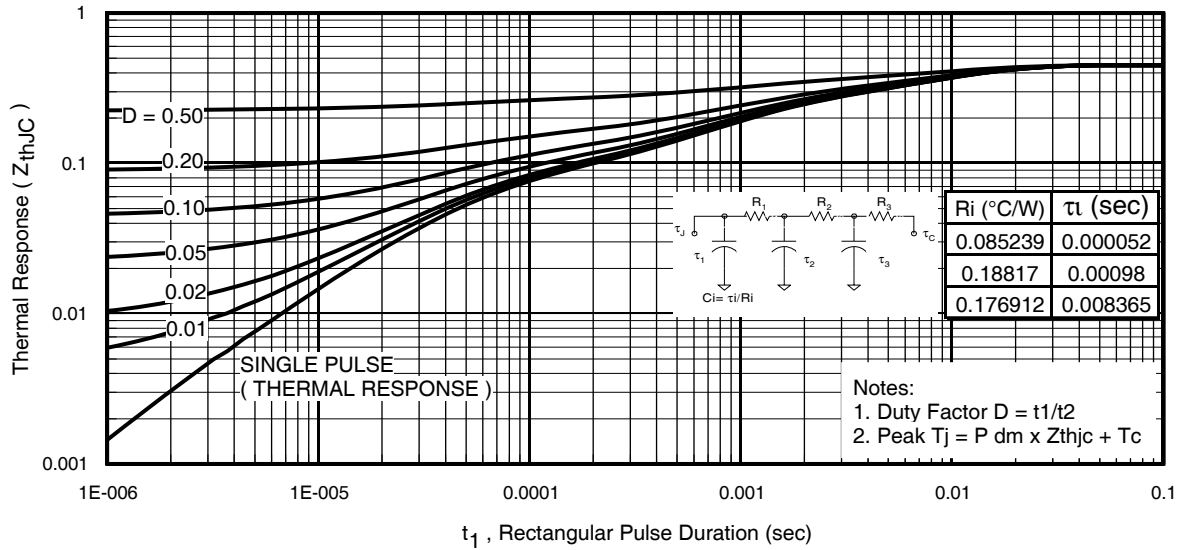


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

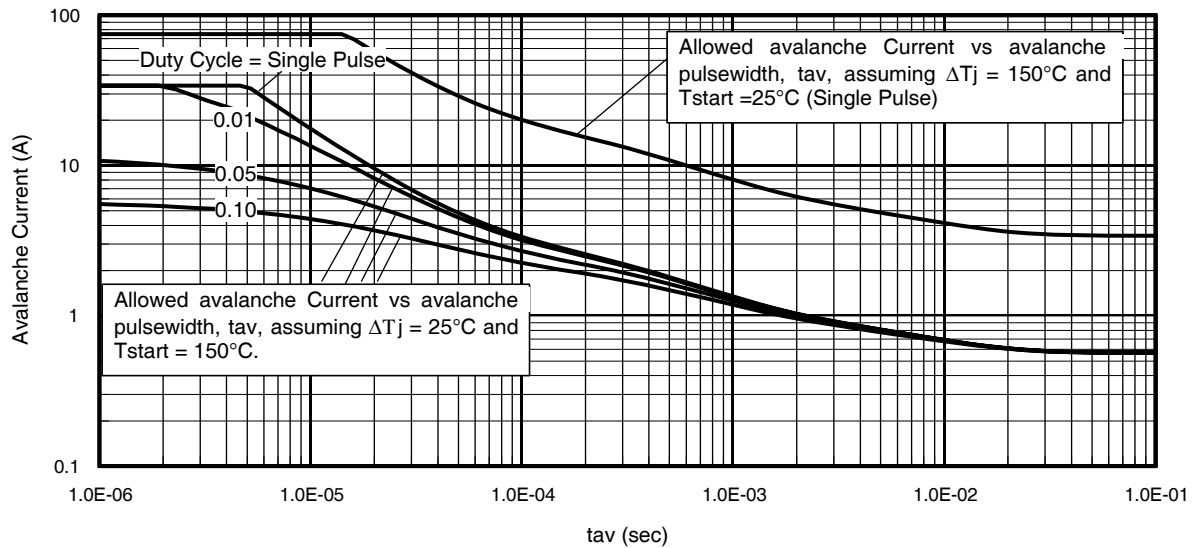


Fig 14. Typical Avalanche Current vs. Pulsewidth

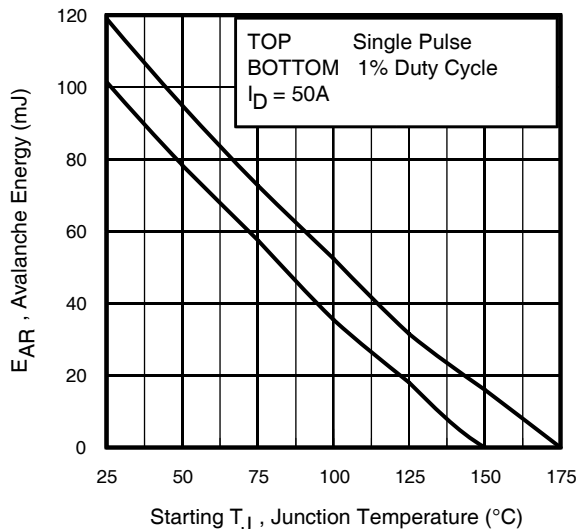


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

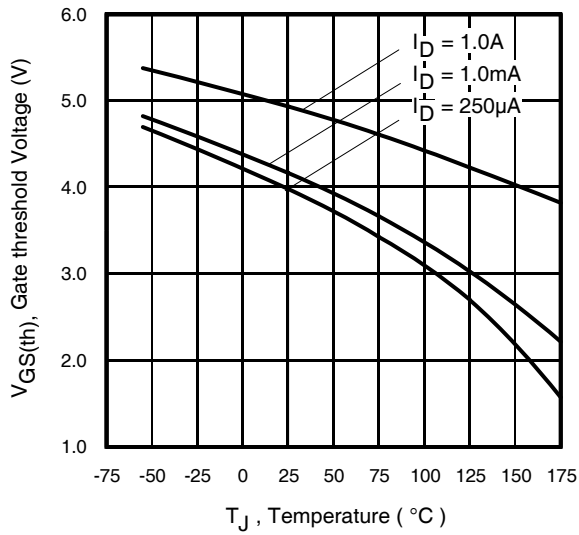


Fig 16. Threshold Voltage Vs. Temperature

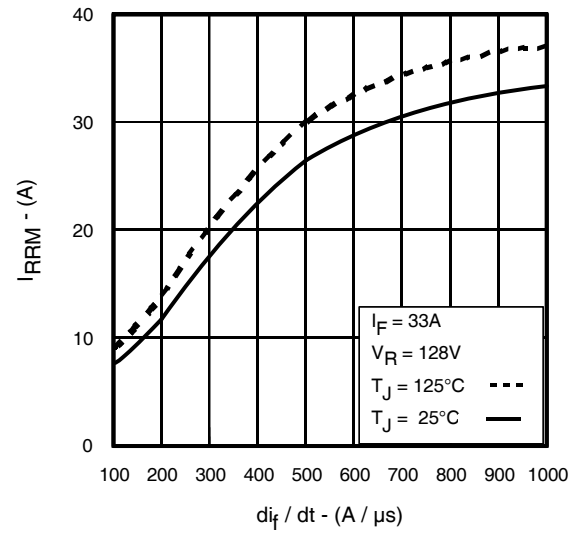


Fig. 17 - Typical Recovery Current vs. di_f/dt

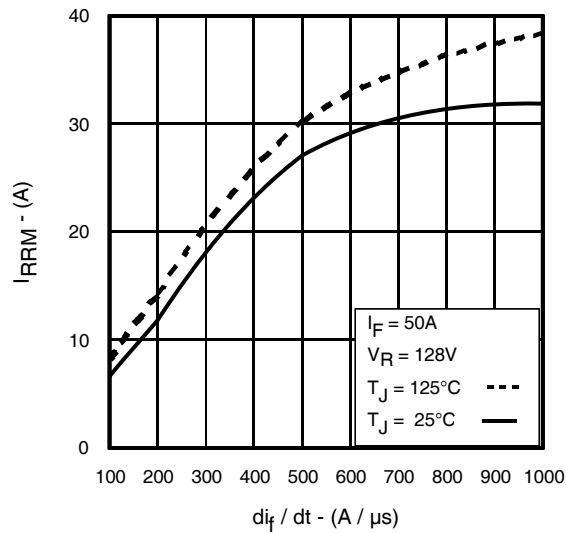


Fig. 18 - Typical Recovery Current vs. di_f/dt

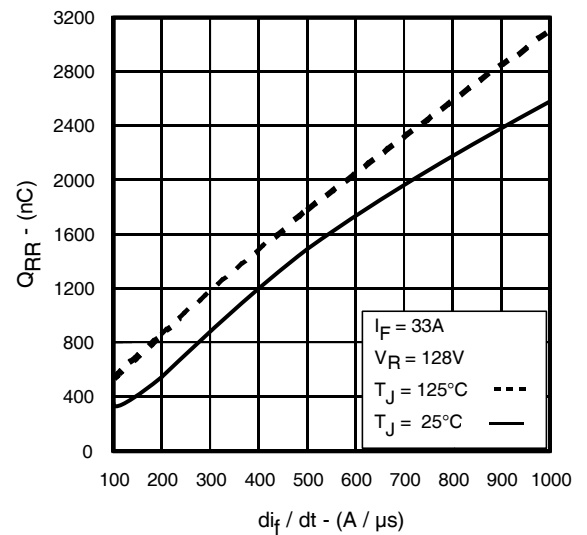


Fig. 19 - Typical Stored Charge vs. di_f/dt

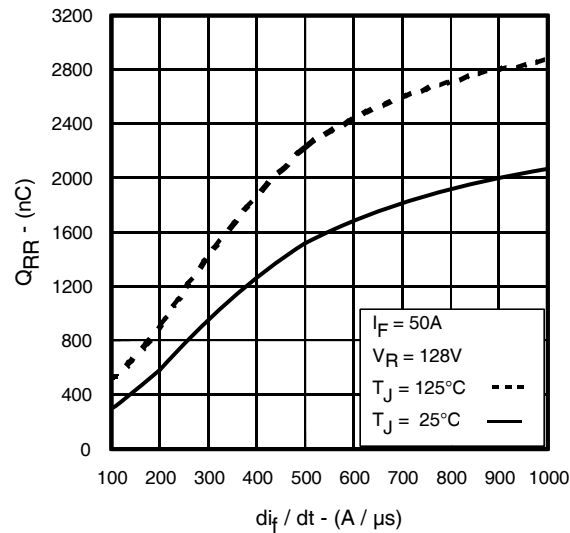


Fig. 20 - Typical Stored Charge vs. di_f/dt

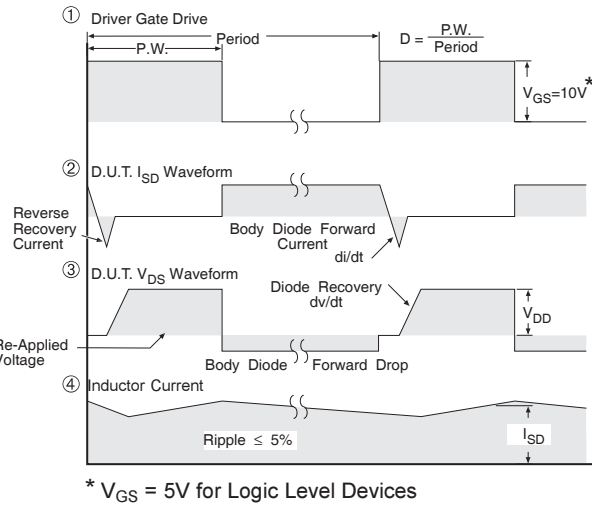
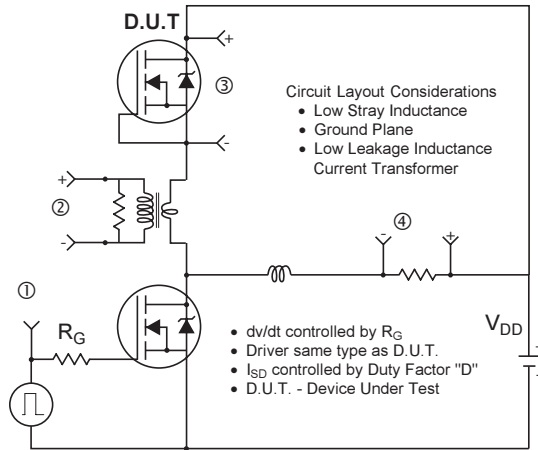


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

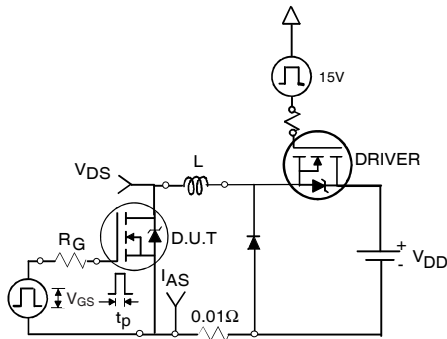


Fig 22a. Unclamped Inductive Test Circuit



Fig 22b. Unclamped Inductive Waveforms

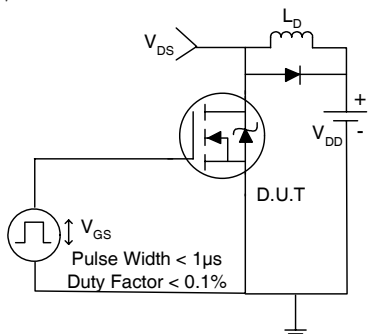


Fig 23a. Switching Time Test Circuit

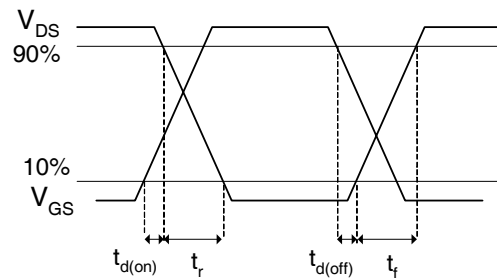


Fig 23b. Switching Time Waveforms

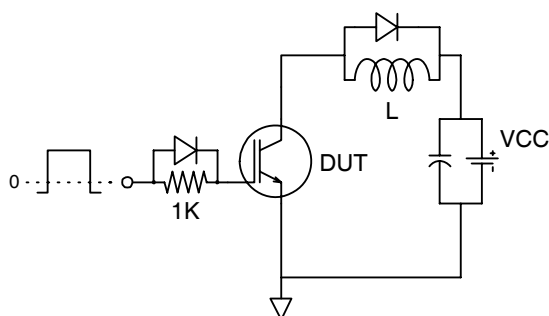
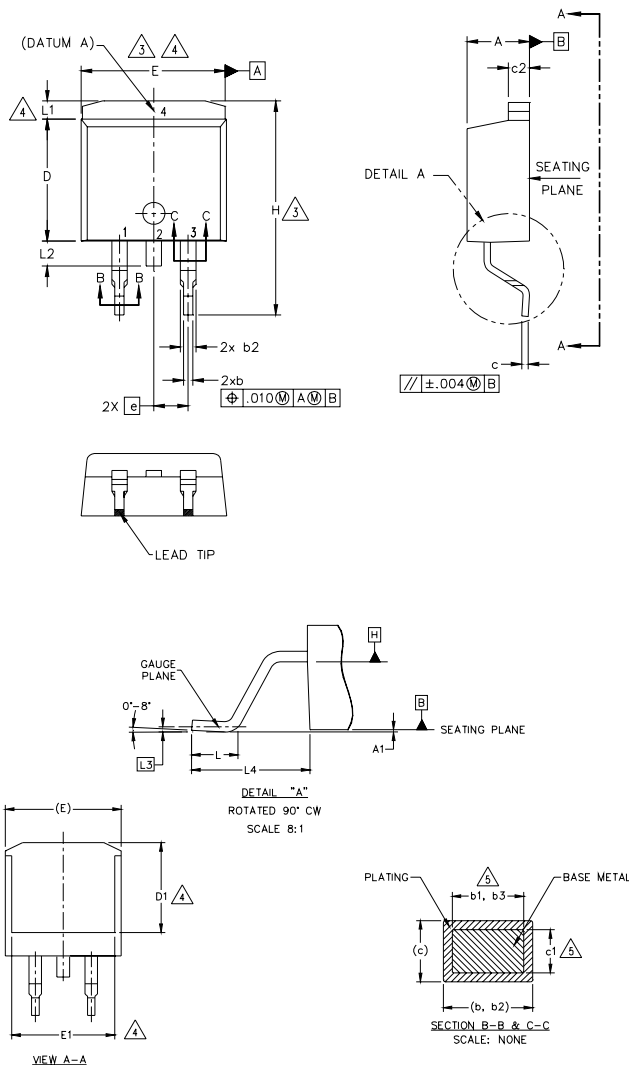


Fig 24a. Gate Charge Test Circuit



Fig 24b. Gate Charge Waveform

D²Pak Package Outline (Dimensions are shown in millimeters (inches))

S Y M B O L	DIMENSIONS				N O T E S
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	3
D	8.38	9.65	.330	.380	
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.65	—	.066	
L2	1.27	1.78	—	.070	4
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

DIODES

- 1.— ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.— CATHODE
3.— ANODE

HEXFET

- 1.— GATE
2, 4.— DRAIN
3.— SOURCE

IGBTs, CoPACK

- 1.— GATE
2, 4.— COLLECTOR
3.— EMITTER

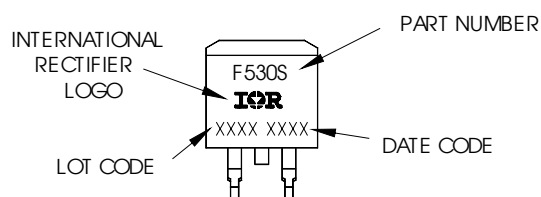
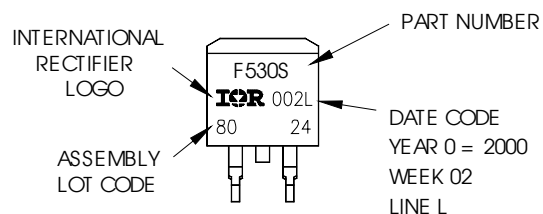
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

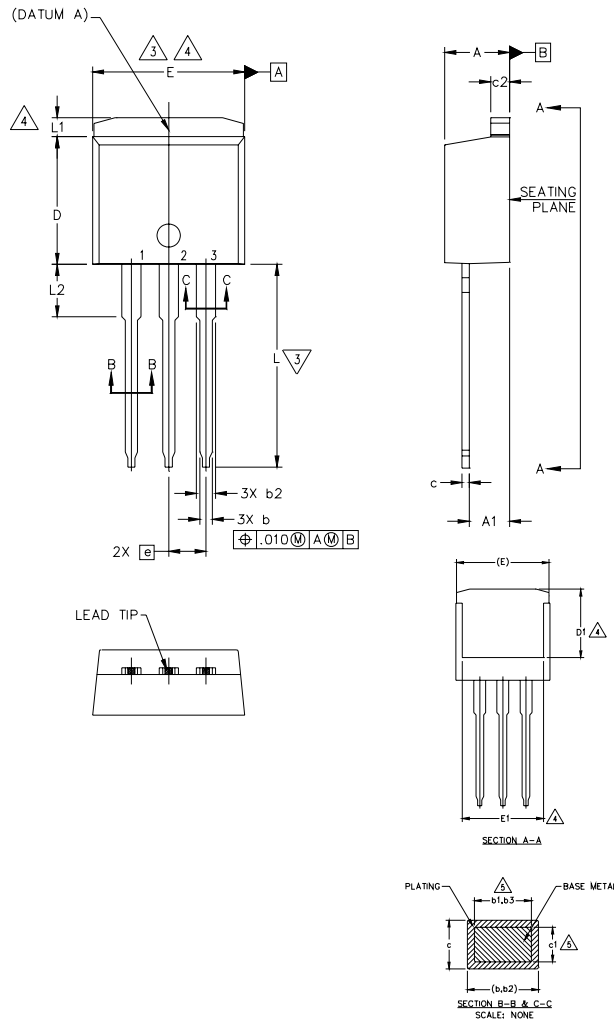
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW02, 2000
IN THE ASSEMBLY LINE "L"

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
For GB Production
ASSEMBLED ON WW02, 2000
IN THE ASSEMBLY LINE "L"



TO-262 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	—	1.65	—	.065	4
L2	3.56	3.71	.140	.146	

LEAD ASSIGNMENTS

HEXFET

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

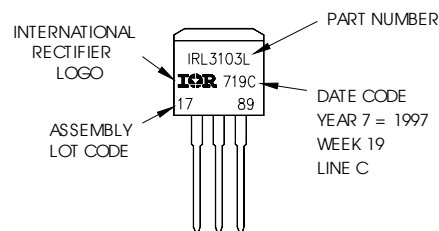
IGBTs, CoPACK

1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

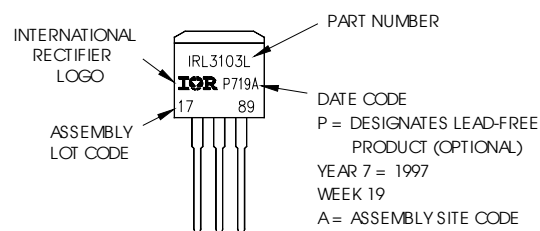
TO-262 Part Marking Infor

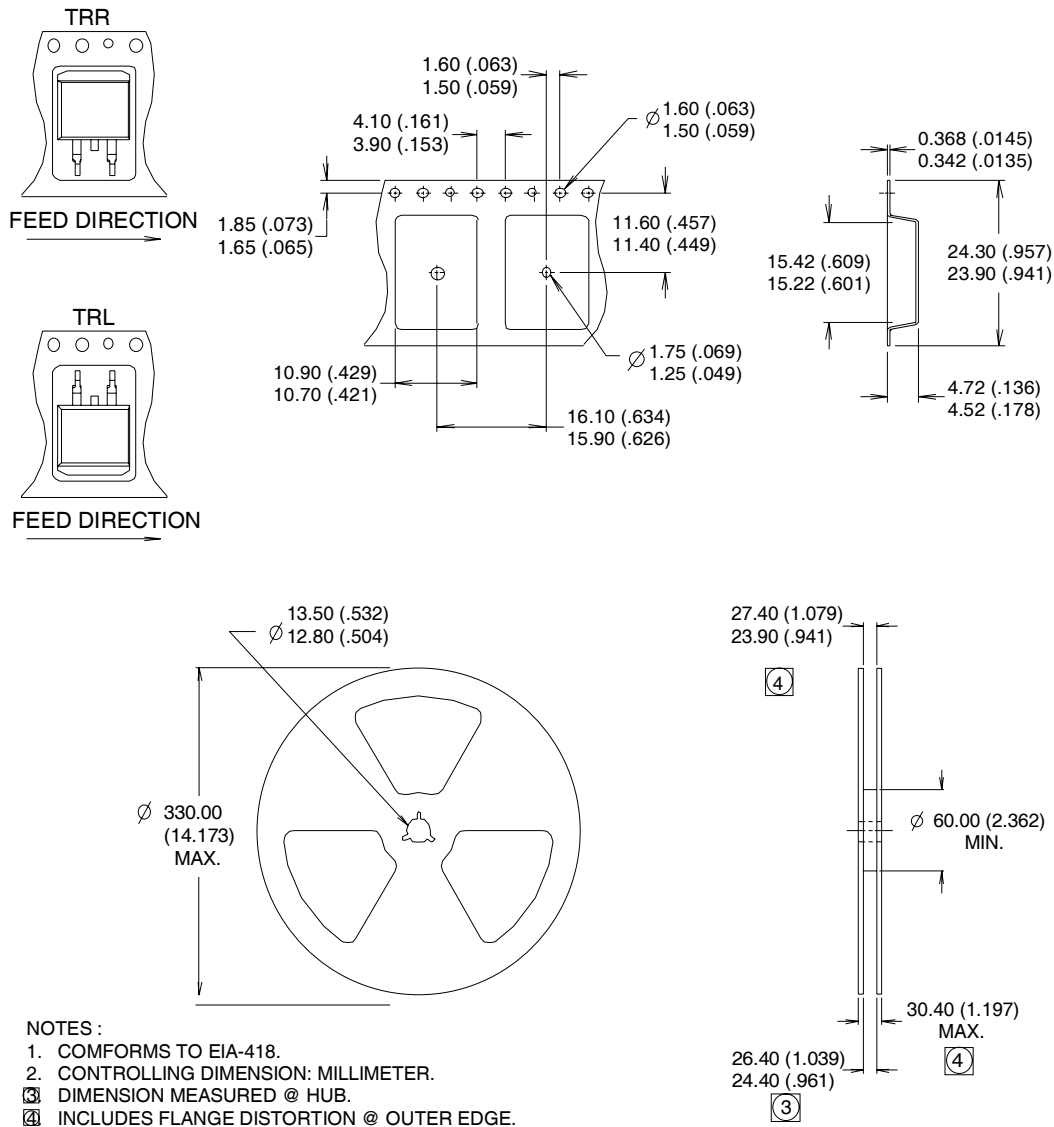
EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position
indicates "Lead - Free"



OR



D²Pak Tape & Reel Information

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

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