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## FDMS0302S

### N-Channel PowerTrench® SyncFET™

30 V, 49 A, 1.9 mΩ

#### Features

- Max  $r_{DS(on)}$  = 1.9 mΩ at  $V_{GS}$  = 10 V,  $I_D$  = 28 A
- Max  $r_{DS(on)}$  = 2.4 mΩ at  $V_{GS}$  = 4.5 V,  $I_D$  = 23 A
- Advanced Package and Silicon Combination for Low  $r_{DS(on)}$  and High Efficiency
- SyncFET Schottky Body Diode
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

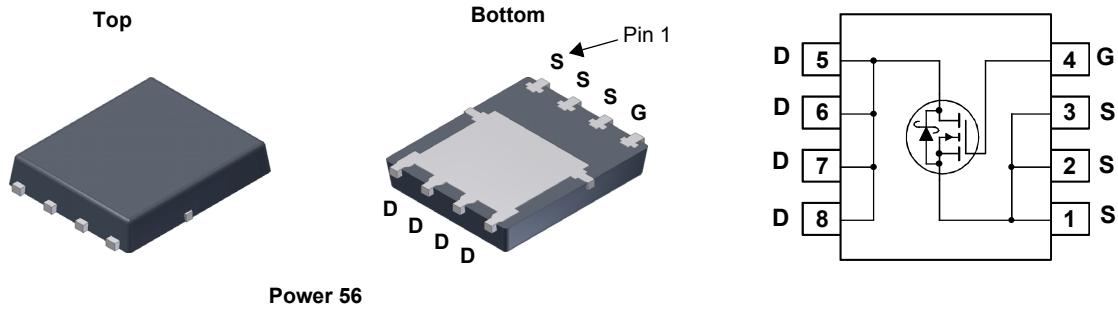


#### General Description

The FDMS0302S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

#### Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/ GPU Low Side Switch
- Networking Point of Load Low Side Switch



#### MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage (Note 4)	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C$ = 25 °C	49	A
	-Continuous (Silicon limited) $T_C$ = 25 °C	177	
	-Continuous $T_A$ = 25 °C (Note 1a)	29	
	-Pulsed	150	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	162	mJ
$P_D$	Power Dissipation $T_C$ = 25 °C	89	W
	Power Dissipation $T_A$ = 25 °C (Note 1a)	2.5	
$T_J$ , $T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

#### Thermal Characteristics

$R_{QJC}$	Thermal Resistance, Junction to Case	1.4	°C/W
$R_{QJA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS0302S	FDMS0302S	Power 56	13 "	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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**Off Characteristics**

$\text{BV}_{\text{DSS}}$	Drain to Source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{\text{GS}} = 0 \text{ V}$	30			V
$\text{BV}_{\text{DSSt}}$	Drain to Source Breakdown Voltage (transient)	$V_{\text{GS}} = 0 \text{ V}, I_{\text{D(aval)}} = 8.6 \text{ A}, T_{\text{case}} = 25^\circ\text{C}, t_{\text{transient}} = 10 \text{ ns}$	34			V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10 \text{ mA}, \text{referenced to } 25^\circ\text{C}$		23		$\text{mV}^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{\text{DS}} = 24 \text{ V}, V_{\text{GS}} = 0 \text{ V}$			500	$\mu\text{A}$
$I_{\text{GSS}}$	Gate to Source Leakage Current, Forward	$V_{\text{GS}} = 20 \text{ V}, V_{\text{DS}} = 0 \text{ V}$			100	$\text{nA}$

**On Characteristics (Note 2)**

$V_{\text{GS(th)}}$	Gate to Source Threshold Voltage	$V_{\text{GS}} = V_{\text{DS}}, I_D = 1 \text{ mA}$	1.2	1.7	3.0	V
$\frac{\Delta V_{\text{GS(th)}}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 10 \text{ mA}, \text{referenced to } 25^\circ\text{C}$		-5		$\text{mV}^\circ\text{C}$
$r_{\text{DS(on)}}$	Static Drain to Source On Resistance	$V_{\text{GS}} = 10 \text{ V}, I_D = 28 \text{ A}$		1.5	1.9	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5 \text{ V}, I_D = 23 \text{ A}$		1.9	2.4	
		$V_{\text{GS}} = 10 \text{ V}, I_D = 28 \text{ A}, T_J = 125^\circ\text{C}$		2.0	2.6	
$g_{\text{FS}}$	Forward Transconductance	$V_{\text{DS}} = 5 \text{ V}, I_D = 28 \text{ A}$		181		S

**Dynamic Characteristics**

$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}} = 15 \text{ V}, V_{\text{GS}} = 0 \text{ V}, f = 1 \text{ MHz}$		5525	7350	pF
$C_{\text{oss}}$	Output Capacitance			2020	2685	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance			150	230	pF
$R_g$	Gate Resistance			0.4	0.9	$\Omega$

**Switching Characteristics**

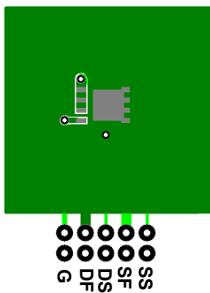
$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}} = 15 \text{ V}, I_D = 28 \text{ A}, V_{\text{GS}} = 10 \text{ V}, R_{\text{GEN}} = 6 \Omega$		20	36	ns
$t_r$	Rise Time			8	17	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time			43	70	ns
$t_f$	Fall Time			5	10	ns
$Q_g$	Total Gate Charge	$V_{\text{GS}} = 0 \text{ V to } 10 \text{ V}$		78	109	nC
	Total Gate Charge		$V_{\text{DD}} = 15 \text{ V}, I_D = 28 \text{ A}$	35	49	nC
$Q_{\text{gs}}$	Gate to Source Gate Charge			16.4		nC
$Q_{\text{gd}}$	Gate to Drain "Miller" Charge			6.6		nC

**Drain-Source Diode Characteristics**

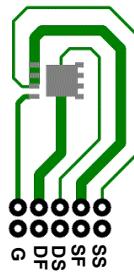
$V_{\text{SD}}$	Source to Drain Diode Forward Voltage	$V_{\text{GS}} = 0 \text{ V}, I_S = 2 \text{ A}$	(Note 2)	0.38	0.7	V
		$V_{\text{GS}} = 0 \text{ V}, I_S = 28 \text{ A}$	(Note 2)	0.74	1.2	
$t_{\text{rr}}$	Reverse Recovery Time	$I_F = 28 \text{ A}, \text{di/dt} = 300 \text{ A}/\mu\text{s}$		46	75	ns
				73	117	

## Notes:

1.  $R_{\text{JJA}}$  is determined with the device mounted on a  $1 \text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5 \text{ in.}$  board of FR-4 material.  $R_{\text{JCA}}$  is guaranteed by design while  $R_{\text{JCA}}$  is determined by the user's board design.



a.  $50^\circ\text{C}/\text{W}$  when mounted on a  $1 \text{ in}^2$  pad of 2 oz copper.



b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width  $< 300 \mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3.  $E_{\text{AS}}$  of 162 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 1 \text{ mH}$ ,  $I_{\text{AS}} = 18 \text{ A}$ ,  $V_{\text{DD}} = 27 \text{ V}$ ,  $V_{\text{GS}} = 10 \text{ V}$ . 100% test at  $L = 0.3 \text{ mH}$ ,  $I_{\text{AS}} = 28 \text{ A}$ .

4. As an N-ch device, the negative  $V_{\text{GS}}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

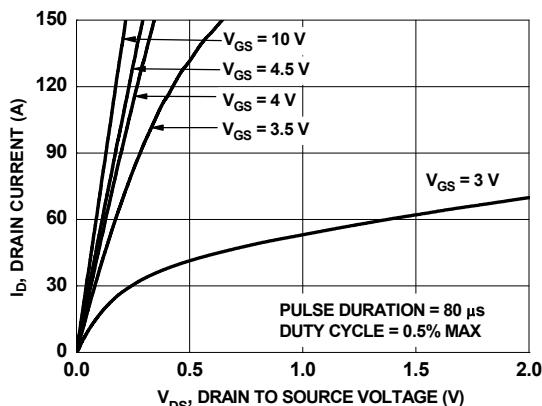


Figure 1. On-Region Characteristics

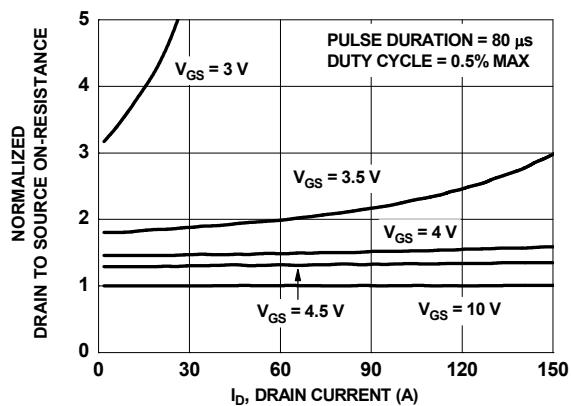


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

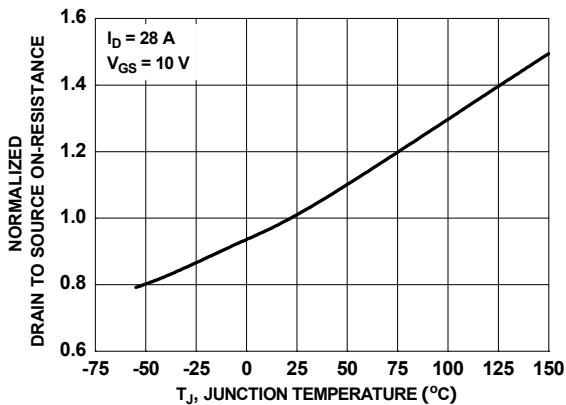


Figure 3. Normalized On-Resistance vs. Junction Temperature

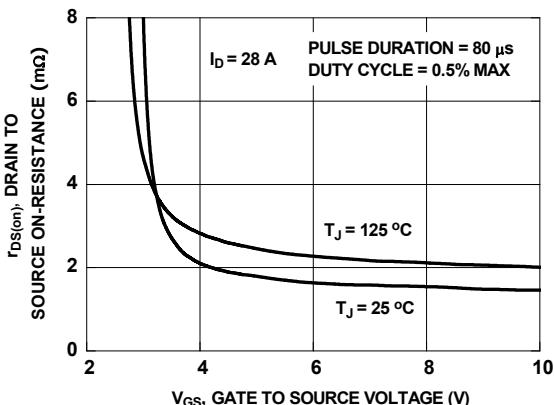


Figure 4. On-Resistance vs. Gate to Source Voltage

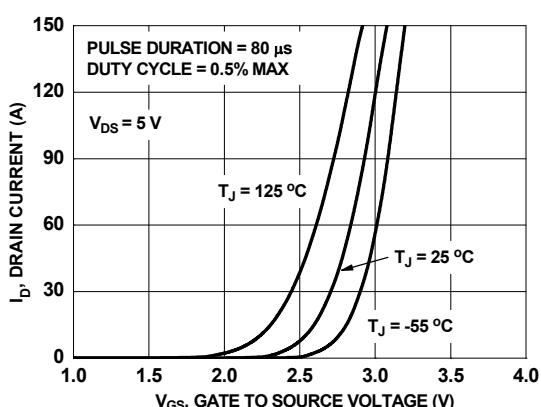


Figure 5. Transfer Characteristics

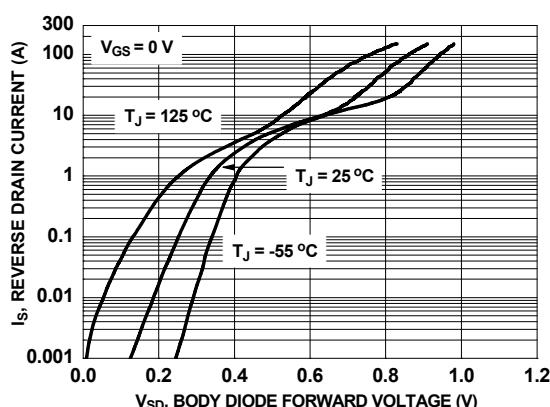


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

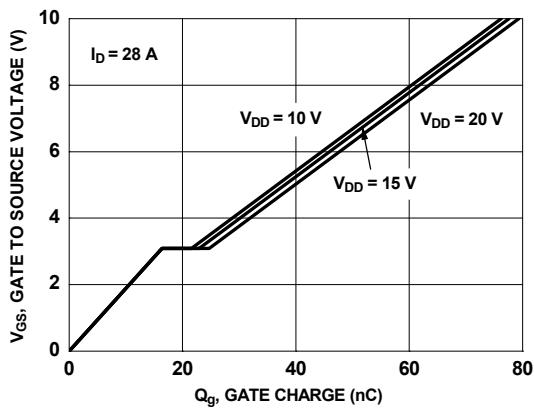


Figure 7. Gate Charge Characteristics

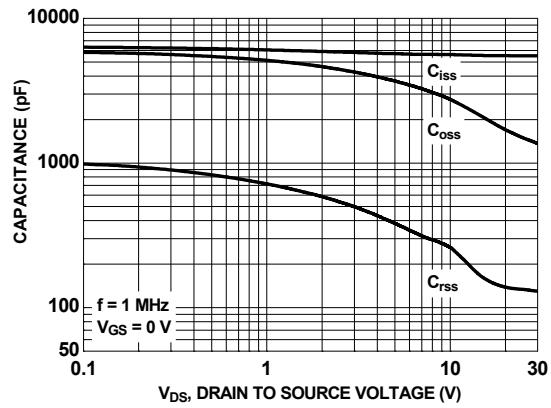


Figure 8. Capacitance vs. Drain to Source Voltage

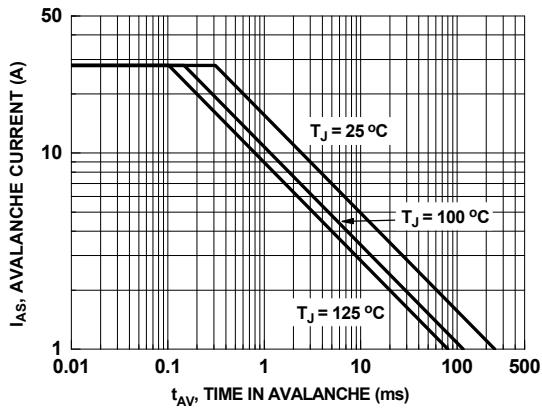


Figure 9. Unclamped Inductive Switching Capability

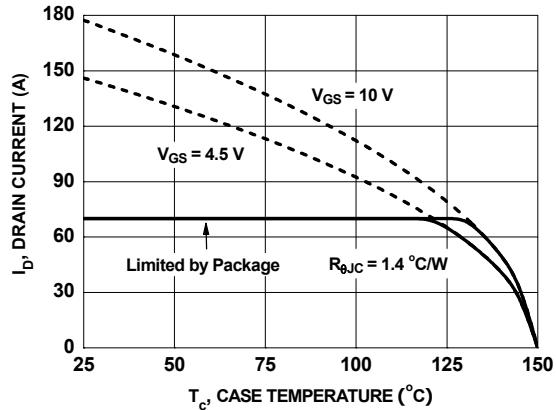


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

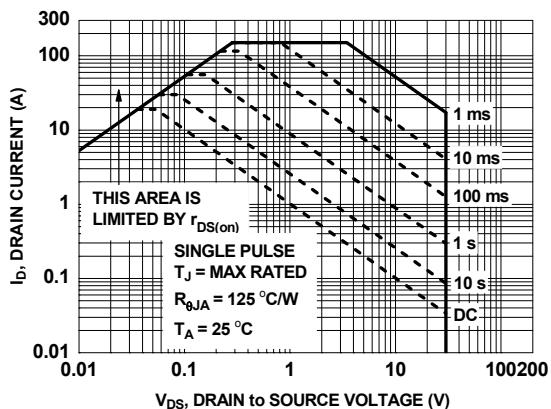


Figure 11. Forward Bias Safe Operating Area

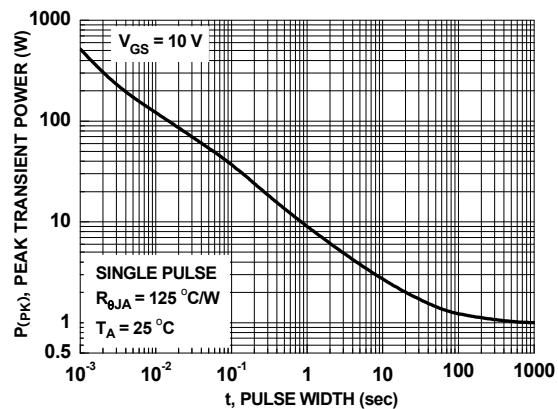


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics  $T_J = 25^\circ\text{C}$  unless otherwise noted.

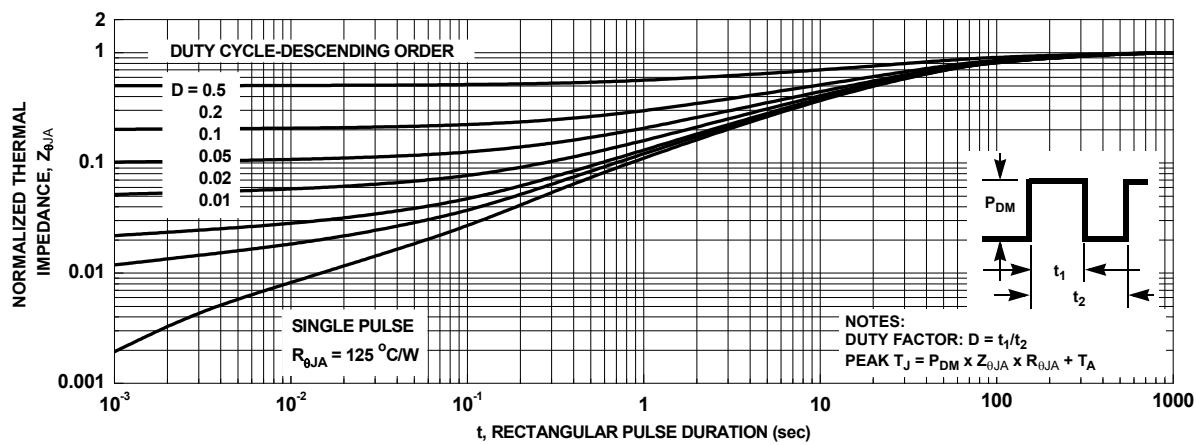


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

## Typical Characteristics (continued)

### SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MoSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS0302S.

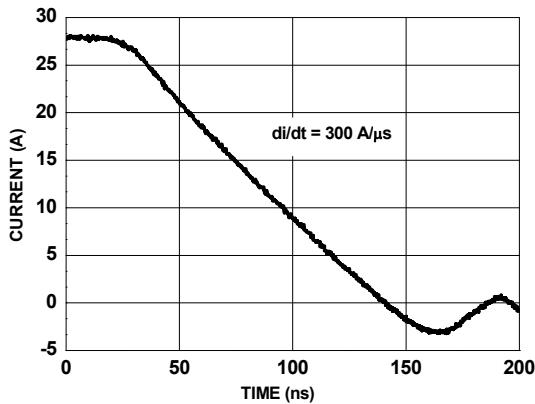


Figure 14. FDMS0302S SyncFET Body Diode Reverse Recovery Characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

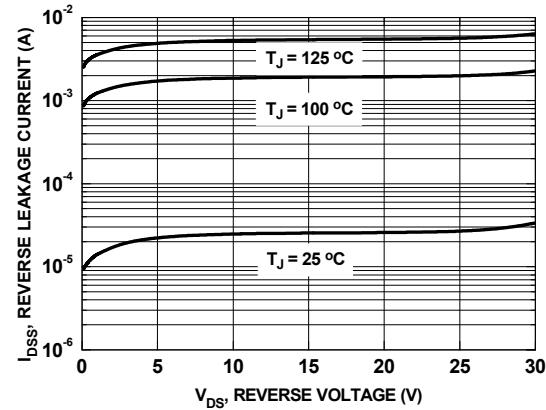
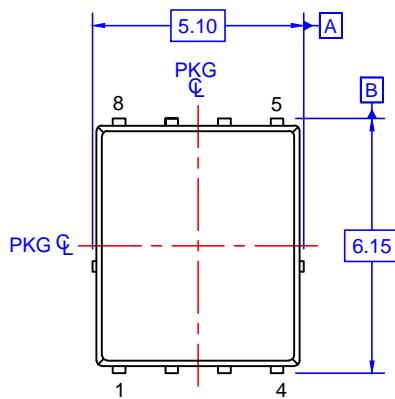
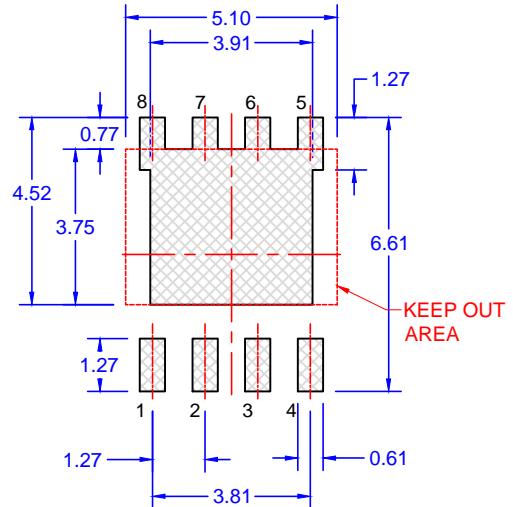
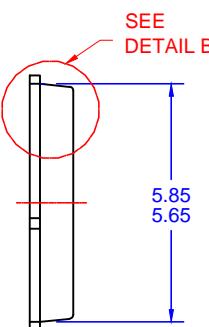


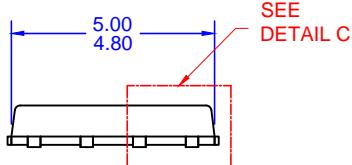
Figure 15. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage



### TOP VIEW

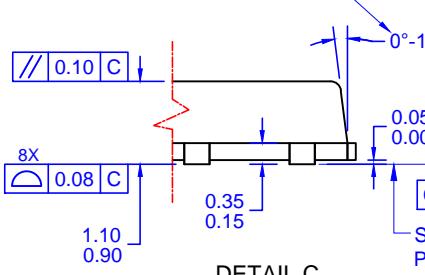


## LAND PATTERN RECOMMENDATION

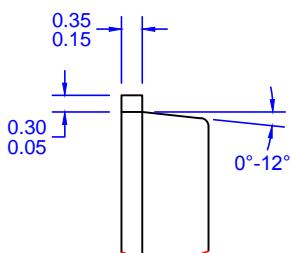


### SIDE VIEW

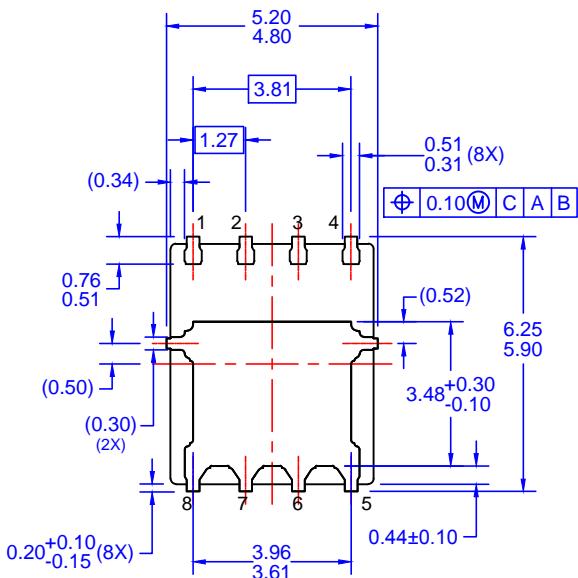
OPTIONAL DRAFT  
ANGLE MAY APPEAR  
ON FOUR SIDES  
OF THE PACKAGE



DETAIL C



DETAIL B



### BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240,  
ISSUE A, VAR. AA.,
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.  
MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR  
VIAS WITHIN THE KEEF OUT AREA.

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