Ordering number : ENA1551A

ATP204

N-Channel Power MOSFET
30V, 100A, 5.6mΩ, Single ATPAK

ON Semiconductor®
http://onsemi.com

Features

- Low ON-resistance
- 4.5V drive
- Halogen free compliance
- Large current
- Slim package
- Protection diode in

Specifications

Absolute Maximum Ratings at Ta=25°C

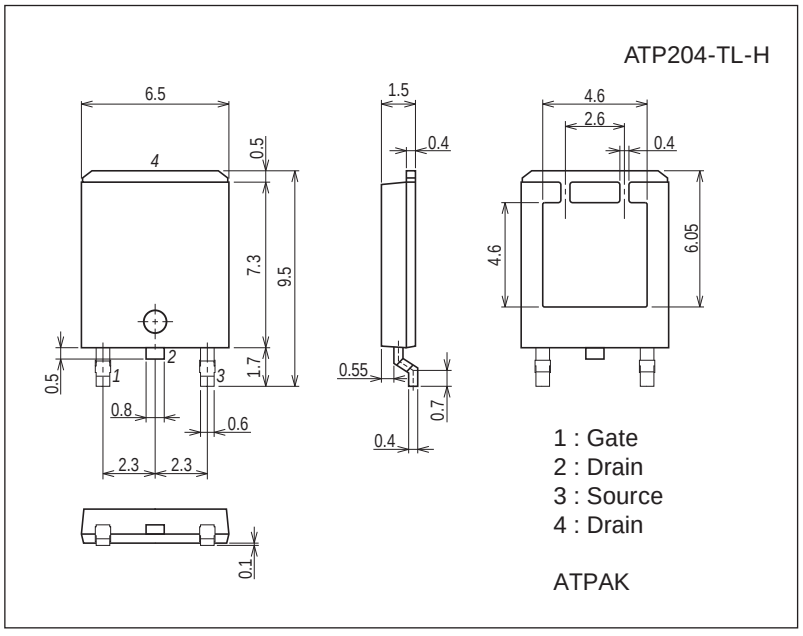
Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		30	V
Gate-to-Source Voltage	V_{GSS}		±20	V
Drain Current (DC)	I_D		100	A
Drain Current (PW≤10μs)	I_{DP}	PW≤10μs, duty cycle≤1%	300	A
Allowable Power Dissipation	P_D	Tc=25°C	60	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C
Avalanche Energy (Single Pulse) *1	E_{AS}		235	mJ
Avalanche Current *2	I_{AV}		50	A

Note :*1 V_{DD}=15V, L=100μH, I_{AV}=50A
*2 L≤100μH, Single pulse

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

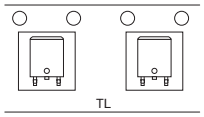
unit : mm (typ)
7057-001



Product & Package Information

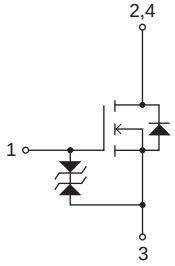
- Package : ATPAK
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

Packing Type: TL



Marking

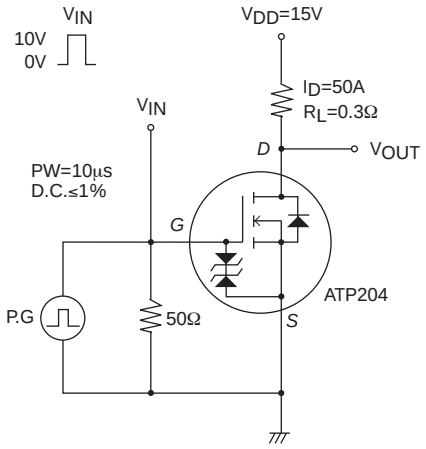
Electrical Connection



Electrical Characteristics at Ta=25°C

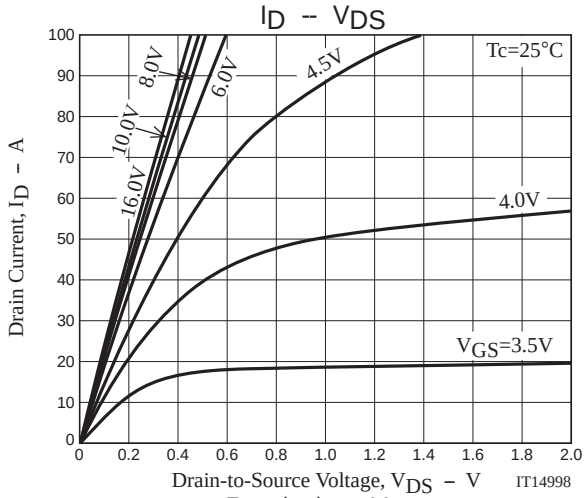
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0V	30			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V			1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0V			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=10V, I_D=1mA	1.2		2.6	V
Forward Transfer Admittance	| yfs |	V_{DS}=10V, I_D=50A		100		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=50A, V_{GS}=10V		4.3	5.6	mΩ
	R_{DS}(on)2	I_D=25A, V_{GS}=4.5V		6.5	9.1	mΩ
Input Capacitance	Ciss	V_{DS}=10V, f=1MHz		4600		pF
Output Capacitance	Coss			700		pF
Reverse Transfer Capacitance	Crss			390		pF
Turn-ON Delay Time	t_d(on)	See specified Test Circuit.		40		ns
Rise Time	t_r			690		ns
Turn-OFF Delay Time	t_d(off)			205		ns
Fall Time	t_f			110		ns
Total Gate Charge	Qg	V_{DS}=15V, V_{GS}=10V, I_D=100A		70		nC
Gate-to-Source Charge	Qgs			22		nC
Gate-to-Drain “Miller” Charge	Qgd			9.2		nC
Diode Forward Voltage	V_{SD}	I_S=100A, V_{GS}=0V		1.03	1.2	V

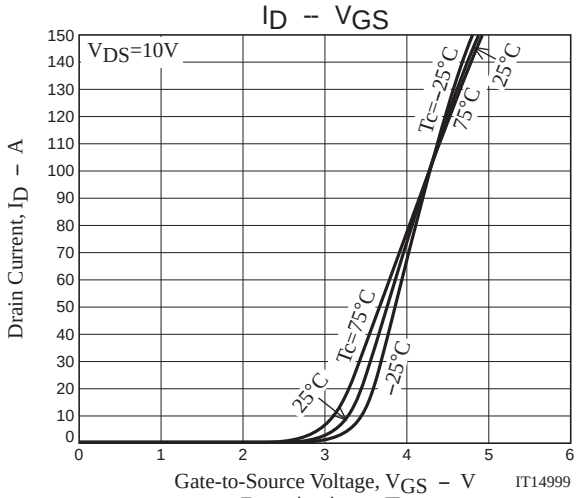
Switching Time Test Circuit

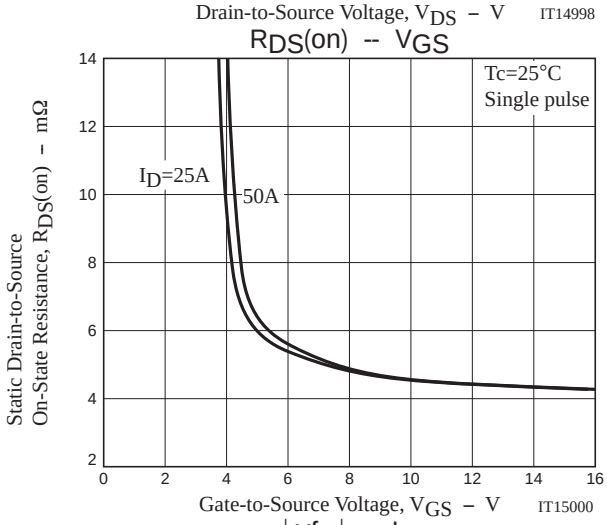


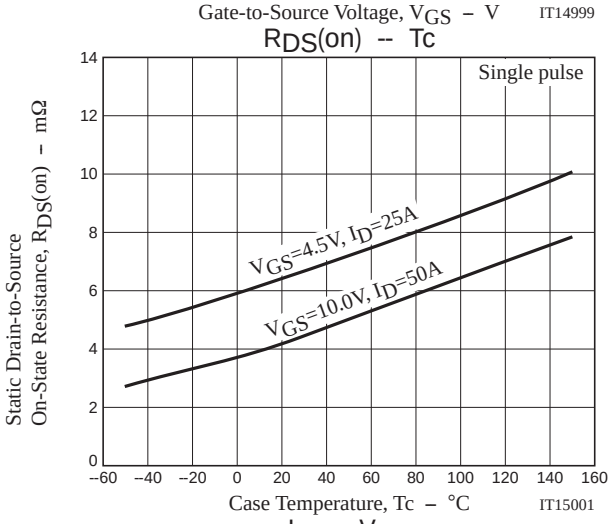
Ordering Information

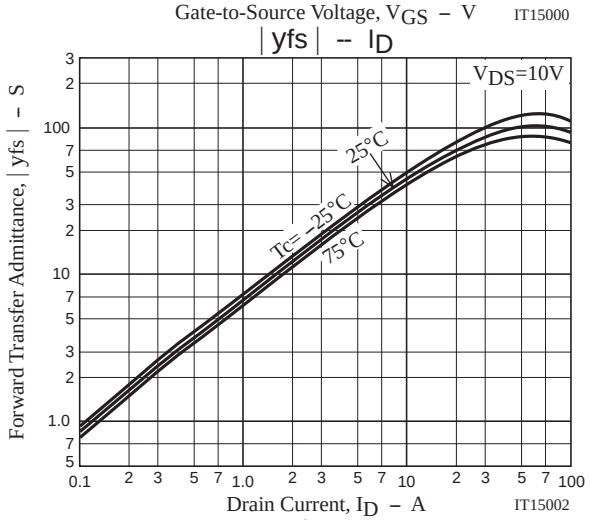
Device	Package	Shipping	memo
ATP204-TL-H	ATPAK	3,000pcs./reel	Pb Free and Halogen Free

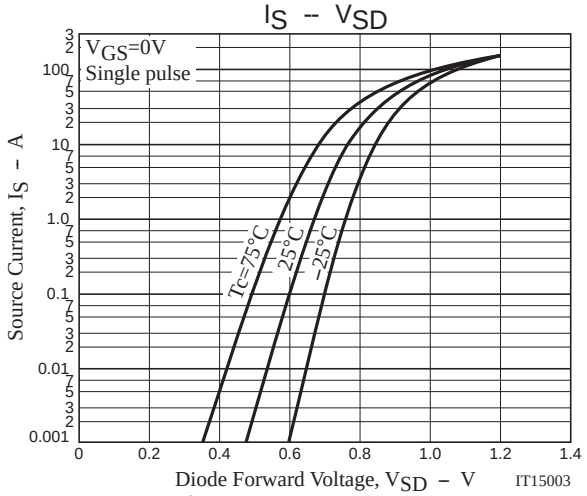

I_D -- V_{DS}
Tc=25°C
8.0V
6.0V
4.5V
10.0V
16.0V
4.0V
V_{GS}=3.5V
Drain Current, I_D – A
Drain-to-Source Voltage, V_{DS} – V
IT14998

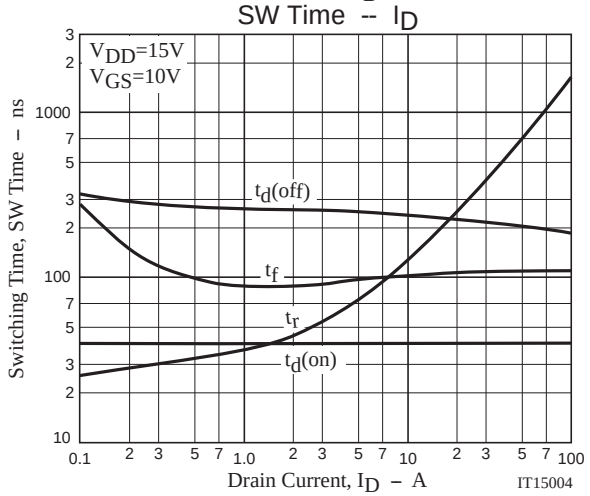

I_D -- V_{GS}
V_{DS}=10V
Tc=–25°C
75°C
25°C
Tc=75°C
25°C
–25°C
Drain Current, I_D – A
Gate-to-Source Voltage, V_{GS} – V
IT14999

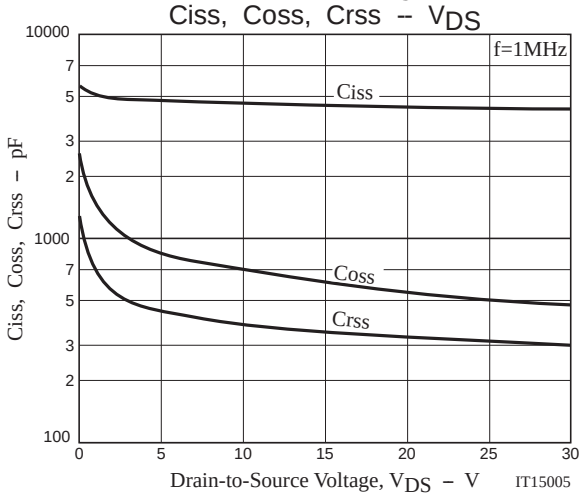

$R_{DS(on)}$ -- V_{GS}
Tc=25°C
Single pulse
I_D=25A
50A
Static Drain-to-Source On-State Resistance, $R_{DS(on)}$ – mΩ
Gate-to-Source Voltage, V_{GS} – V
IT15000

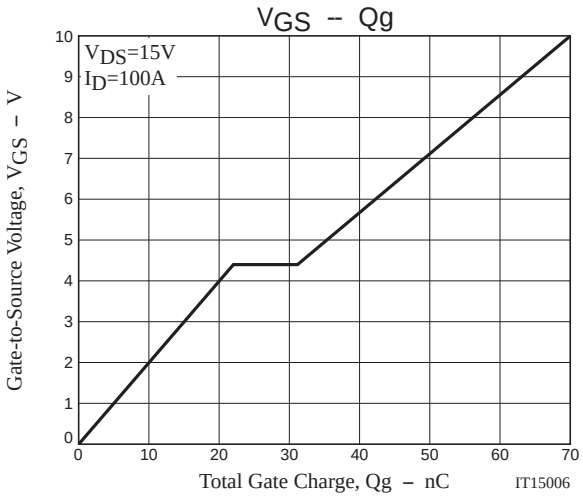

$R_{DS(on)}$ -- Tc
Single pulse
V_{GS}=4.5V, I_D=25A
V_{GS}=10.0V, I_D=50A
Static Drain-to-Source On-State Resistance, $R_{DS(on)}$ – mΩ
Case Temperature, Tc – °C
IT15001

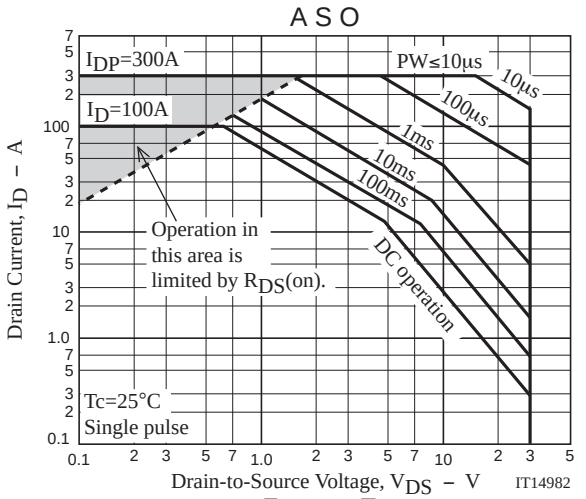

| yfs | -- I_D
V_{DS}=10V
25°C
Tc=–25°C
75°C
Forward Transfer Admittance, | yfs | – S
Drain Current, I_D – A
IT15002

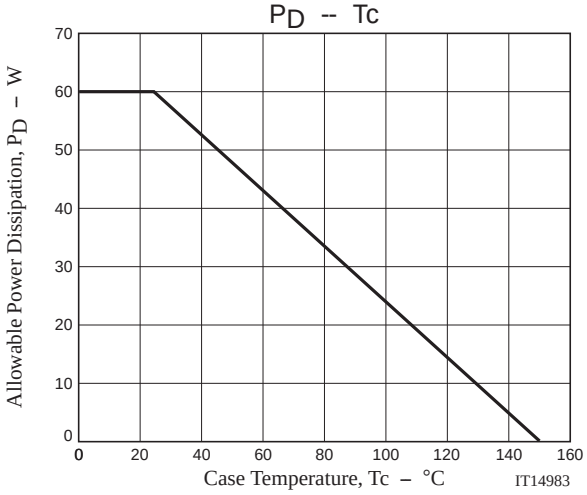

I_S -- V_{SD}
V_{GS}=0V
Single pulse
Tc=75°C
25°C
–25°C
Source Current, I_S – A
Diode Forward Voltage, V_{SD} – V
IT15003

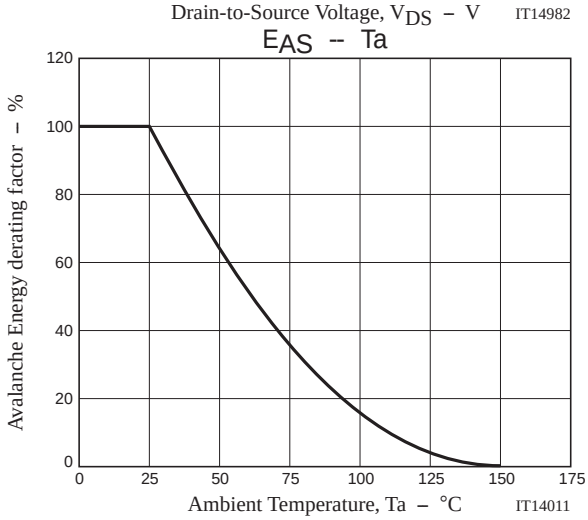

SW Time -- I_D
V_{DD}=15V
V_{GS}=10V
$t_{d(off)}$
t_f
t_r
$t_{d(on)}$
Switching Time, SW Time – ns
Drain Current, I_D – A
IT15004


Ciss, Coss, Crss -- V_{DS}
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, V_{DS} – V
IT15005


VGS – Qg
VDS=15V
ID=100A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT15006


A S O
IDP=300A
ID=100A
PW≤10μs
10μs
100μs
1ms
10ms
100ms
DC operation
Operation in this area is limited by RDS(on).
Tc=25°C
Single pulse
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT14982


PD -- Tc
Allowable Power Dissipation, PD – W
Case Temperature, Tc – °C
IT14983


EAS -- Ta
Avalanche Energy derating factor – %
Ambient Temperature, Ta – °C
IT14011

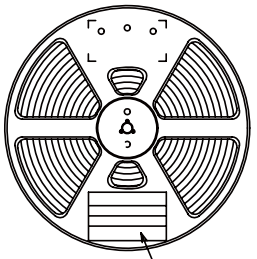
Taping Specification

ATP204-TL-H

1. Packing Format (TL)

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	INNER BOX SD-C-18	OUTER BOX SD-A-18
ATPAK	ATP	3,000	3,000	15,000	1 reels contained Dimensions:mm (external) 340×340×28	5 inner boxes contained Dimensions:mm (external) 355×355×165

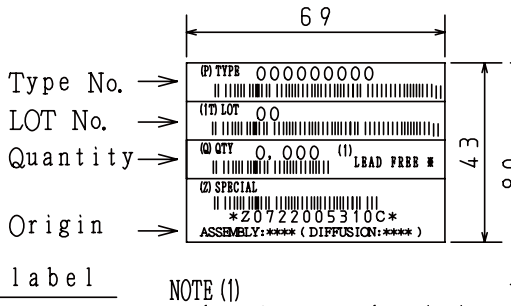
Packing method



Reel label

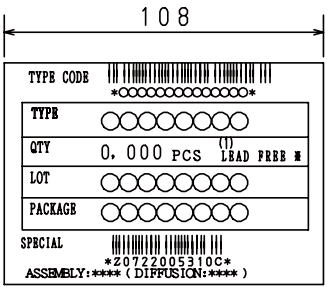
Reel label, Inner box label

(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



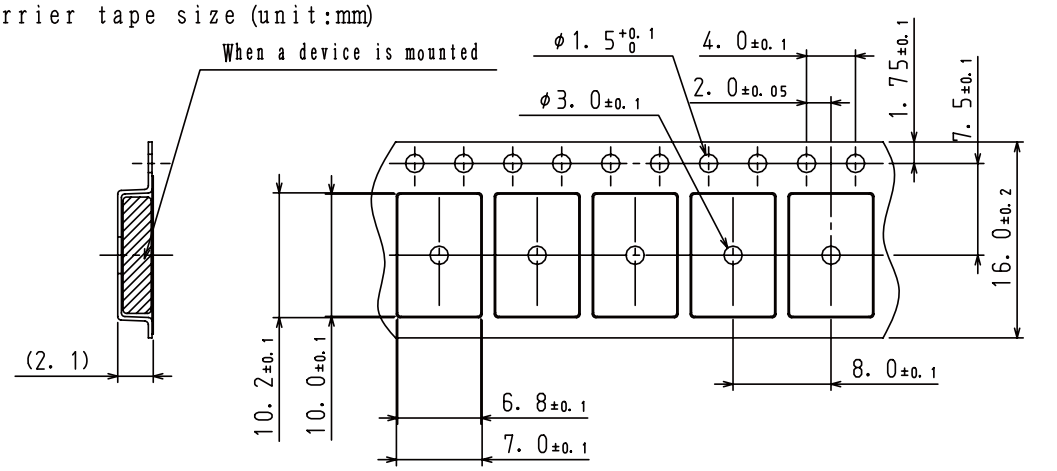
NOTE (1)

The LEAD FREE ※ description shows that the surface treatment of the terminal is lead free.

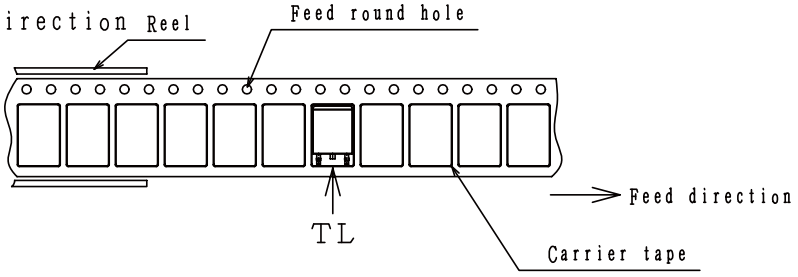
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



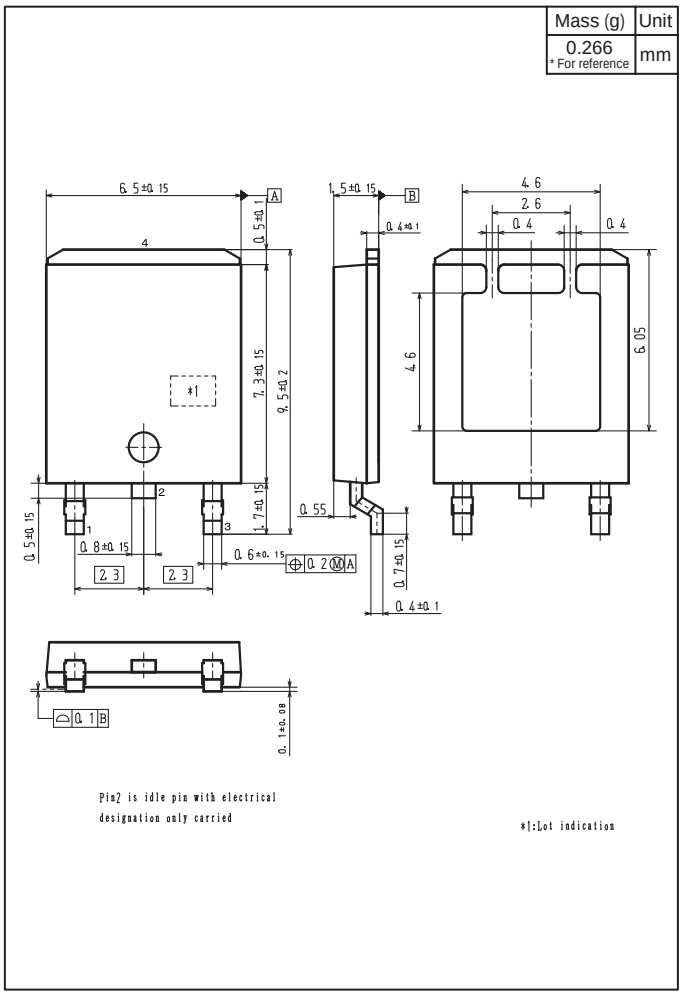
2-2. Device placement direction



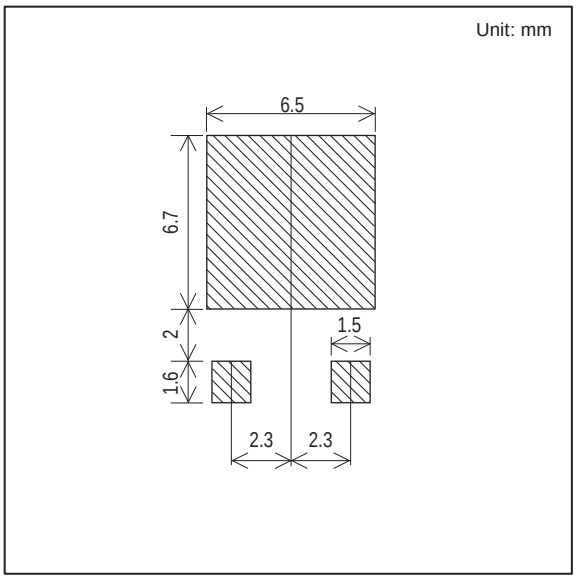
The one erectrode terminals on feed hole side····TL

Outline Drawing

ATP204-TL-H



Land Pattern Example



Note on usage : Since the ATP204 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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