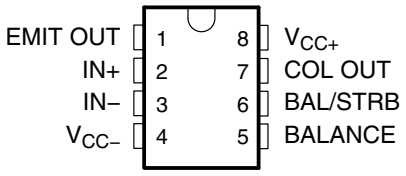
- **Low Power Drain . . . 900 μW Typical With 5-V Supply**
- **Operates From ±15 V or From a Single Supply as Low as 3 V**
- **Output Drive Capability of 25 mA**
- **Emitter Output Can Swing Below Negative Supply**
- **Response Time . . . 1.2 μs Typ**
- **Low Input Currents:**
  Offset Current . . . 2 nA Typ
  Bias Current . . . 15 nA Typ
- **Wide Common-Mode Input Range:**
  –14.5 V to 13.5 V Using ±15-V Supply
- **Offset Balancing and Strobe Capability**
- **Same Pinout as LM211, LM311**
- **Designed To Be Interchangeable With Industry-Standard LP311**

LP211 . . . D PACKAGE
LP311 . . . D, P, OR PS PACKAGE
(TOP VIEW)



description/ordering information

The LP211 and LP311 devices are low-power versions of the industry-standard LM211 and LM311 devices. They take advantage of stable, high-value, ion-implanted resistors to perform the same function as the LM311 series, with a 30:1 reduction in power consumption, but only a 6:1 slowdown in response time. They are well suited for battery-powered applications and all other applications where fast response times are not needed. They operate over a wide range of supply voltages, from ±18 V down to a single 3-V supply with less than 300-μA current drain, but are still capable of driving a 25-mA load. The LP211 and LP311 are quite easy to apply free of oscillation if ordinary precautions are taken to minimize stray coupling from the output to either input or to the trim pins. In addition, offset balancing is available to minimize input offset voltage. Strobe capability also is provided to turn off the output (regardless of the inputs) by pulling the strobe pin low.

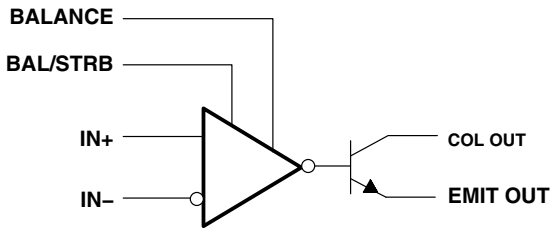
The LP211 is characterized for operation from –25°C to 85°C. The LP311 is characterized for operation from 0°C to 70°C.

ORDERING INFORMATION

T_A	V_{IO} max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–0°C to 70°C	7.5 mV	PDIP (P)	Tube of 50	LP311P	LP311P
		SOIC (D)	Tube of 75	LP311D	LP311
			Reel of 2500	LP311DR	
		SOP (PS)	Reel of 2000	LP311PSR	L311
–25°C to 85°C	7.5 mV	SOIC (D)	Tube of 75	LP211D	LP211
			Reel of 2500	LP211DR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC+} . . . . . 18 V
V_{CC-} . . . . . –18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±30 V
Input voltage, V_I (either input, see Notes 1 and 3) . . . . . ±15 V
Voltage from emitter output to V_{CC-} . . . . . 30 V
Voltage from collector output to V_{CC-} . . . . . 40 V
Voltage from collector output to emitter output . . . . . 40 V
Duration of output short circuit (see Note 4) . . . . . 40 V
Package thermal impedance, θ_{JA} (see Notes 5 and 6): D package . . . . . 97°C/W
P package . . . . . 85°C/W
PS package . . . . . 95°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential input voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage of ±15 V, whichever is less.
4. The output may be shorted to ground or to either power supply.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
($\|V_{CC\pm}\| \le 15$ V)	Input voltage	V_{CC-} + 0.5	V_{CC+} – 1.5	V
$V_{CC+} - V_{CC-}$	Supply voltage	3.5	30	V

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP†	MAX	UNIT
V_{ID}	Input offset voltage	RS < 100 kΩ,	See Note 7	25°C		2	7.5	mV
				Full range			10	
V_{OL}	Low-level output voltage	V_{ID} < –10 mV, See Note 8	I_{OL} = 25 mA,	25°C		0.4	1.5	V
		V_{CC} = 4.5 V, V_{ID} < –10 mV, See Note 8	V_{CC-} = 0, I_{OL} = 1.6 mA,	Full range		0.1	0.4	
I_{IO}	Input offset current	See Note 7		25°C		2	25	nA
				Full range			35	
I_{IB}	Input bias current			25°C		15	100	nA
				Full range			150	
	Low-level strobe current	$V_{(strobe)}$ = 0.3 V, See Note 9	V_{ID} < –10 mV,	25°C		100	300	μA
$I_{O(off)}$	Output off-state current	V_{ID} > 10 mV,	V_{CE} = 35 V	25°C		0.2	100	nA
A_{VD}	Large-signal differential-voltage amplification	R_L = 5 kΩ		25°C	40	100		V/mV
I_{CC+}	Supply current from V_{CC+}	V_{ID} = –50 mV,	R_L = ∞	Full range		150	300	μA
I_{CC-}	Supply current from V_{CC-}	V_{ID} = 50 mV,	R_L = ∞	Full range		– 80	– 180	μA

† All typical values are at $V_{CC\pm}$ = ±15 V, T_A = 25°C.

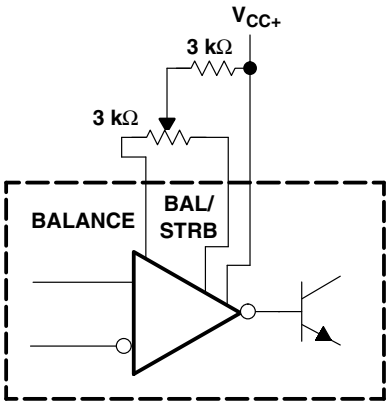
NOTES: 7. The offset voltages and offset currents given are the maximum values required to drive the output within 1 V of either supply with a 1-mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.
8. Voltages are with respect to EMIT OUT and V_{CC-} tied together.
9. The strobe should not be shorted to ground; it should be current driven at 100 μA to 300 μA.

switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	UNIT
Response time	See Note 10	1.2	μs

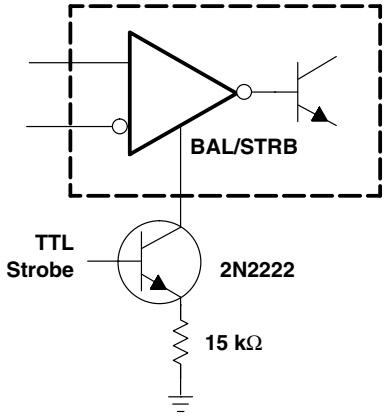
NOTE 10: The response time is specified for a 100-mV input step with 5-mV overdrive.

TYPICAL APPLICATION CIRCUIT



NOTE: If offset balancing is not used, the BALANCE and BAL/STRB pins should be shorted together.

Figure 1. Offset Balancing



NOTE: Do not connect strobe pin directly to ground, because the output is turned off whenever current is pulled from the strobe pin.

Figure 2. Strobing

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP211D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LP211
LP211D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LP211
LP211DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LP211
LP211DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LP211
LP211DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-25 to 85	
LP311D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP311
LP311D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP311
LP311DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP311
LP311DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP311
LP311P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LP311P
LP311P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LP311P
LP311PE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

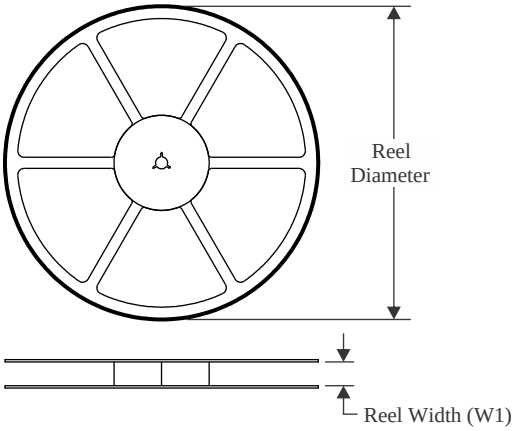
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

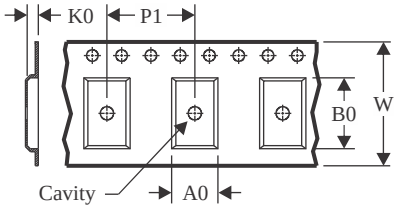
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

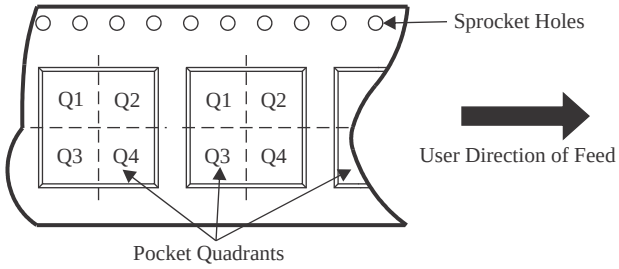


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

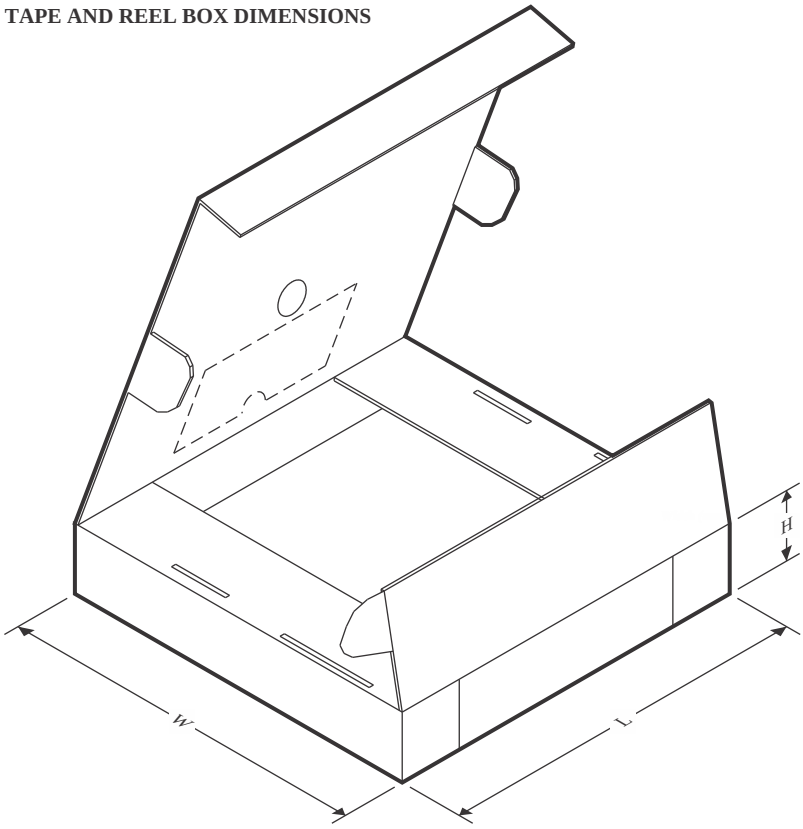
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP211DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LP311DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

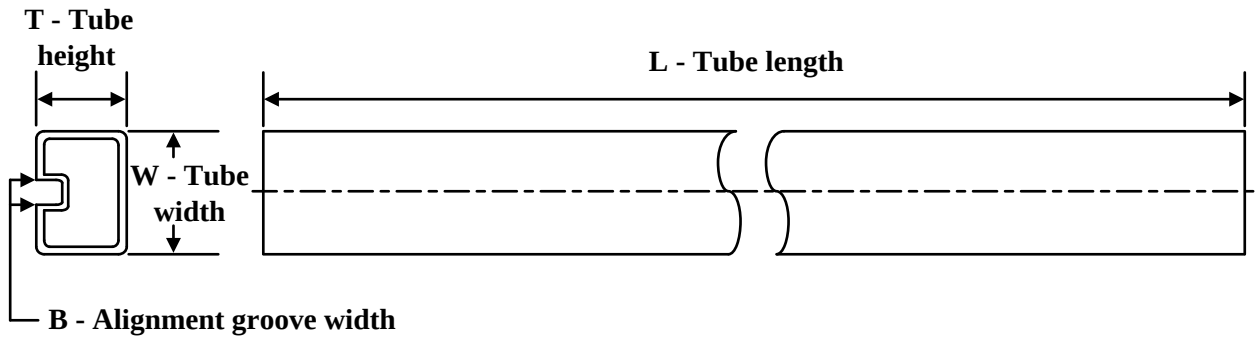
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

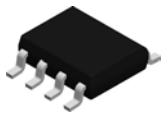
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP211DR	SOIC	D	8	2500	353.0	353.0	32.0
LP311DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP211D	D	SOIC	8	75	507	8	3940	4.32
LP211D.A	D	SOIC	8	75	507	8	3940	4.32
LP311D	D	SOIC	8	75	507	8	3940	4.32
LP311D.A	D	SOIC	8	75	507	8	3940	4.32
LP311P	P	PDIP	8	50	506	13.97	11230	4.32
LP311P.A	P	PDIP	8	50	506	13.97	11230	4.32

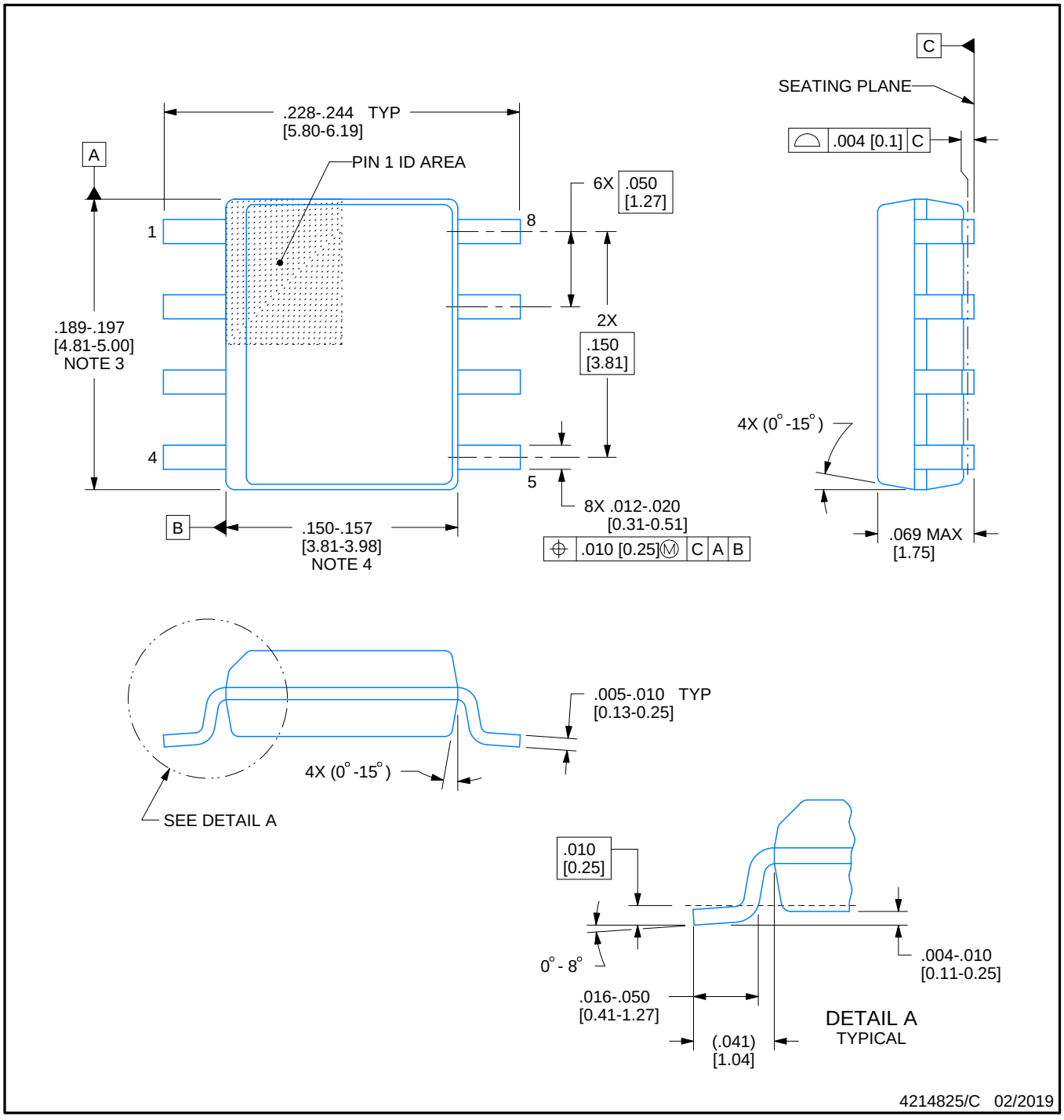


PACKAGE OUTLINE

D0008A

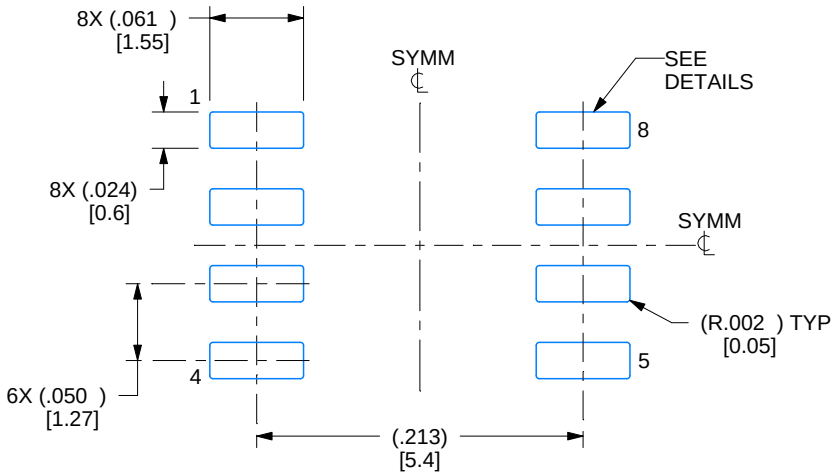
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

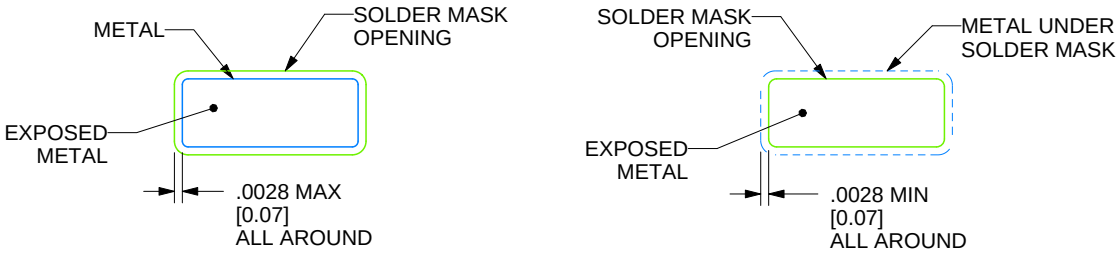


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

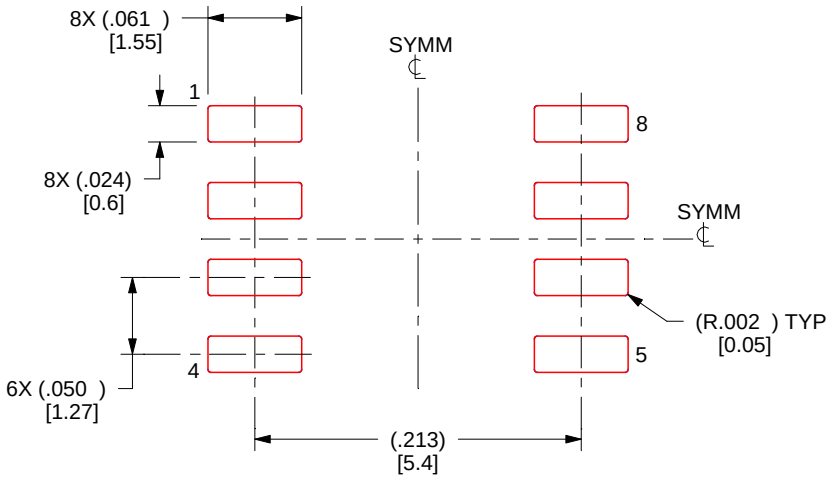
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



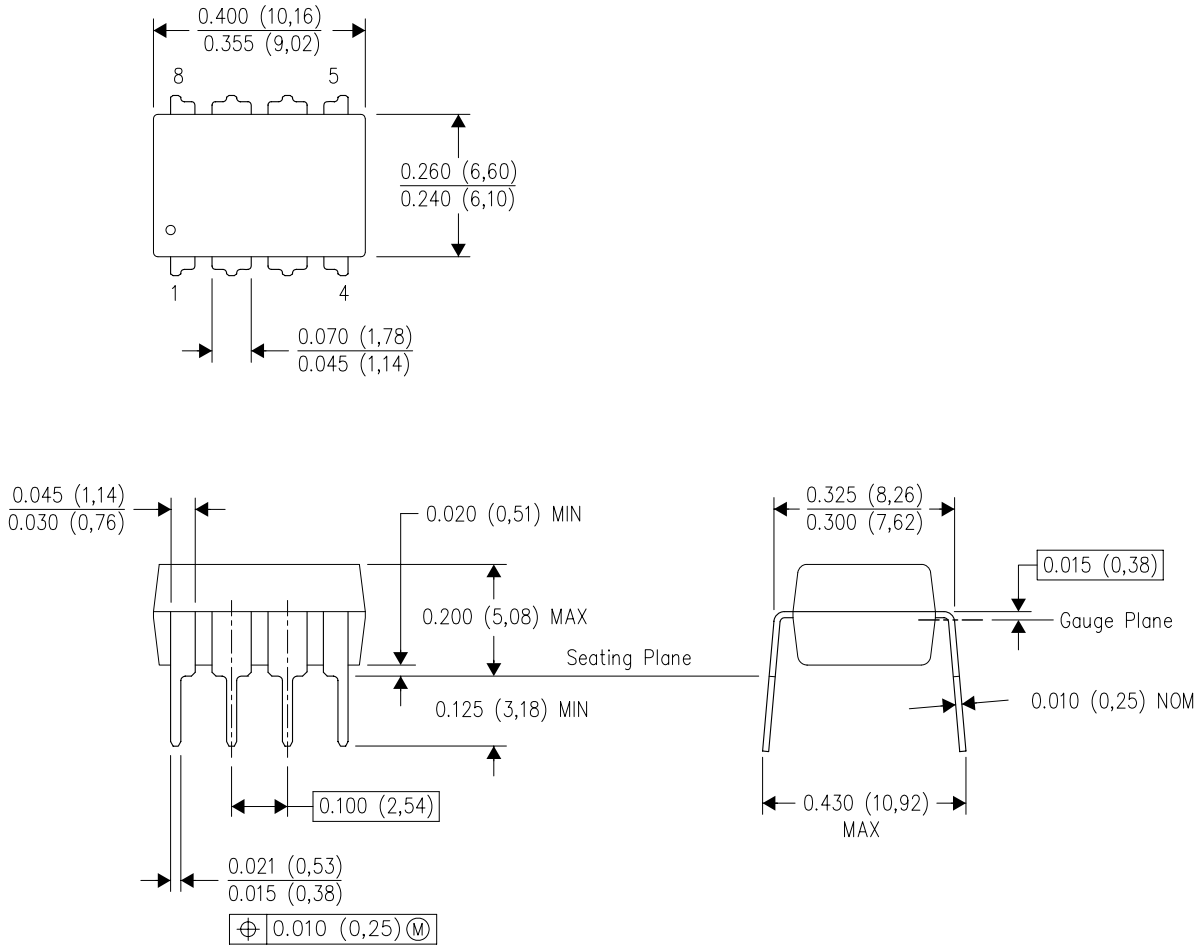
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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