

74LVC163

Presettable synchronous 4-bit binary counter; synchronous reset

Rev. 9 — 12 February 2024

Product data sheet

1. General description

The 74LVC163 is a synchronous presettable binary counter which features an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (pin CP). The outputs (pins Q0 to Q3) of the counters may be preset to a HIGH-level or LOW-level. A LOW-level at the parallel enable input (pin $\overline{PE}$) disables the counting action and causes the data at the data inputs (pins D0 to D3) to be loaded into the counter on the positive-going edge of the clock (provided that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (pin CEP and CET). A LOW-level at the master reset input (pin $\overline{MR}$) sets all four outputs of the flip-flops (pins Q0 to Q3) to LOW-level after the next positive-going transition on the clock input (pin CP) (provided that the set-up and hold time requirements for PE are met). This action occurs regardless of the levels at input pins $\overline{PE}$, CET and CEP. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (pin CEP and CET) must be HIGH in count. The CET input is fed forward to enable the terminal count output (pin TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH-level output of Q0. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by t_{PHL} (propagation delay CP to TC) and t_{su} (set-up time CEP to CP) according to the formula: $f_{max} = \frac{1}{t_{PHL(max)} + t_{su}}$.

2. Features and benefits

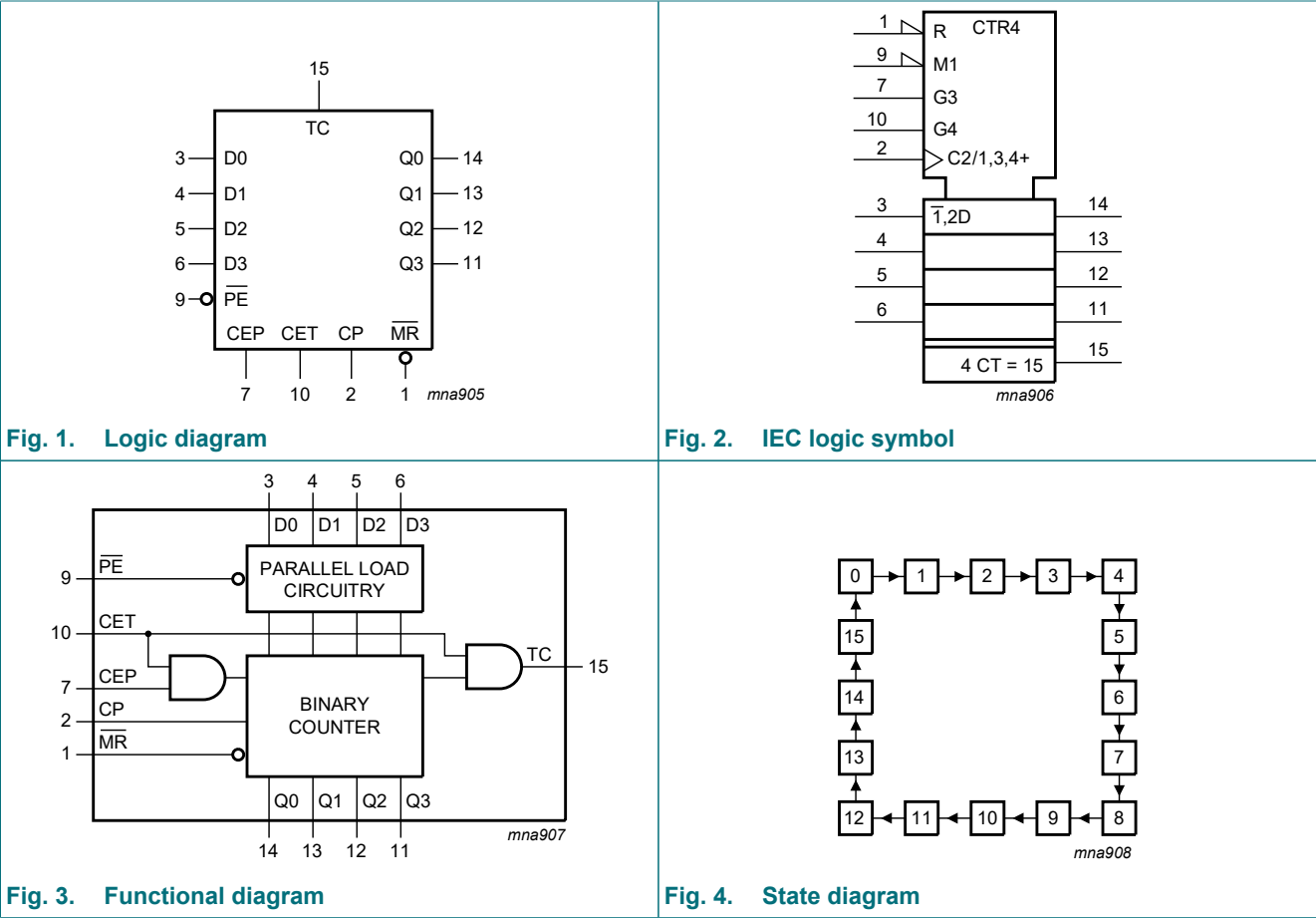
- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Synchronous reset
- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to 125 °C

3. Ordering information

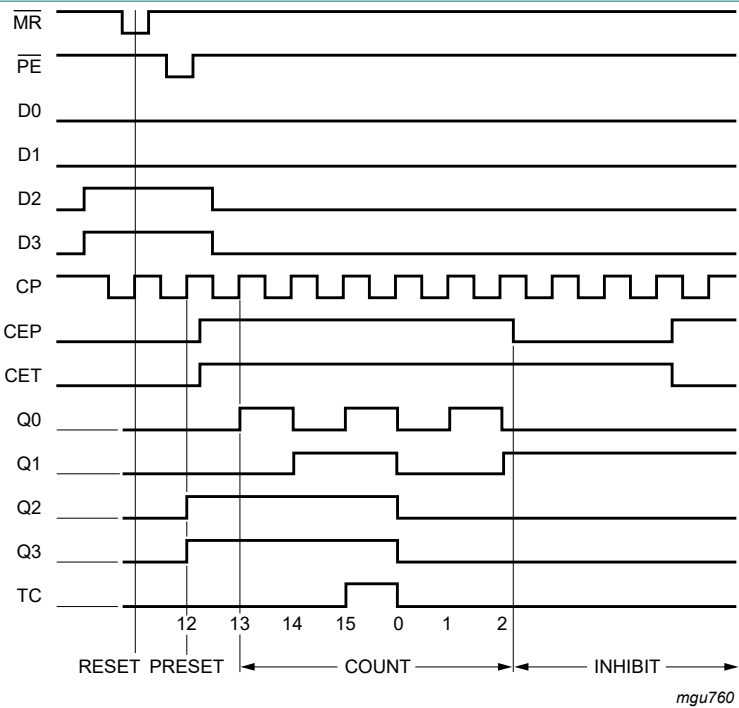
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC163D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC163PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC163BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram



Presettable synchronous 4-bit binary counter; synchronous reset



Typical timing sequence: Reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

Fig. 5. Timing sequence

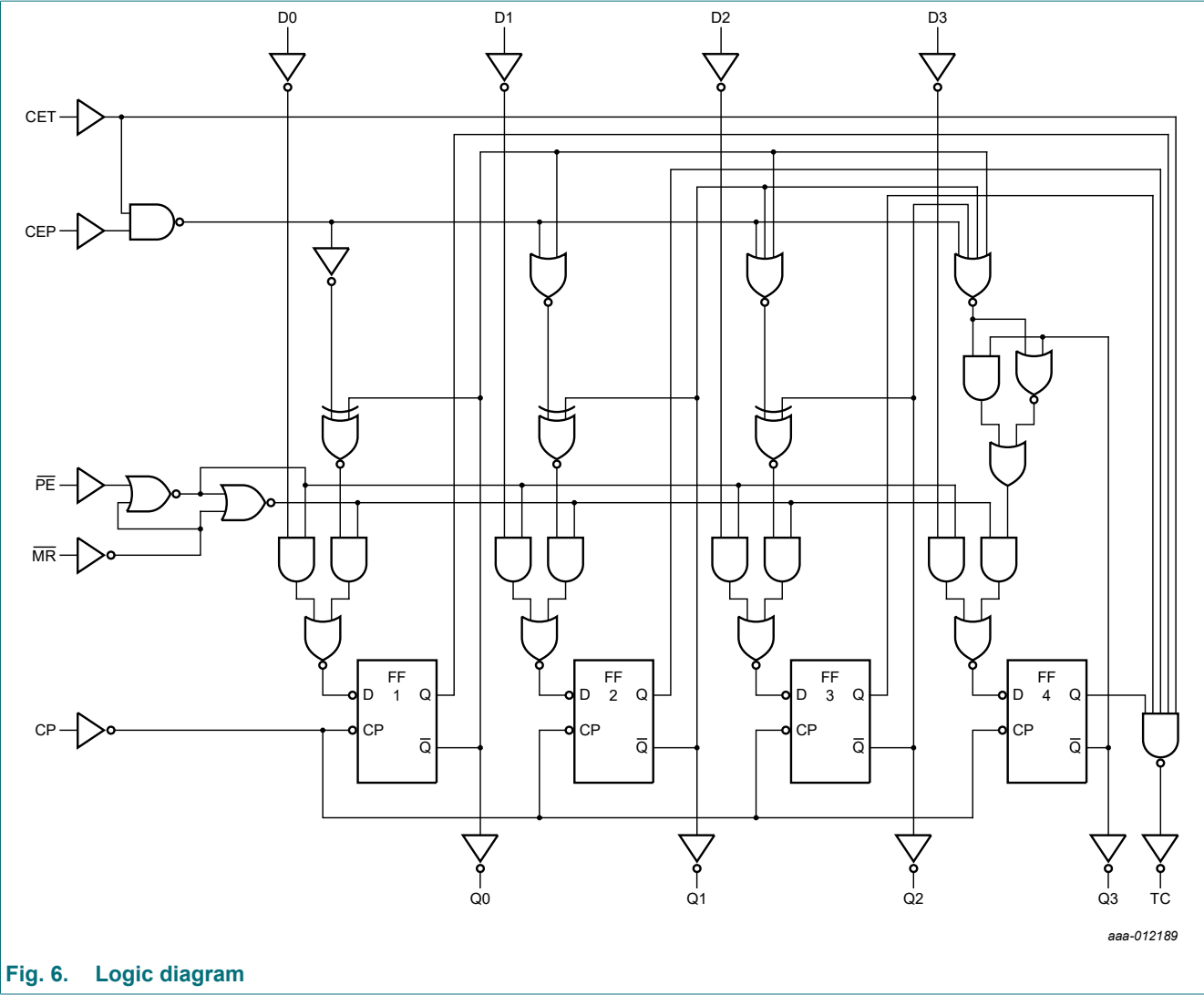
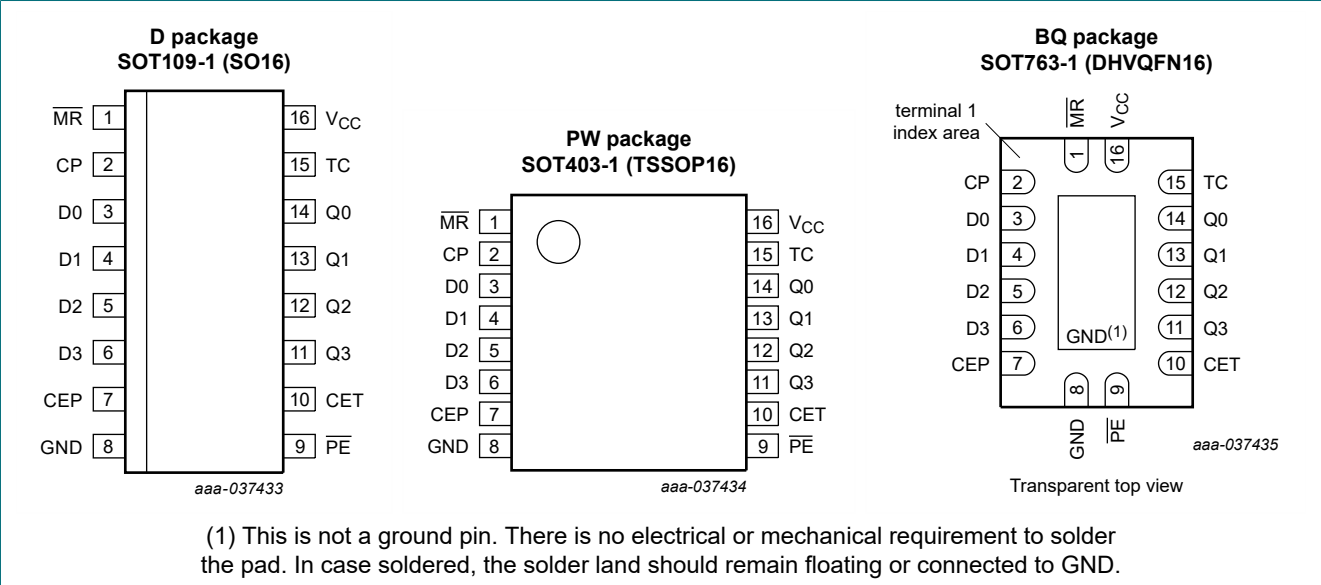


Fig. 6. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
MR	1	synchronous master reset (active LOW)
CP	2	clock input (LOW-to-HIGH, edge-triggered)
D0, D1, D2, D3	3, 4, 5, 6	data input
CEP	7	count enable input
GND	8	ground (0)
PE	9	parallel enable input (active LOW)
CET	10	count enable carry input
Q0, Q1, Q2, Q3	14, 13, 12, 11	flip-flop output
TC	15	terminal count output
V _{CC}	16	supply voltage

6. Functional description

Table 3. Functional table
* = the TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH);
H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care; ↑ = LOW-to-HIGH clock transition.

Operating modes	Input						Output	
	MR	CP	CEP	CET	PE	Dn	Qn	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
Count	h	↑	h	h	h	X	count	*
Hold (do nothing)	h	X	l	X	h	X	q _n	*
	h	X	X	l	h	X	q _n	L

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage	[1]	-0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	[2]	-0.5	V _{CC} + 0.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 x V _{CC}	-	-	0.65 x V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 x V _{CC}	-	0.35 x V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	μA

Presetable synchronous 4-bit binary counter; synchronous reset

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 2.7\text{ V to }3.6\text{ V}$; $V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$	-	5	500	-	5000	μA
C_I	input capacitance	$V_{CC} = 0\text{ V to }3.6\text{ V}$; $V_I = \text{GND to }V_{CC}$	-	5.0	-	-	-	pF

[1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ (unless stated otherwise) and $T_{amb} = 25\text{ °C}$.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 12.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	CP to Qn; see Fig. 7 [2]						
		$V_{CC} = 1.2\text{ V}$	-	18	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	7.4	14.5	1.5	16.7	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.6	4.2	8.1	2.6	9.4	ns
		$V_{CC} = 2.7\text{ V}$	1.5	4.0	7.3	1.5	9.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	3.8	7.3	1.5	9.5	ns
		CET to TC; see Fig. 7 [2]						
		$V_{CC} = 1.2\text{ V}$	-	23	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.9	8.5	15.7	1.9	18.1	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	3.0	4.8	8.8	3.0	10.2	ns
		$V_{CC} = 2.7\text{ V}$	1.5	4.6	8.1	1.5	10.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	4.3	7.9	1.5	10.0	ns
		CET to TC; see Fig. 8 [2]						
		$V_{CC} = 1.2\text{ V}$	-	16	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	6.3	12.7	1.5	14.6	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.3	3.6	7.1	2.3	8.2	ns
t_W	pulse width	CP HIGH or LOW; see Fig. 7						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	6.0	-	-	6.0	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	5.0	-	-	5.0	-	ns
		$V_{CC} = 2.7\text{ V}$	5.0	-	-	5.0	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	4.0	1.2	-	4.0	-	ns

Presettable synchronous 4-bit binary counter; synchronous reset

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{su}	set-up time	Dn to CP; see Fig. 10						
		V _{CC} = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V _{CC} = 2.7 V	3.0	-	-	3.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	2.5	1.0	-	2.5	-	ns
		MR, PE to CP; see Fig. 9 and Fig. 10						
		V _{CC} = 1.65 V to 1.95 V	4.5	-	-	4.5	-	ns
		V _{CC} = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V _{CC} = 2.7 V	3.5	-	-	3.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	3.0	1.2	-	3.0	-	ns
		CEP, CET to CP; see Fig. 11						
		V _{CC} = 1.65 V to 1.95 V	8.5	-	-	8.5	-	ns
		V _{CC} = 2.3 V to 2.7 V	6.5	-	-	6.5	-	ns
		V _{CC} = 2.7 V	5.5	-	-	5.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	5.0	2.1	-	5.0	-	ns
t _h	hold time	Dn, $\overline{\text{PE}}$, CEP, CET to CP; see Fig. 10 and Fig. 11						
		V _{CC} = 1.65 V to 1.95 V	2.0	-	-	2.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	2.0	-	-	2.0	-	ns
		V _{CC} = 2.7 V	0.0	-	-	0.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	0.0	-	0.5	-	ns
f _{max}	maximum frequency	see Fig. 7						
		V _{CC} = 1.65 V to 1.95 V	100	-	-	80	-	ns
		V _{CC} = 2.3 V to 2.7 V	125	-	-	100	-	ns
		V _{CC} = 2.7 V	150	-	-	120	-	MHz
		V _{CC} = 3.0 V to 3.6 V	150	200	-	120	-	MHz
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V [3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation capacitance	per input; V _I = GND to V _{CC} [4]						
		V _{CC} = 1.65 V to 1.95 V	-	9.8	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	13.4	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	16.6	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

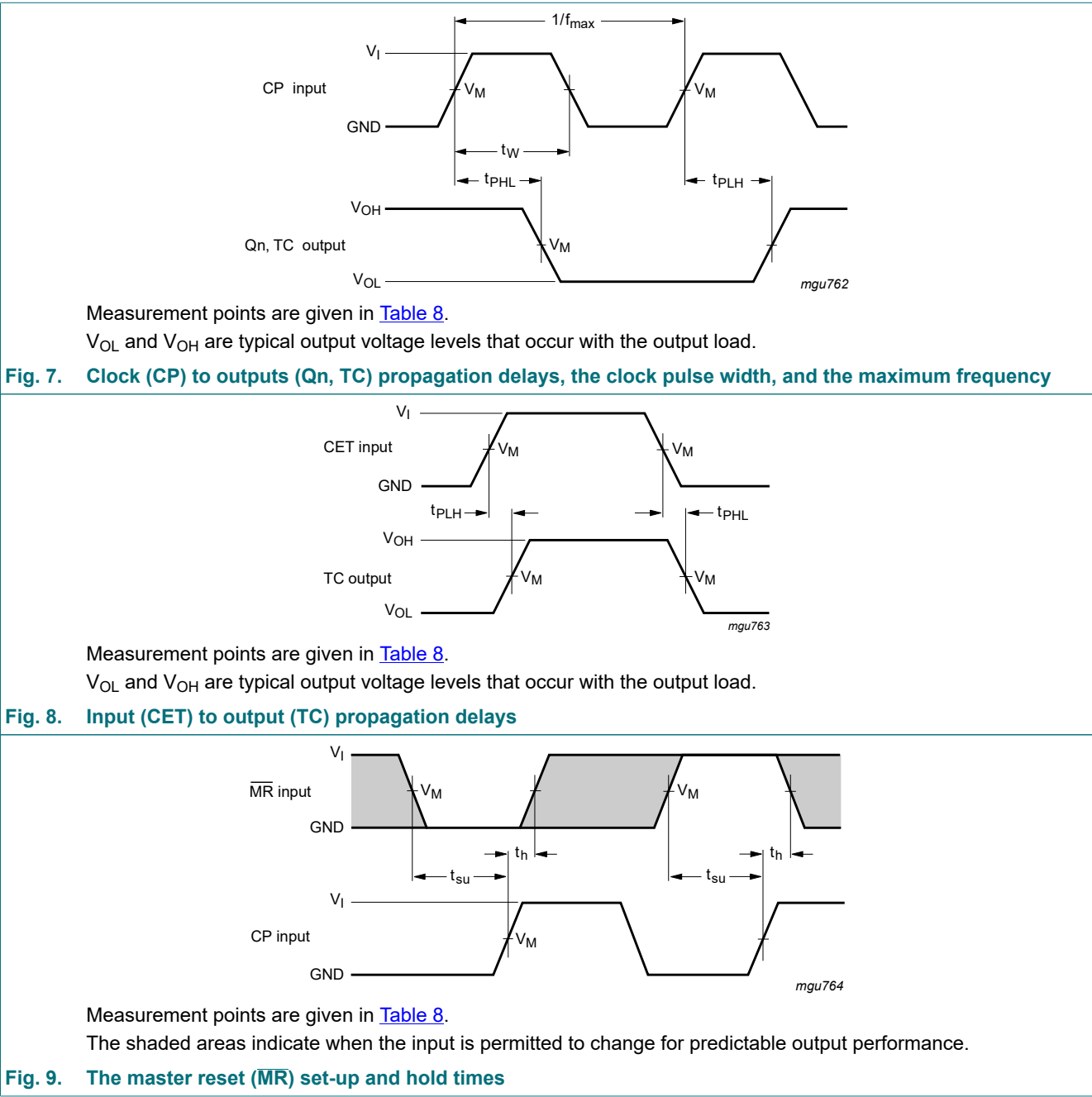
C_L = output load capacitance in pF

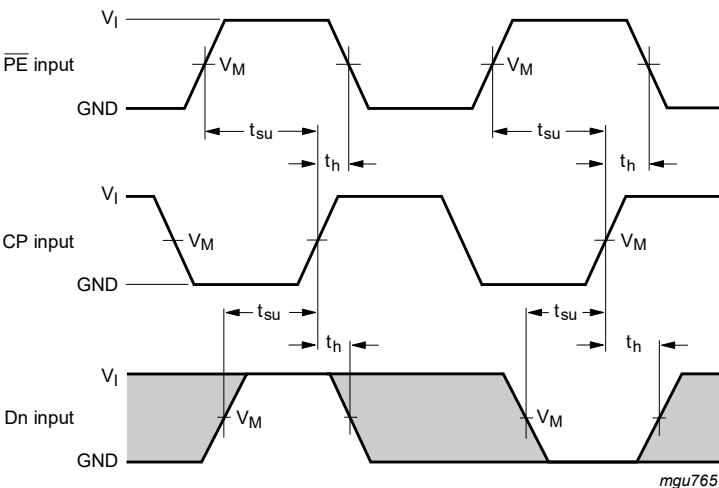
V_{CC} = supply voltage in V

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

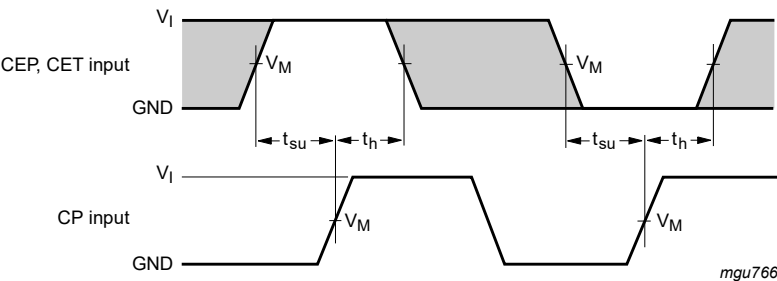
10.1. Waveforms and test circuit





Measurement points are given in [Table 8](#).
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 10. Set-up and hold times for the input (Dn) and parallel enable input (PE)

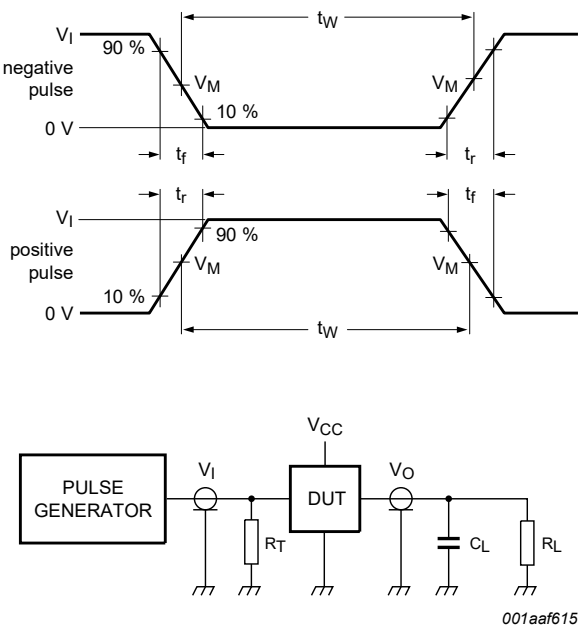


Measurement points are given in [Table 8](#).
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 11. CEP and CET set-up and hold times

Table 8. Measurement points

Supply voltage	Input		Output
V _{CC}	V _I	V _M	V _M
1.2 V	V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}
1.65 V to 1.95 V	V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}
2.3 V to 2.7 V	V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}
2.7 V	2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V



Test data is given in [Table 9](#).
Definitions for test circuit:
 R_L = Load resistance;
 C_L = Load capacitance including jig and probe capacitance;
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 12. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

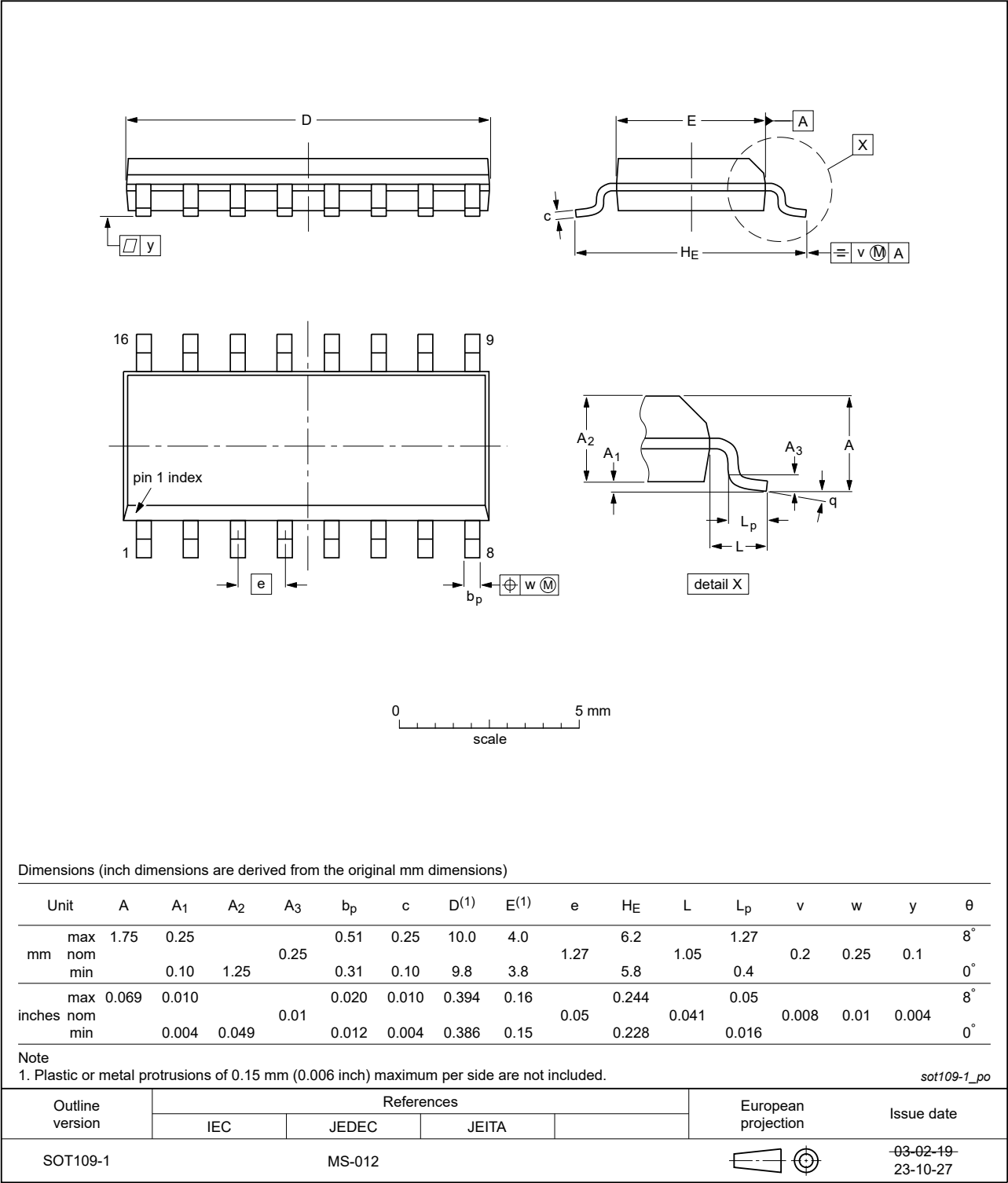


Fig. 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

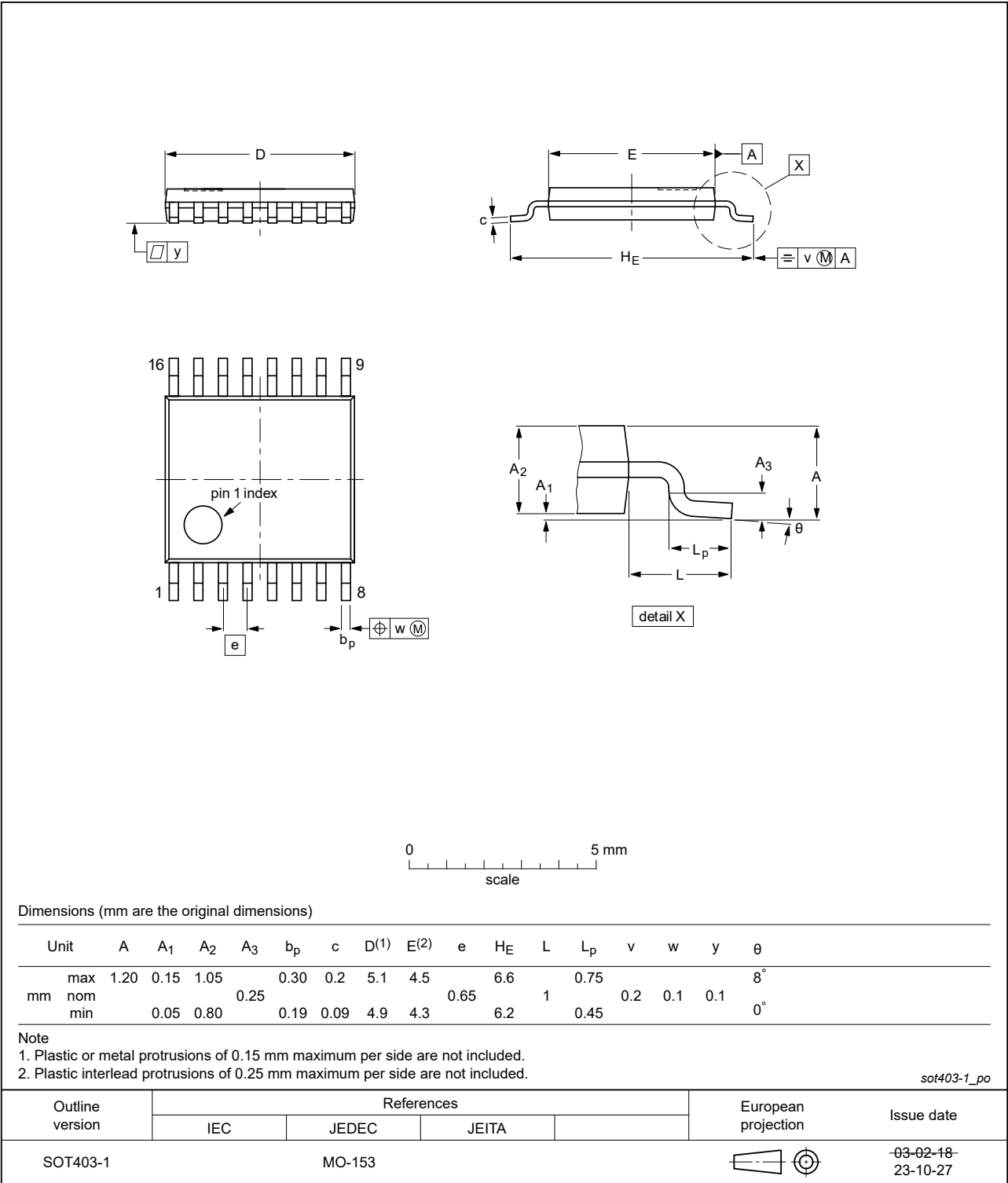


Fig. 14. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

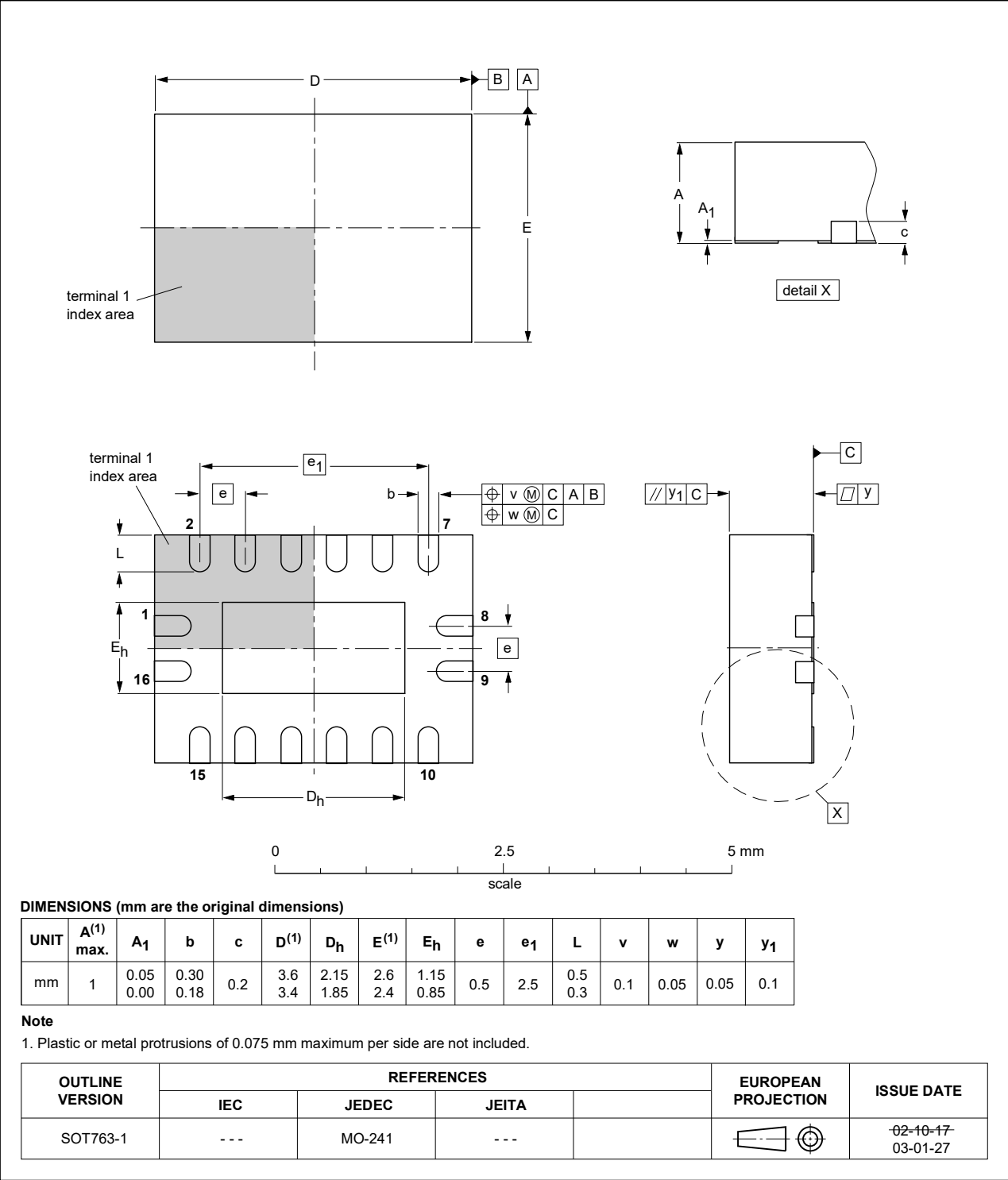


Fig. 15. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC163 v.9	20240212	Product data sheet	-	74LVC163 v.8
Modifications:	Fig. 13, Fig. 14: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74LVC163 v.8	20230823	Product data sheet	-	74LVC163 v.7
Modifications:	Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVC163 v.7	20210419	Product data sheet	-	74LVC163 v.6
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Type number 74LVC163DB (SOT338-1/SSOP16) removed. Section 7: Derating values for P_{tot} total power dissipation have been updated.			
74LVC163 v.6	20121120	Product data sheet	-	74LVC163 v.5
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. Table 4, Table 5, Table 6, Table 7, Table 8 and Table 9: values added for lower voltage ranges.			
74LVC163 v.5	20040505	Product specification	-	74LVC163 v.4
74LVC163 v.4	20030602	Product specification	-	74LVC163 v.3
74LVC163 v.3	20030509	Product specification	-	74LVC163 v.2
74LVC163 v.2	19980520	Product specification	-	74LVC163 v.1
74LVC163 v.1	19960823	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

Definitions

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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Ordering information.....2

4. Functional diagram.....2

5. Pinning information.....5

5.1. Pinning.....5

5.2. Pin description.....5

6. Functional description..... 6

7. Limiting values..... 6

8. Recommended operating conditions.....7

9. Static characteristics.....7

10. Dynamic characteristics..... 8

10.1. Waveforms and test circuit..... 10

11. Package outline..... 13

12. Abbreviations..... 16

13. Revision history.....16

14. Legal information.....17

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