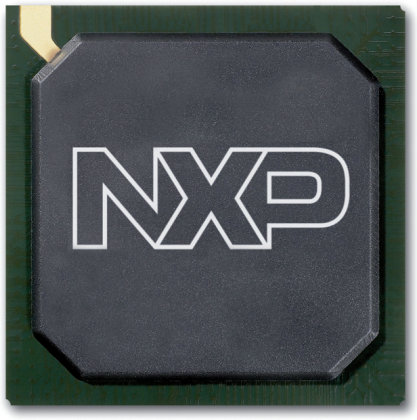


NXP MPEG-2 SD decoder with integrated QPSK demodulator CX24152/5

Highly integrated, cost efficient MPEG-2 SD decoder with integrated QPSK demodulator

NXP's MPEG-2 SD decoder with integrated QPSK demodulator features all the major subsystems required to implement the core system and decoder electronics of a DBS interactive TV STB.

Key features

- MPEG-2/DVB/DIRECTV® broadcast service decoder for worldwide markets
- Single IC DBS STB solution with integrated QPSK demod/FEC and NTSC Ch 3/4 RF modulator
- High-performance 32-bit 220 MIPS ARM920 CPU with 16KB I & D caches
- Advanced security features for DBS broadcasters
- High-performance 2D graphics rendering acceleration
- Multiplane video/graphics compositing and display engine
- High-performance 16 or 32-bit unified memory controller architecture

This includes an MPEG-2 A/V decoder (Dolby Digital audio is optional), transport processor, a 32-bit RISC CPU, a 2D graphics accelerator, TV encoder, QPSK demodulator, channel 3/4 RF modulator, a video/graphics display compositing controller and a set of peripheral I/O ports for set-top box front and back panel connectors. For a complete system hardware design, the only additional components required are a tuner, modem codec, audio DAC, SDRAM and flash memory ICs. This high level of integration delivers the low-cost system bill-of-materials sought after by mainstream digital DBS multichannel TV operators.

NXP founded by Philips

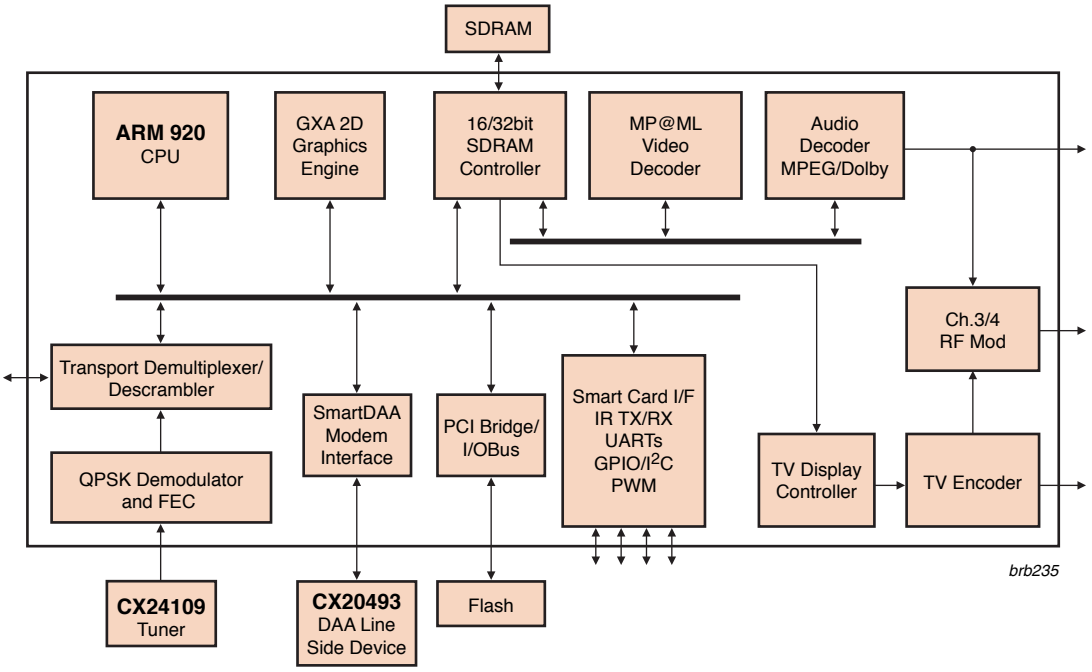
An advanced interactive set-top receiver will include sophisticated middleware to run downloadable applications using a high-speed return channel. Example applications include Advanced EPGs, online games, shopping, and interactive polling. The ARM920 CPU in the CX24152/5 offers up to 224 Dhrystone 2.1 MIPS at a 200MHz clock speed. This CPU platform represents a major advance in capability for the low cost STB category and will enable complex, MIPS hungry, feature rich middleware platforms such as MHP to be adopted by broadcasters for low cost STBs. The advanced CPU platform delivers performance that can be deployed by STB manufacturers in a variety of ways including improved interactive application loading and EPG scrolling performance, hardware feature differentiation via multimedia host signal processing and scalability to Linux based software platforms via MMU hardware support. Return channel can be supported by an interface to a host-controlled V.92 modem or PCI interface to DSL, Ethernet or wireless broadband modem.

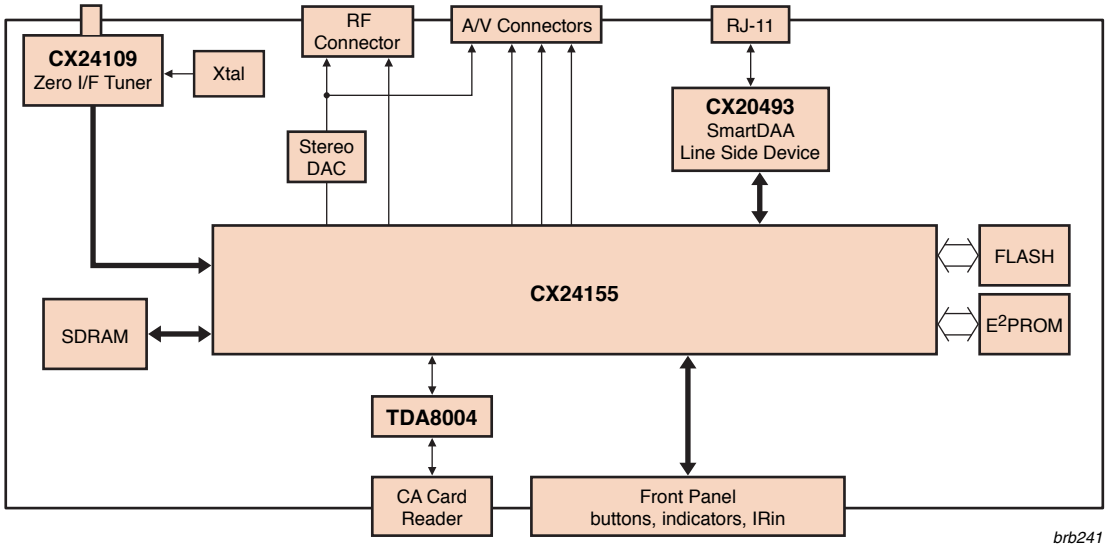
Advanced security for DBS broadcasters

The CX24152/5 incorporates an innovative set of security technologies that greatly enhances the ability of broadcasters to protect their service against piracy. Using an advanced on-chip one-time-programmable (OTP) memory technology, NXP offers broadcasters the ability to personalize individual STBs via the system IC with unique serial numbers and encryption keys. This allows the broadcaster to secure transactions between the STB smart card and the broadcaster service decoder. The CX24152/5 also includes embedded cryptographic technology to allow secure authentication of the STB system software that is loaded into the flash memory.

Full-featured development platform

The CX24152/5 IC family is integrated into a fully engineered interactive TV STB reference development system that implements third-party interactive middleware/RTOS platforms and provides complete STB functionality. The hardware platform comes equipped with fully integrated OpenTV, Alticast, Nucleus+, pSOS and VxWorks runtime libraries and driver software components. A mature and robust hardware abstraction layer is assured by re-use of core driver libraries developed on early generation ICs.
The development platform set-top box hardware is designed with both two and four layer PCB configurations and a variety of PSTN modem options. A choice of two robust tool chain development environments are supported for code developers including the ADS 1.2 from ARM, Inc. and Tornado 2.2 from WindRiver Systems, Inc. NXP offers a complete development code solution that has been tightly integrated with both third party tool chain environments.


SDRAM
ARM 920
CPU
GXA 2D
Graphics
Engine
16/32bit
SDRAM
Controller
MP@ML
Video
Decoder
Audio
Decoder
MPEG/Dolby
Ch.3/4
RF Mod
Transport Demultiplexer/
Descrambler
SmartDAA
Modem
Interface
PCI Bridge/
I/OBus
Smart Card I/F
IR TX/RX
UARTs
GPIO/I2C
PWM
TV Display
Controller
TV Encoder
QPSK Demodulator
and FEC
CX24109
Tuner
CX20493
DAA Line
Side Device
Flash
brb235


CX24109
Zero I/F Tuner
Xtal
RF
Connector
A/V Connectors
RJ-11
CX20493
SmartDAA
Line Side Device
Stereo
DAC
CX24155
FLASH
E2PROM
SDRAM
TDA8004
CA Card
Reader
Front Panel
buttons, indicators, IRin
brb241

CX24152/5 part number & feature selection guide

The CX24152/5 IC family includes two primary part numbers defined by different functionality combinations.

Table 1

"CX" Part #	Demod	DACs	RF Mod	Still Plane	DRAM	DVB-CI	PCI note 1
CX24152	yes	6	no	yes	16/32-bit	yes	yes
CX24155	yes	6	yes	yes	16/32-bit	yes	yes

License based features and CPU speed grade configurations are designated using a part number suffix or dash number.

CX24152-mn CX24155-mn	"-1n"	"-2n"	"-3n"	"-4n"	"-5n"	"-6n"	"-7n"	"-8n"	"-9n"	"-0n"
Macrovision		✓		✓	reserved	reserved		✓		✓
Dolby Digital			✓	✓					✓	✓
200 MHz CPU	✓	✓	✓	✓						
160 MHz CPU							✓	✓	✓	✓

m = License based feature and/or PU speed designator (0 thru 9)
n = Die revision (e.g. n=1 for die rev A, 2 for die rev B etc.)

CX24152/5 features

- MPEG-2 MP@ML video decoder supporting NTSC and PAL CCIR601 image resolution
- MPEG-1/MPEG-2 and Dolby Digital (AC-3) audio decoder
- MPEG-2/DVB/DIRECTV transport stream demultiplexing
- 1-45 Msym/sec QPSK/BPSK demodulator/FEC with DiSEqC 2.x signaling support
- NTSC channel 3/4 RF modulator
- NTSC/PAL/SECAM TV encoder supporting simultaneous CVBS, YC & RGB/YPrPb analog video output signals
- 3DES ciphering engine & integrated OTP memory for unique, IC security personalization
- On-chip boot ROM for secure STB software authentication
- Integrated DVB common descrambler & DES ECB descrambler
- NDS Videoguard conditional access hardware support
- 200 MHz 224 MIPS 32-bit ARM920 CPU with 16KB I & D caches and MMU
- Advanced 2D graphics rendering engine for alphablt, bitblt, textblt, line draw and color expansion acceleration
- Unified memory architecture supporting 16 or 32-bit SDRAM
- MPEG picture and still plane upscaling and downscaling
- Multiplane video/graphics image compositing with color key or 256-level alpha blending
- Video-picture-in-graphics with flexible picture size and aspect ratio
- Flicker filtering, aspect ratio conversion and hardware cursor
- 4/8/16-bit ARGB/A YCrCb graphics
- Integrated 32-bit 33 MHz PCI 2.1 bus bridge controller

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