

# Dual 4-bit static shift register

## BU4015B / BU4015BF

The BU4015B and BU4015BF are 4-stage static shift registers, each consisting of two circuits.

The D flip-flops for each stage share a common reset input, enabling external asynchronous reset at any point.

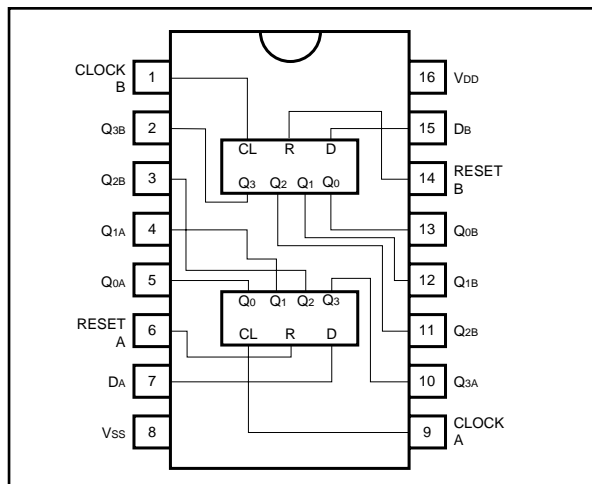
Also, the flip-flops at each stage are triggered by the rising edge of the clock input.

“H” level reset input resets the contents of all stages to “L”, regardless of the clock and data input, and sets data outputs Q0 to Q3 to “L”.

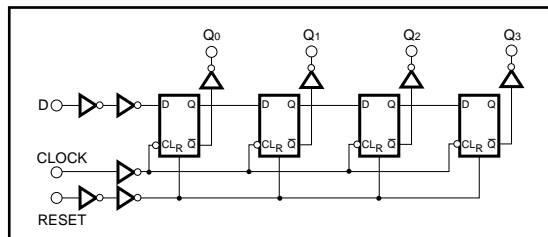
### ●Features

- 1) Low power dissipation.
- 2) Wide range of operating power supply voltages.
- 3) High input impedance.
- 4) High fan-out.
- 5) Direct drive of 2 L-TTL inputs and 1 LS-TTL input.

### ●Block diagram



### ●Logic circuit diagram



### ●Truth table

CLOCK	D	RESET	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
	L	L	L	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>
	H	L	H	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>
	X	L	No Change			
X	X	H	L	L	L	L

X : Irrelevant

●Absolute maximum ratings ( $V_{SS} = 0V$ ,  $T_a = 25^\circ C$ )

Parameter	Symbol	Limits	Unit
Power supply voltage	$V_{DD}$	$-0.3 \sim +18$	V
Power dissipation	$P_d$	1000 (DIP), 500 (SOP)	mW
Operating temperature	$T_{opr}$	$-40 \sim +85$	$^\circ C$
Storage temperature	$T_{stg}$	$-55 \sim +150$	$^\circ C$
Input voltage	$V_{IN}$	$-0.3 \sim V_{DD} + 0.3$	V

●Electrical characteristics

DC characteristics (unless otherwise noted,  $T_a = 25^\circ C$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit	$V_{DD}$ (V)	Conditions
Input high level voltage	$V_{IH}$	3.5	—	—	V	5	—
		7.0	—	—		10	
		11.0	—	—		15	
Input low level voltage	$V_{IL}$	—	—	1.5	V	5	—
		—	—	3.0		10	
		—	—	4.0		15	
Input high level current	$I_{IH}$	—	—	0.3	$\mu A$	15	$V_{IH} = 15V$
Input low level current	$I_{IL}$	—	—	-0.3	$\mu A$	15	$V_{IL} = 0V$
Output high level voltage	$V_{OH}$	4.95	—	—	V	5	$I_O = 0mA$
		9.95	—	—		10	
		14.95	—	—		15	
Output low level voltage	$V_{OL}$	—	—	0.05	V	5	$I_O = 0mA$
		—	—	0.05		10	
		—	—	0.05		15	
Output high level current	$I_{OH}$	-0.16	—	—	mA	5	$V_{OH} = 4.6V$
		-0.4	—	—		10	$V_{OH} = 9.5V$
		-1.2	—	—		15	$V_{OH} = 13.5V$
Output low level current	$I_{OL}$	0.44	—	—	mA	5	$V_{OL} = 0.4V$
		1.1	—	—		10	$V_{OL} = 0.5V$
		3.0	—	—		15	$V_{OL} = 1.5V$
Static current dissipation	$I_{DD}$	—	—	20	$\mu A$	5	$V_I = V_{DD}$ or GND
		—	—	40		10	
		—	—	80		15	

Switching characteristics (unless otherwise noted, Ta = 25°C, V<sub>SS</sub> = 0V, C<sub>L</sub> = 50pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V <sub>DD</sub> (V)	Conditions
Output rise time	t <sub>TLH</sub>	—	180	—	ns	5	—
		—	90	—		10	
		—	65	—		15	
Output fall time	t <sub>THL</sub>	—	100	—	ns	5	—
		—	50	—		10	
		—	40	—		15	
Propagation delay time, CLOCK, D→Q	t <sub>PLH</sub> t <sub>PHL</sub>	—	310	—	ns	5	—
		—	125	—		10	
		—	90	—		15	
Propagation delay time, RESET to Q	t <sub>PLH</sub> t <sub>PHL</sub>	—	460	—	ns	5	—
		—	180	—		10	
		—	120	—		15	
Setup time	t <sub>su</sub>	—	100	—	ns	5	—
		—	50	—		10	
		—	40	—		15	
Minimum clock pulse width	t <sub>WH</sub> (CLK)	—	185	—	ns	5	—
		—	85	—		10	
		—	55	—		15	
Minimum reset pulse width	t <sub>WH</sub> (R)	—	200	—	ns	5	—
		—	80	—		10	
		—	60	—		15	
Maximum clock frequency	f (CLK) Max.	—	20	—	MHz	5	—
		—	6.0	—		10	
		—	7.5	—		15	
Maximum clock rise time and fall time	t <sub>r</sub> (CLK) t <sub>f</sub> (CLK)	—	100	—	μs	5	—
		—	40	—		10	
		—	15	—		15	
Input capacitance	C <sub>IN</sub>	—	5	—	pF	—	—

[illegible]

The timing diagram for the 74VHC00 shows four signals: D, CLOCK, Q<sub>0</sub>, and RESET. The signals are defined by their transitions and timing parameters:

- D:** Data input signal. Transitions are marked with 20ns intervals. Setup time ( $t_{su}$ ) and hold time ( $t_{sh}$ ) are indicated relative to the clock edge.
- CLOCK:** Clock signal. Transitions are marked with 20ns intervals. Propagation delays ( $t_{PLH}$ ,  $t_{PHL}$ ) and pulse widths ( $t_{PW}$ ) are indicated.
- Q<sub>0</sub>:** Output signal. Transitions are marked with 90%, 50%, and 10% levels. Propagation delays ( $t_{TLH}$ ,  $t_{THL}$ ) and pulse widths ( $t_{PH}$ ,  $t_{PL}$ ) are indicated.
- RESET:** Reset signal. Transitions are marked with 10%, 50%, and 90% levels. Propagation delays ( $t_{PLH}$ ,  $t_{PHL}$ ) and pulse widths ( $t_{PW}$ ) are indicated.

Figure 1 is a line graph showing Power Dissipation (Pd in mW) on the Y-axis versus Ambient Temperature (Ta in °C) on the X-axis. The Y-axis ranges from 0 to 1200 mW in increments of 200. The X-axis ranges from 0 to 150 °C in increments of 25. Two lines are plotted: one for DIP16 and one for SOP16. Both lines show a linear decrease in power dissipation as ambient temperature increases, starting from a maximum value at 25 °C and reaching zero at 150 °C.

Ambient Temperature (Ta) (°C)	DIP16 Power Dissipation (Pd) (mW)	SOP16 Power Dissipation (Pd) (mW)
25	1000	550
50	800	440
75	600	330
100	400	220
125	200	110
150	0	0

Technical drawing of a 12-pin connector. The drawing includes three views: a top view, a side view, and a perspective view. The top view shows a rectangular component with a width of  $19.4 \pm 0.3$  and a height of  $6.5 \pm 0.3$ . It features 12 pins arranged in two rows of 6. The side view shows the profile of the component with a height of  $3.2 \pm 0.2$  and a pin height of  $4.25 \pm 0.03$ . The perspective view shows the component at an angle, with a width of  $7.62$  and a pin height of  $0.3 \pm 0.1$ . The drawing also includes dimensions for the pin pitch ( $2.54$ ), the pin diameter ( $0.51 \text{ Min.}$ ), and the pin length ( $0.5 \pm 0.1$ ).

The drawing shows three views of the connector:

- Top View:** A rectangular component with 16 pins. The overall width is  $10.0 \pm 0.2$ . The distance from the left edge to the first pin is  $6.2 \pm 0.3$ . The distance between the first and last pins is  $4.4 \pm 0.2$ . The distance from the last pin to the right edge is  $9.9$ . The pins are numbered 1 to 16.
- Side View:** Shows the profile of the connector. The total height is  $1.5 \pm 0.1$ . The height of the main body is  $0.11$ . The distance from the left edge to the start of the pins is  $1.27$ . The distance between the pins is  $0.4 \pm 0.1$ .
- Detail View:** A close-up of the pin and its housing. The distance from the housing edge to the pin tip is  $0.3 \text{ Min.}$ . The height of the housing above the pin is  $0.15 \pm 0.1$ .

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