Dual 4-bit static shift register

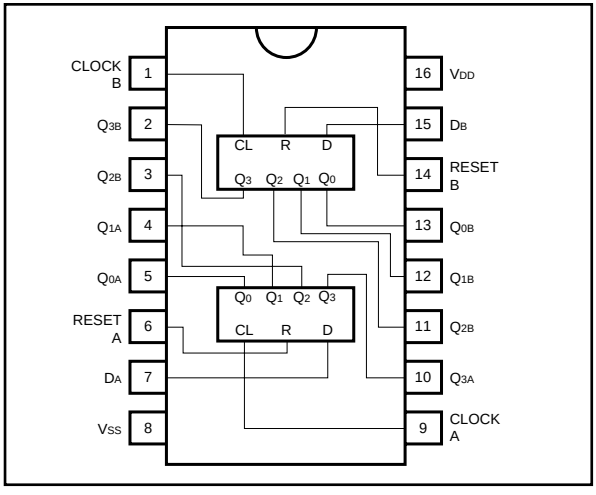
BU4015B / BU4015BF

The BU4015B and BU4015BF are 4-stage static shift registers, each consisting of two circuits.
The D flip-flops for each stage share a common reset input, enabling external asynchronous reset at any point.
Also, the flip-flops at each stage are triggered by the rising edge of the clock input.
“H” level reset input resets the contents of all stages to “L”, regardless of the clock and data input, and sets data outputs Q0 to Q3 to “L”.

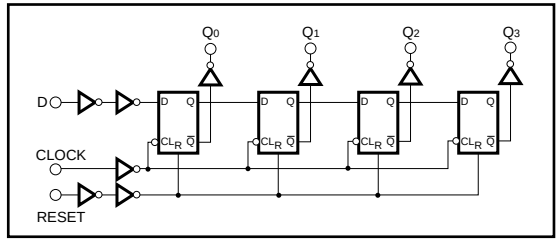
●Features

1) Low power dissipation.
2) Wide range of operating power supply voltages.
3) High input impedance.
4) High fan-out.
5) Direct drive of 2 L-TTL inputs and 1 LS-TTL input.

●Block diagram



●Logic circuit diagram



●Truth table

CLOCK	D	RESET	Q_0	Q_1	Q_2	Q_3
↑	L	L	L	Q_0	Q_1	Q_2
↑	H	L	H	Q_0	Q_1	Q_2
↓	X	L	No Change			
X	X	H	L	L	L	L

X : Irrelevant

●Absolute maximum ratings (V_{SS} = 0V, Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	– 0.3 ~ + 18	V
Power dissipation	Pd	1000 (DIP), 500 (SOP)	mW
Operating temperature	Topr	– 40 ~ + 85	°C
Storage temperature	Tstg	– 55 ~ + 150	°C
Input voltage	V_{IN}	– 0.3 ~ V_{DD} + 0.3	V

●Electrical characteristics

DC characteristics (unless otherwise noted, Ta = 25°C, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V_{DD} (V)	Conditions
Input high level voltage	V_{IH}	3.5	—	—	V	5	—
		7.0	—	—		10	
		11.0	—	—		15	
Input low level voltage	V_{IL}	—	—	1.5	V	5	—
		—	—	3.0		10	
		—	—	4.0		15	
Input high level current	I_{IH}	—	—	0.3	μA	15	V_{IH} = 15V
Input low level current	I_{IL}	—	—	– 0.3	μA	15	V_{IL} = 0V
Output high level voltage	V_{OH}	4.95	—	—	V	5	I_O = 0mA
		9.95	—	—		10	
		14.95	—	—		15	
Output low level voltage	V_{OL}	—	—	0.05	V	5	I_O = 0mA
		—	—	0.05		10	
		—	—	0.05		15	
Output high level current	I_{OH}	– 0.16	—	—	mA	5	V_{OH} = 4.6V
		– 0.4	—	—		10	V_{OH} = 9.5V
		– 1.2	—	—		15	V_{OH} = 13.5V
Output low level current	I_{OL}	0.44	—	—	mA	5	V_{OL} = 0.4V
		1.1	—	—		10	V_{OL} = 0.5V
		3.0	—	—		15	V_{OL} = 1.5V
Static current dissipation	I_{DD}	—	—	20	μA	5	V_I = V_{DD} or GND
		—	—	40		10	
		—	—	80		15	

Switching characteristics (unless otherwise noted, Ta = 25°C, V_{SS} = 0V, C_L = 50pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V_{DD} (V)	Conditions
Output rise time	t_{TLH}	—	180	—	ns	5	—
		—	90	—		10	
		—	65	—		15	
Output fall time	t_{THL}	—	100	—	ns	5	—
		—	50	—		10	
		—	40	—		15	
Propagation delay time, CLOCK, D→Q	t_{PLH} t_{PHL}	—	310	—	ns	5	—
		—	125	—		10	
		—	90	—		15	
Propagation delay time, RESET to Q	t_{PLH} t_{PHL}	—	460	—	ns	5	—
		—	180	—		10	
		—	120	—		15	
Setup time	t_{su}	—	100	—	ns	5	—
		—	50	—		10	
		—	40	—		15	
Minimum clock pulse width	$t_{WH\ (CLK)}$	—	185	—	ns	5	—
		—	85	—		10	
		—	55	—		15	
Minimum reset pulse width	$t_{WH\ (R)}$	—	200	—	ns	5	—
		—	80	—		10	
		—	60	—		15	
Maximum clock frequency	$f_{(CLK)\ Max.}$	—	20	—	MHz	5	—
		—	6.0	—		10	
		—	7.5	—		15	
Maximum clock rise time and fall time	$t_{r\ (CLK)}$ $t_{f\ (CLK)}$	—	100	—	µs	5	—
		—	40	—		10	
		—	15	—		15	
Input capacitance	C_{IN}	—	5	—	pF	—	—

●Measurement circuits

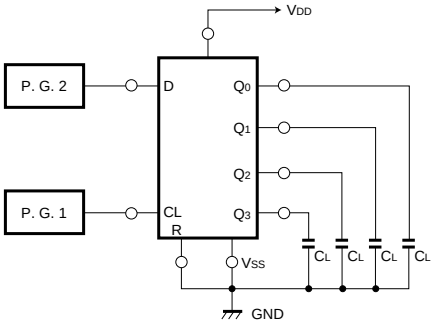


Fig.1 Switching characteristics measurement circuit

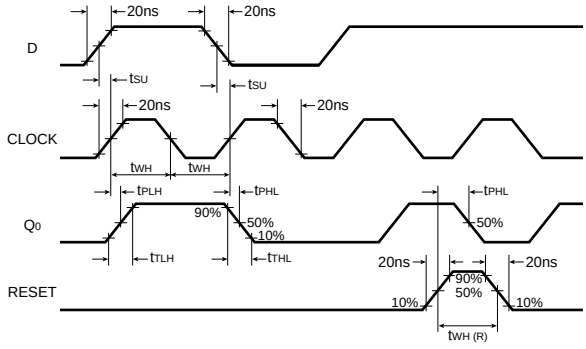


Fig.2 Switching time measurement waveform

●Electrical characterisistic curve

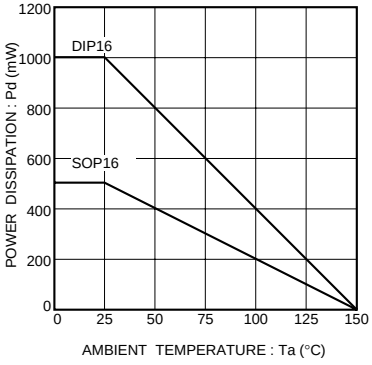
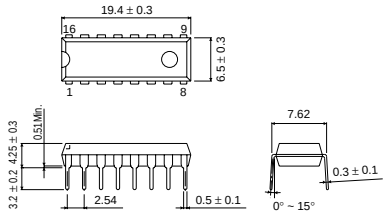


Fig.3 Power dissipation vs. ambient temperature

●External dimensions (Units: mm)

BU4015B



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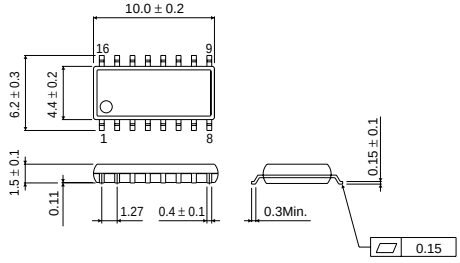

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