HI-201HS/883

High Speed Quad SPST CMOS Analog Switch

FN8265
Rev.0.00
April 9, 2012

The HI-201HS/883 is a monolithic CMOS analog switch featuring very fast switching speeds and low ON resistance. This integrated circuit consists of four independently selectable SPST switches and is pin compatible with the industry standard HI-201 switch.

Fabricated using silicon-gate technology and the Intersil dielectric isolation process, this TTL compatible device offers improved performance over previously available CMOS analog switches while eliminating the problem of latch-up associated with other fabrication processes. Featuring maximum switching times of 50ns, low ON resistance of 50Ω maximum, and a wide analog signal range, the HI-201HS/883 is designed for any military application where improved switching performance, particularly switching speed, is required. (A more detailed discussion on the design and application of the HI-201HS/883 can be found in Application Note AN543.)

The HI-201HS/883 is available in a 16 Ld CerDIP package and is specified over the temperature range of -55°C to +125°C.

Features

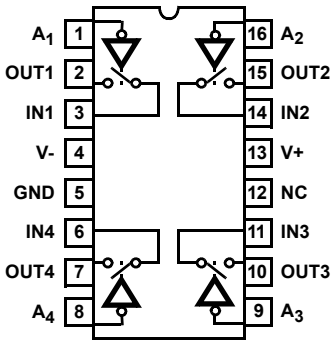
- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low "On" Release . . . . . 50Ω Max
- Wide Analog Signal Range . . . . . ±15V
- Turn-On Time. 50ns
- Analog Current Range (Continuous) 25mA
- TTL/CMOS Compatible
- No Latch-Up
- Pin Compatible with Standard HI-201

Applications

- High Speed Multiplexing
- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Op Amp Gain Switching Networks
- Integrator Reset Circuits

Pin Configuration

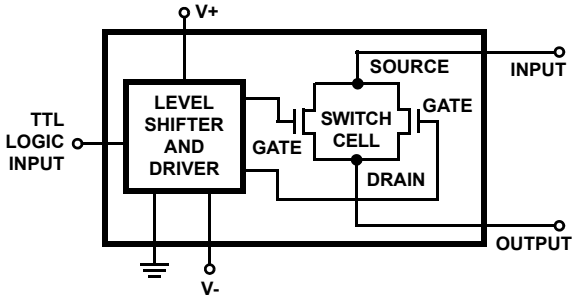
HI1-0201HS/883
(16 LD CERDIP)
TOP VIEW



TRUTH TABLE

LOGIC	SWITCH
0	ON
1	OFF

Functional Diagram



Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI1-0201HS/883	HI1-201HS/883	-55 to +125	16 Ld CerDIP	F16.3

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) . . . . . $\pm$18V
Analog Input Voltage, ($+V_S$) . . . . . $+V_{SUPPLY}$ +2V
($-V_S$) . . . . . $-V_{SUPPLY}$ -2V
Digital Input Voltage, ($+V_A$) . . . . . $+V_{SUPPLY}$ +4V
($-V_A$) . . . . . $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 50mA
Continuous Current Any Terminal (Except S or D) 25mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CerDIP Package	75	16

Package Power Dissipation at +75°C
CerDIP Package 1.0W
Package Power Dissipation Derating Factor above +75°C
CerDIP Package . . . . . 13.36mW/°C
Junction Temperature . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . ≤275°C

Recommended Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage Range ($\pm V_{SUPPLY}$) . . . . . $\pm$15V
Analog Input Voltage (V_S) . . . . . $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) . . . . . 0V to 0.8V
Logic High Level (V_{AH}) . . . . . 3.0V to $+V_{SUPPLY}$

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V, unless otherwise specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Switch "ON" Resistance	r_{DS}	V_A = 0.8V, V_S = 10V, I_D = -1mA All Unused Channels V_{AL} = 0.8V	1	+25	-	50	Ω
			2, 3	-55 to +125	-	75	Ω
		V_A = 0.8V, V_S = -10V, I_D = 1mA All Unused Channels V_{AL} = 0.8V	1	+25	-	50	Ω
			2, 3	-55 to +125	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = +14V, V_D = -14V, V_{AH} = 3.0V All Unused Channels V_{AH} = 3.0V, V_D = +14V, V_S = -14V	1	+25	-10	10	nA
			2, 3	-55 to +125	-100	100	nA
		V_S = -14V, V_D = +14V, V_{AH} = 3.0V All Unused Channels V_{AH} = 3.0V, V_D = -14V, V_S = +14V	1	+25	-10	10	nA
			2, 3	-55 to +125	-100	100	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = -14V, V_S = +14V, V_{AH} = 3.0V All Unused Channels V_{AH} = 3.0V, V_D = +14V, V_S = -14V	1	+25	-10	10	nA
			2, 3	-55 to +125	-100	100	nA
		V_D = +14V, V_S = -14V, V_{AH} = 3.0V All Unused Channels V_{AH} = 3.0V, V_D = -14V, V_S = +14V	1	+25	-10	10	nA
			2, 3	-55 to +125	-100	100	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = +14V, V_{AL} = 0.8V, All Unused Channels V_{AL} = 0.8V, V_D = V_S = -14V	1	+25	-10	10	nA
			2, 3	-55 to +125	-100	100	nA
		V_D = V_S = -14V, V_{AL} = 0.8V, All Unused Channels V_{AL} = 0.8V, V_D = V_S = +14V	1	+25	-10	10	nA
			2, 3	-55 to +125	-100	100	nA
Low Level Input Current	I_{AL}	V_{AL} = 0.8V All Unused Channels V_{AH} = 4.0V	1	+25	-	500	µA
			2, 3	-55 to +125	-	500	µA
High Level Input Current	I_{AH}	V_{AH} = 4.0V All Unused Channels V_{AL} = 0.8V	1	+25	-	40	µA
			2, 3	-55 to +125	-	40	µA
Supply Current	$+I_{CC}$	All Channels V_{AL} = 0.8V	1, 2	+25, +125	-	10	mA
			3	-55	-	10	mA
		All Channels V_{AH} = 3.0V	1, 2	+25, +125	-	10	mA
			3	-55	-	10	mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V, unless otherwise specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Supply Current	$-I_{CC}$	All Channels V_{AL} = 0.8V	1, 2	+25, +125	-	6	mA
			3	-55	-	6	mA
		All Channels V_{AH} = 3.0V	1, 2	+25, +125	-	6	mA
			3	-55	-	6	mA

TABLE 2. A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V, unless otherwise specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Turn “ON” Time	$t_{(ON)}$	C_L = 35pF, R_L = 1kΩ V_{AH} = 3.0V, V_{AL} - 0.8V	9	+25	-	50	ns
			10, 11	-55, +125	-	100	ns
Turn “OFF” Time	$t_{(OFF)}$	C_L = 35pF, R_L = 1kΩ V_{AH} = 3.0V, V_{AL} - 0.8V	9	+25	-	50	ns
			10, 11	-55, +125	-	100	ns

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (NOTE 1)

Device Characterized at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, GND = 0V

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE (°C)	MIN	MAX	UNITS
Address Capacitance	C_A	f = 1MHz, V_{AL} = 0V	1	+25	-	35	pF
Switch Input Capacitance	$C_{S\ (OFF)}$	f = 1MHz, V_{AH} = 5V, Measure Input to GND	1	+25	-	20	pF
Switch Output Capacitance	$C_{D\ (OFF)}$	f = 1MHz, V_{AH} = 5V, Measure Output to Ground	1	+25	-	20	pF
	$C_{D\ (ON)}$	f = 1MHz, V_{AL} = 0V, Measure Output to Ground	1	+25	-	50	pF
Drain to Source Capacitance	C_{DS}	f = 1MHz, V_{AH} = 5V	1	+25	-	2.0	pF
Off Isolation	V_{ISO}	f = 100kHz, V_A = 3.0, R_L = 1k, V_{GEN} = $1V_{P-P}$, C_L = 10pF	1	+25	50	-	dB
Cross Talk	V_{CT}	f = 100kHz, V_A = 3.0, R_L = 1k, V_{GEN} = $1V_{P-P}$, C_L = 10pF	1	+25	50	-	dB
Charge Transfer Error	V_{CTE}	R_L = 1k, C_L = 0.01µF	1	+25	-	10	mV

NOTE:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (Tables 1 and 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1 (Note 2), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

NOTE:

2. PDA applies to Subgroup 1 only.

Test Circuits

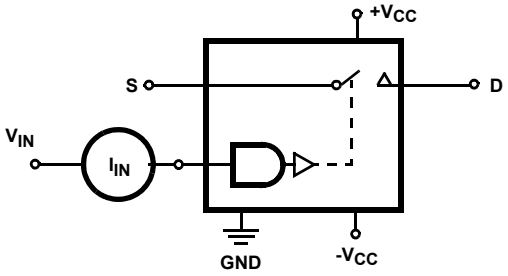


FIGURE 1. INPUT LEAKAGE CURRENT

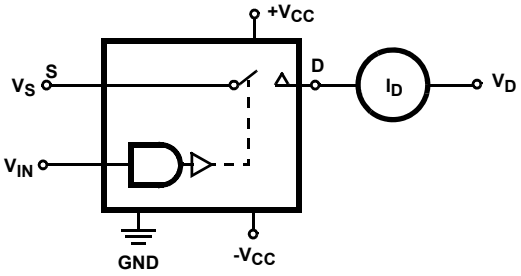


FIGURE 2. $I_{D(OFF)}$

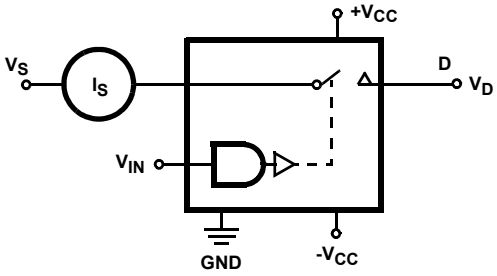


FIGURE 3. $I_{S(OFF)}$

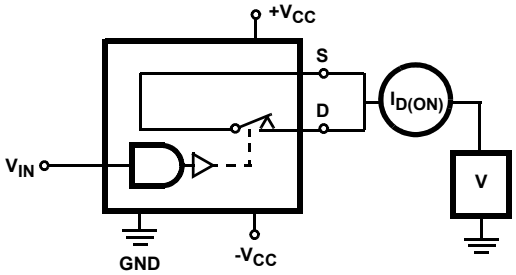


FIGURE 4. $I_{D(ON)}$

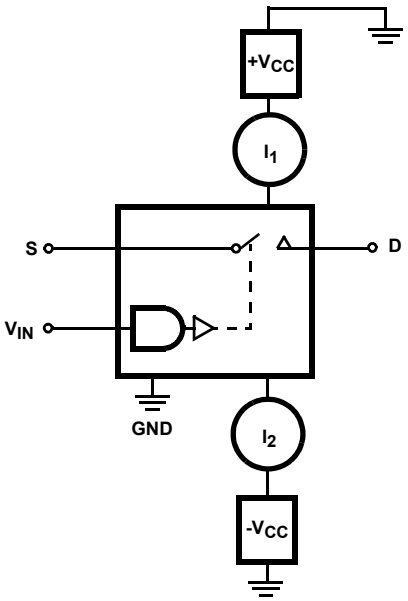
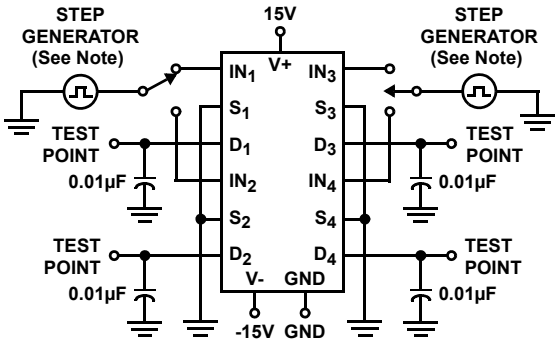


FIGURE 5. SUPPLY CURRENTS



NOTE: The pulse generator has the following characteristics:
V_{GEN} = 0V to 3V, rise time ≤ 20ns, fall time ≤ 20ns, PRR = 100kHz.

FIGURE 6. CHARGE TRANSFER ERROR

Test Circuits (Continued)

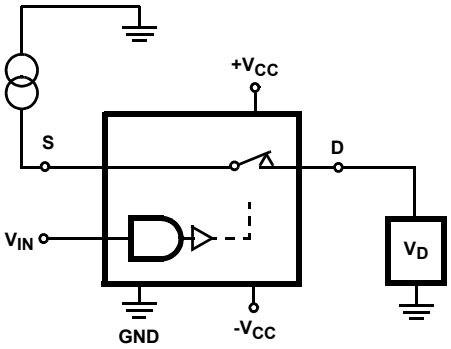
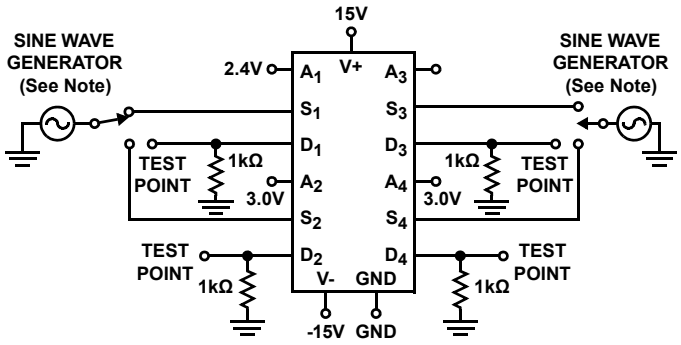
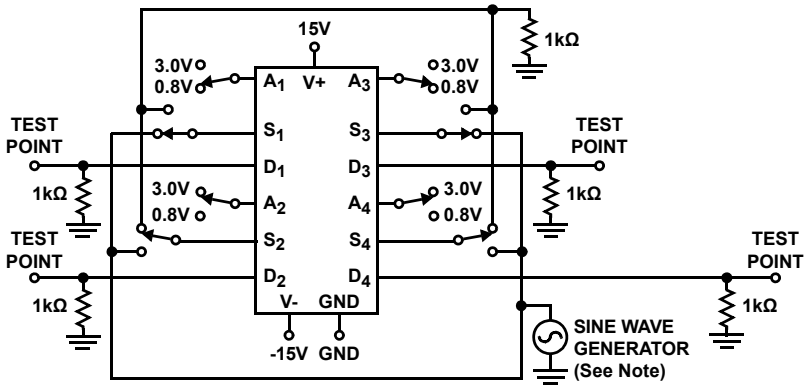


FIGURE 7. R_{DS}



NOTE: The pulse generator has the following characteristics: V_{GEN} = $1V_{P-P}$, Frequency = 100kHz.

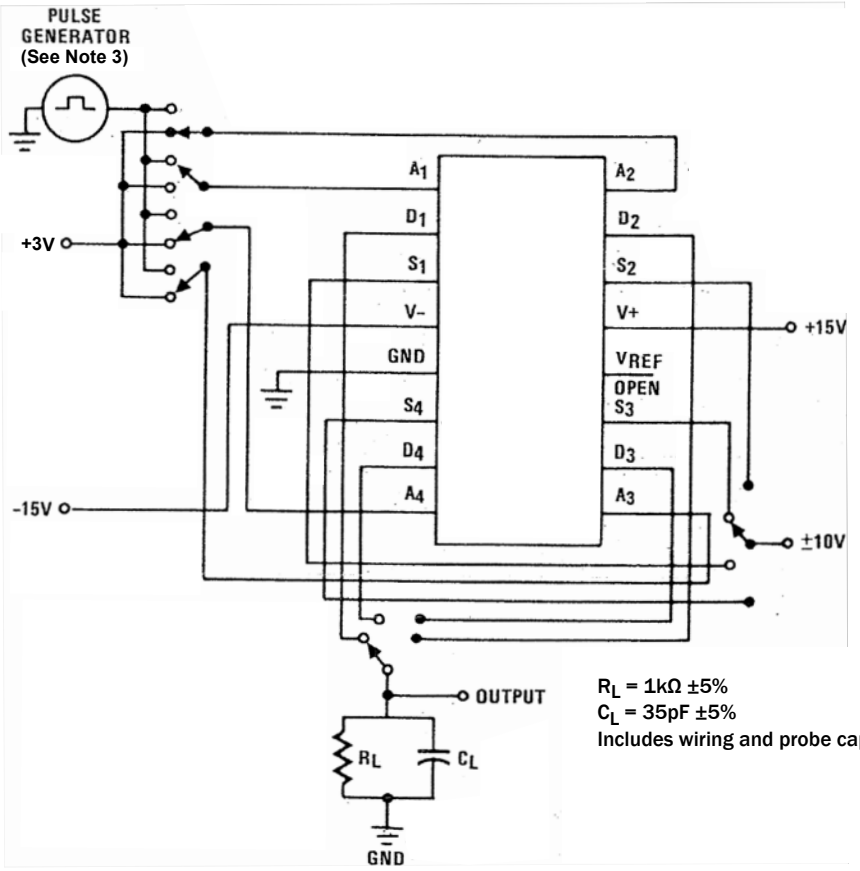
FIGURE 8. OFF CHANNEL ISOLATION



NOTE: The pulse generator has the following characteristics: V_{GEN} = $1V_{P-P}$, Frequency = 100kHz.

FIGURE 9. CROSSTALK BETWEEN CHANNELS

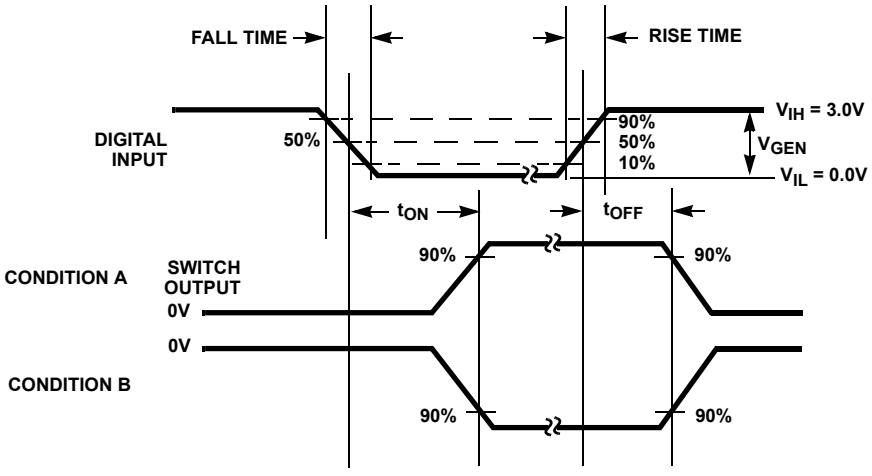
Switching Waveforms



R_L = 1kΩ ±5%
C_L = 35pF ±5%
Includes wiring and probe capacitance

NOTES:

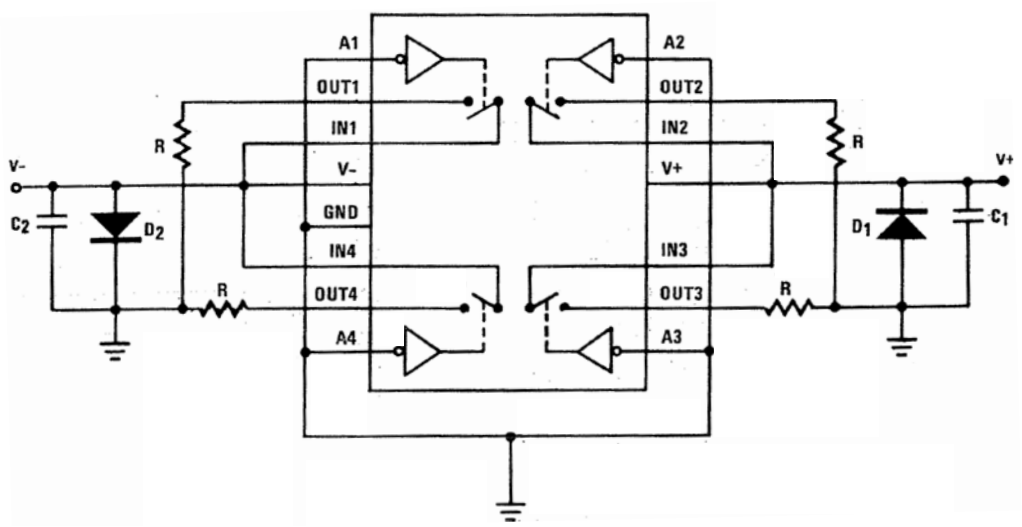
3. The pulse generator has the following characteristics: V_{GEN} = 3.0V, t_{THL} ≤ 20ns
4. See Table 2 for complete terminal conditions



NOTE: Rise time and fall time ≤20ns.

Burn-In Circuit

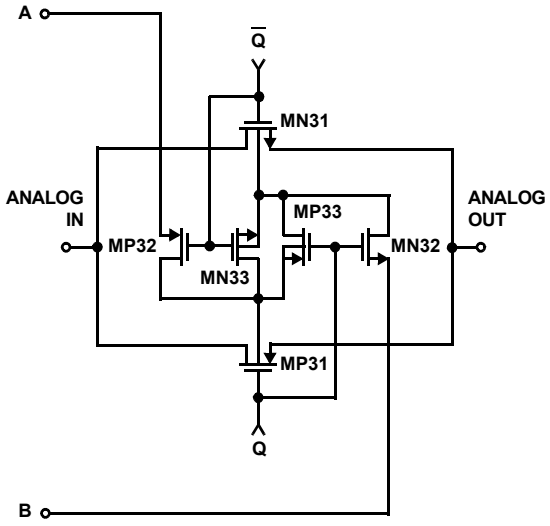
HI-201HS/883 CERDIP



NOTE:
R = 10kΩ, 5%, 1/4W or 1/2W.
$C_1 = C_2 = 0.01\mu F$ (per socket) or 0.1µF (per row).
$D_1 = D_2$ = IN4002 or equivalent (one per board).
|(V+) - (V-)| = 30V.

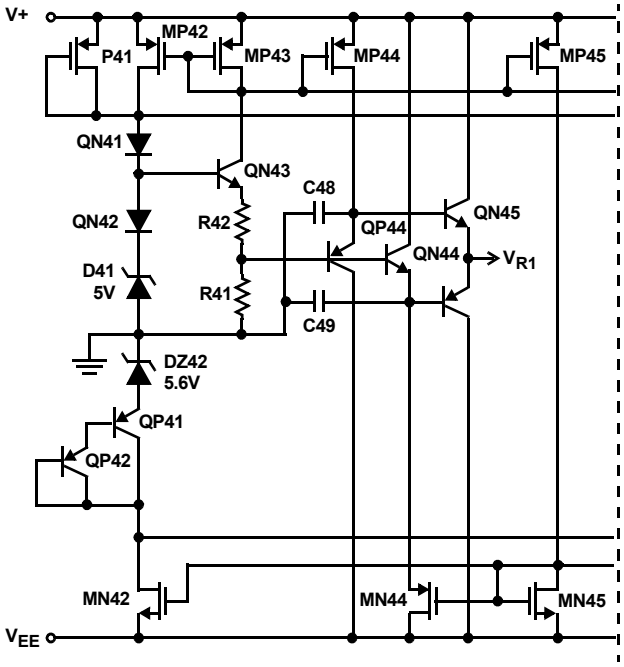
Schematic Diagrams

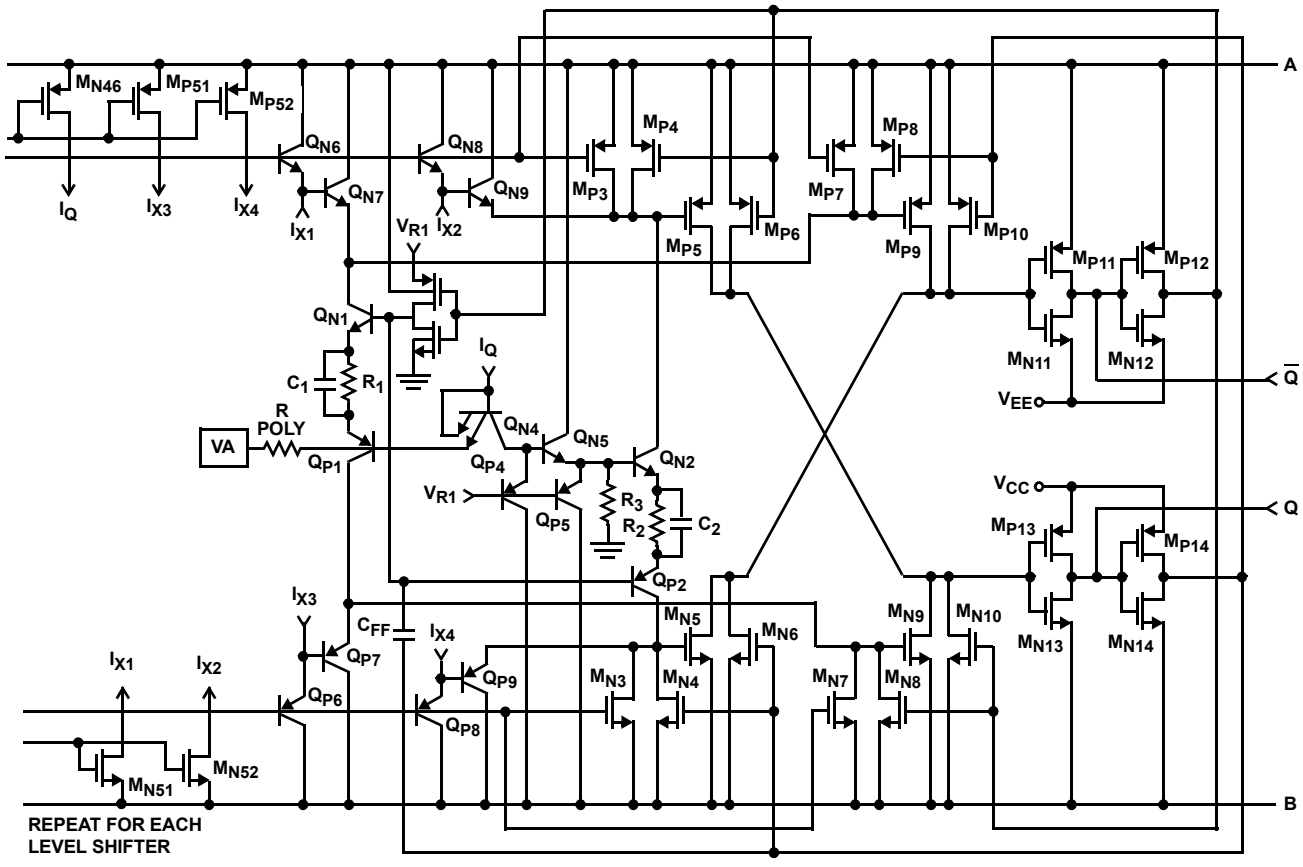
SWITCH CELL



Schematic Diagrams (Continued)

REFERENCE/LEVEL SHIFTER





Die Characteristics

DIE DIMENSIONS:

92mils x 111mils x 19mils

METALLIZATION:

Type: Aluminum
Thickness: 16kÅ ±2kÅ

GLASSIVATION:

Type: Nitride
Nitride Thickness: 7kÅ ±0.7kÅ

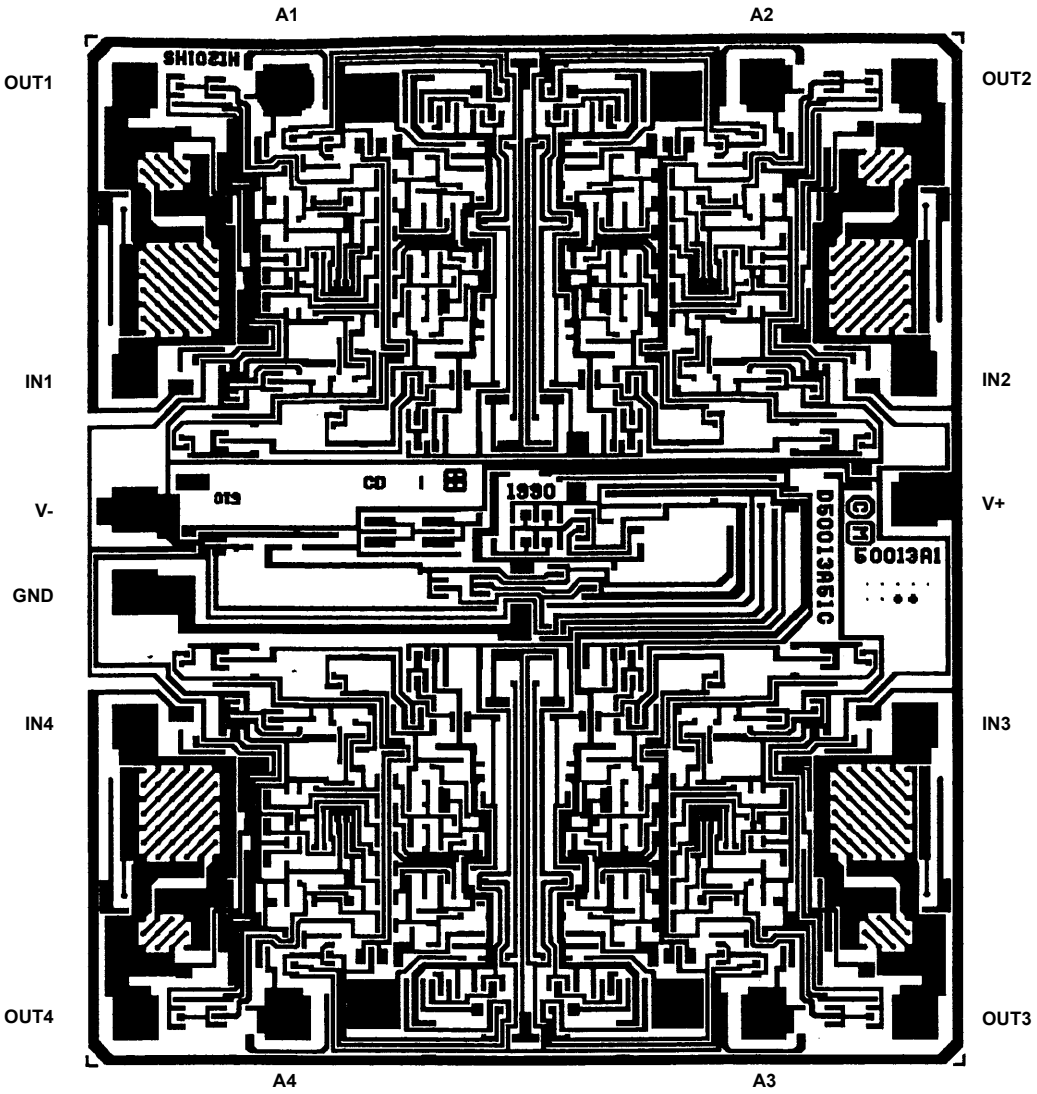
WORST CASE CURRENT DENSITY:

$4.5 \times 10^5 A/cm^2$ at 25mA

This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

Metallization Mask Layout

HI-201HS/883



The information contained in this section has been developed through characterization and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 3.0V$, $V_{AL} = 0.8V$

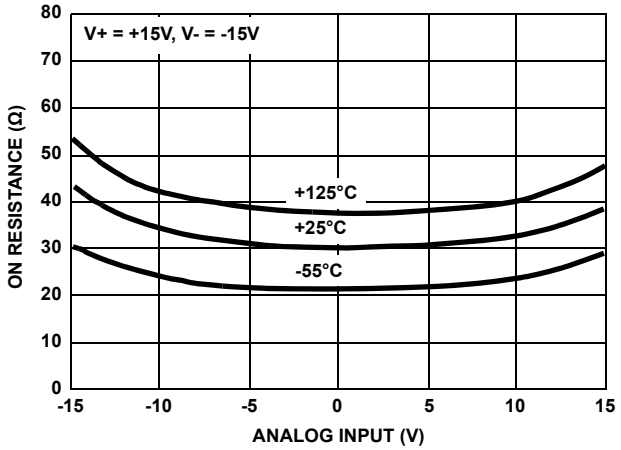


FIGURE 10. ON RESISTANCE vs ANALOG SIGNAL LEVEL AND TEMPERATURE

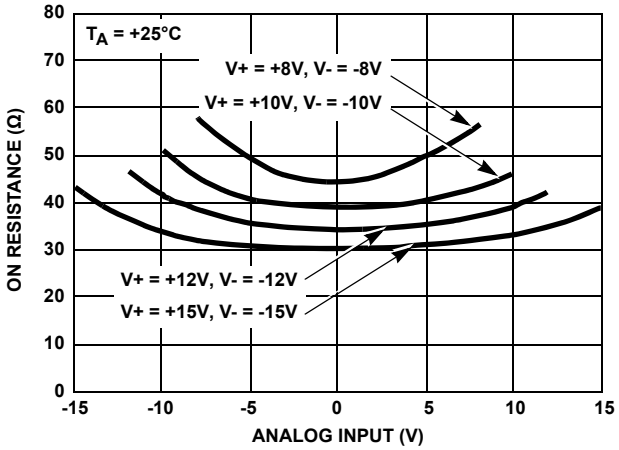


FIGURE 11. ON RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

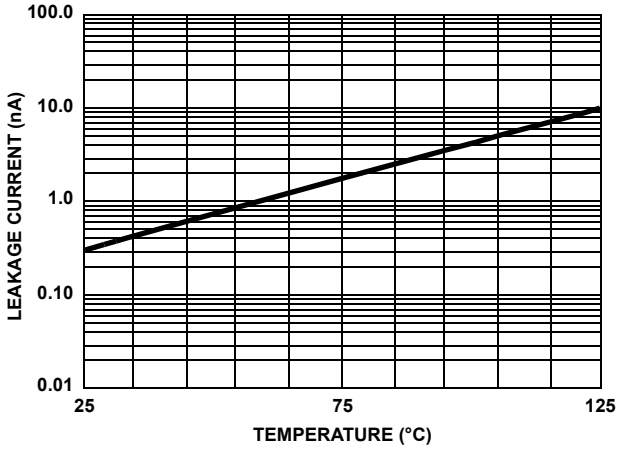


FIGURE 12. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE

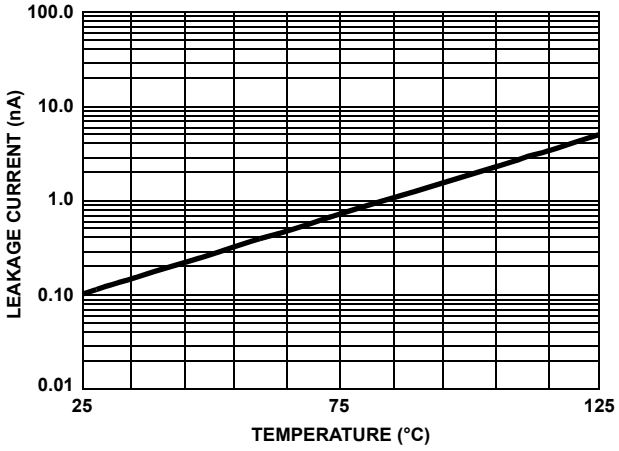


FIGURE 13. $I_{D(ON)}$ vs TEMPERATURE

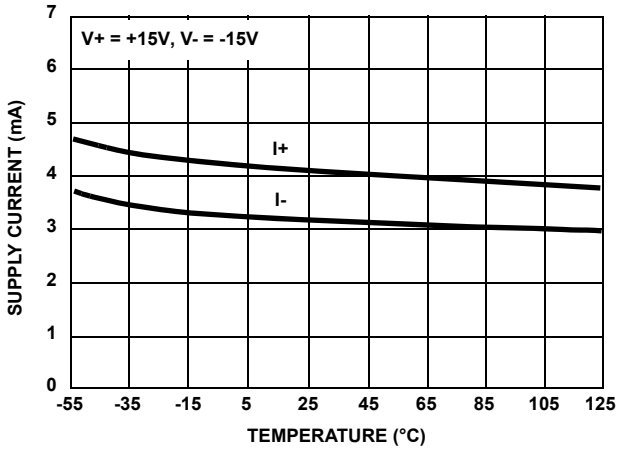


FIGURE 14. SUPPLY CURRENT vs TEMPERATURE

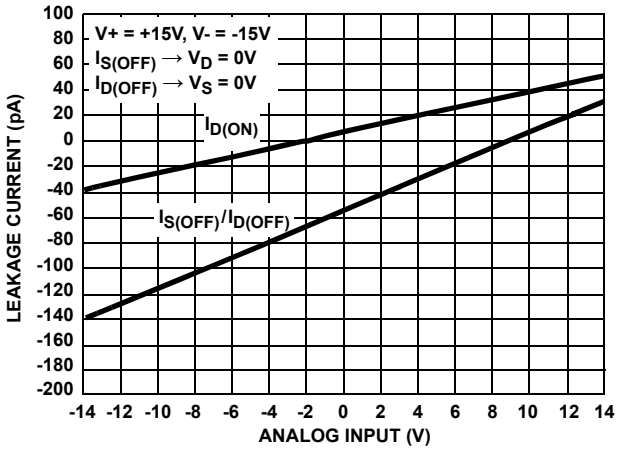


FIGURE 15. LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE

The information contained in this section has been developed through characterization and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 3.0V$, $V_{AL} = 0.8V$ **(Continued)**

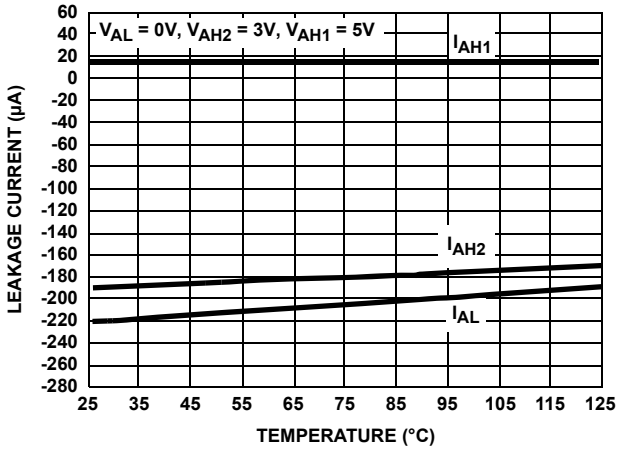


FIGURE 16. DIGITAL INPUT LEAKAGE CURRENT vs TEMPERATURE

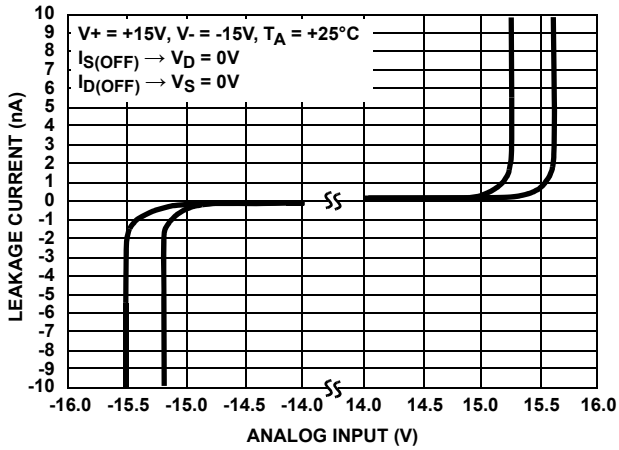


FIGURE 17. LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE

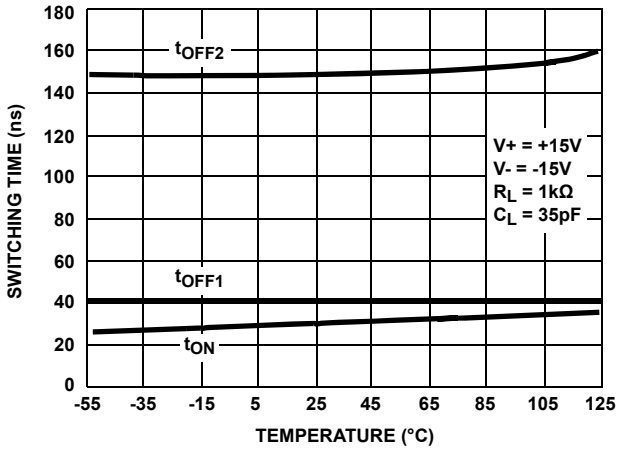


FIGURE 18. SWITCHING TIME vs TEMPERATURE

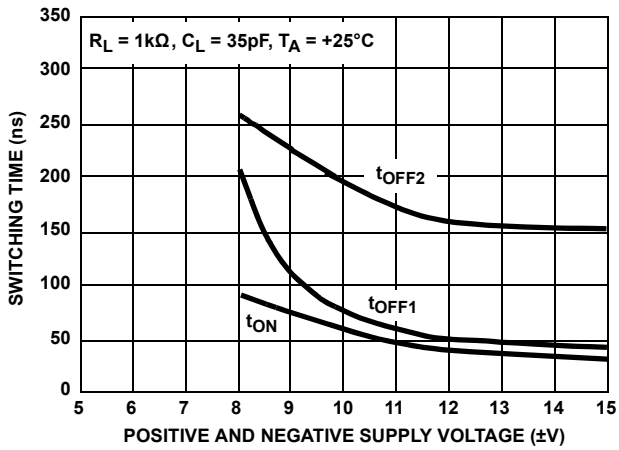


FIGURE 19. SWITCHING TIME vs POSITIVE AND NEGATIVE SUPPLY VOLTAGE

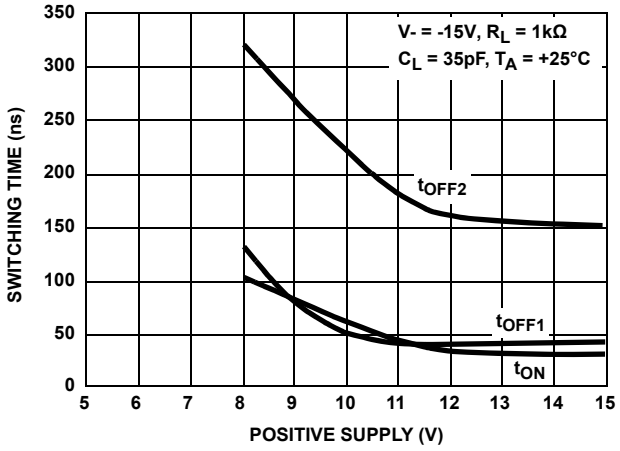


FIGURE 20. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE

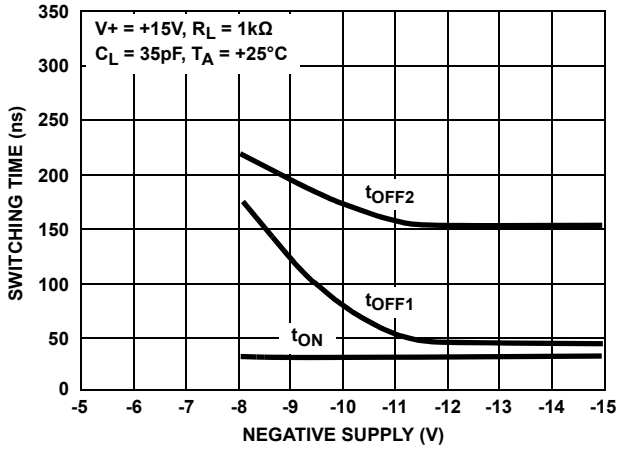


FIGURE 21. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE

The information contained in this section has been developed through characterization and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 3.0V$, $V_{AL} = 0.8V$ **(Continued)**

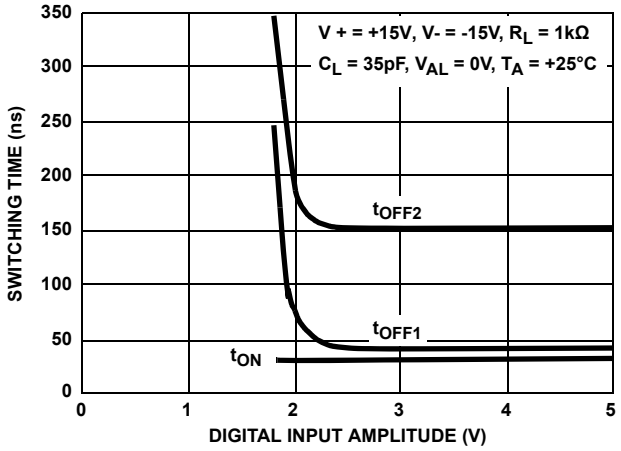


FIGURE 22. SWITCHING TIME vs INPUT LOGIC AMPLITUDE

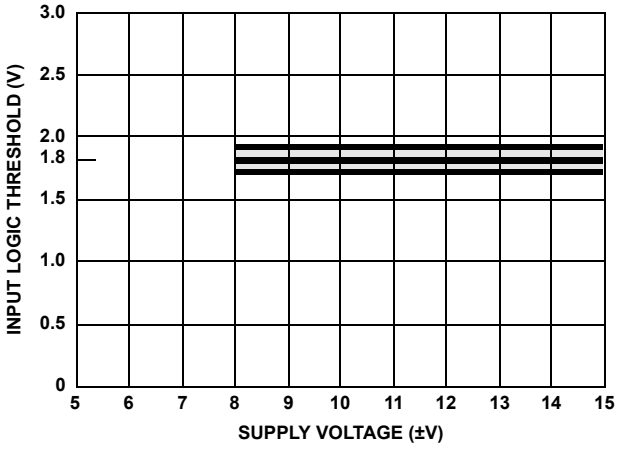


FIGURE 23. INPUT SWITCHING THRESHOLD vs POSITIVE AND NEGATIVE SUPPLY VOLTAGE

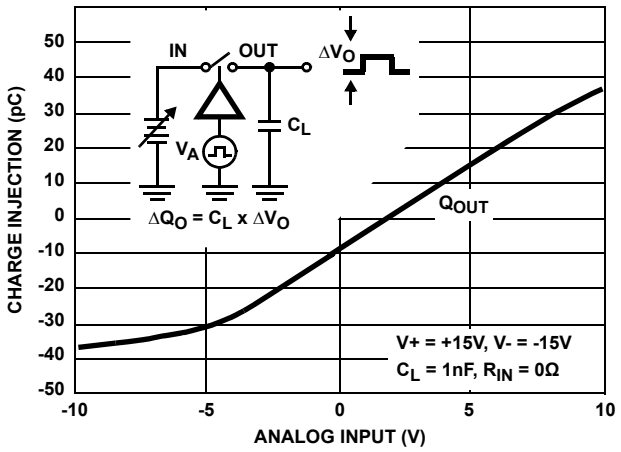


FIGURE 24. CHARGE INJECTION vs ANALOG INPUT

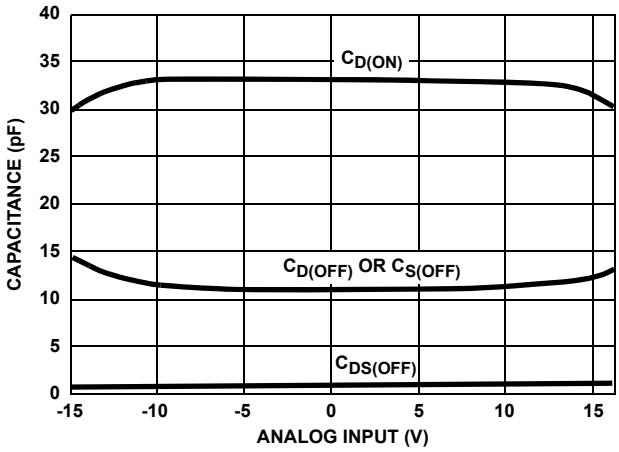


FIGURE 25. CAPACITANCE vs ANALOG INPUT

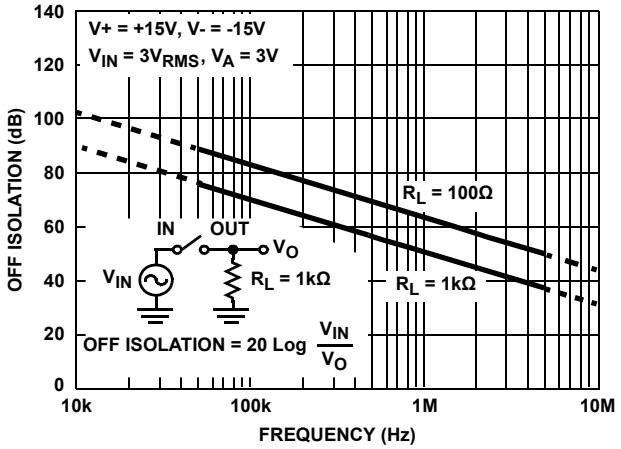


FIGURE 26. OFF ISOLATION vs FREQUENCY

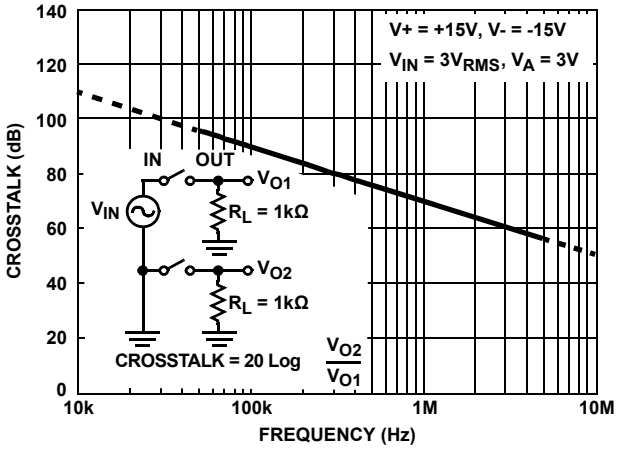
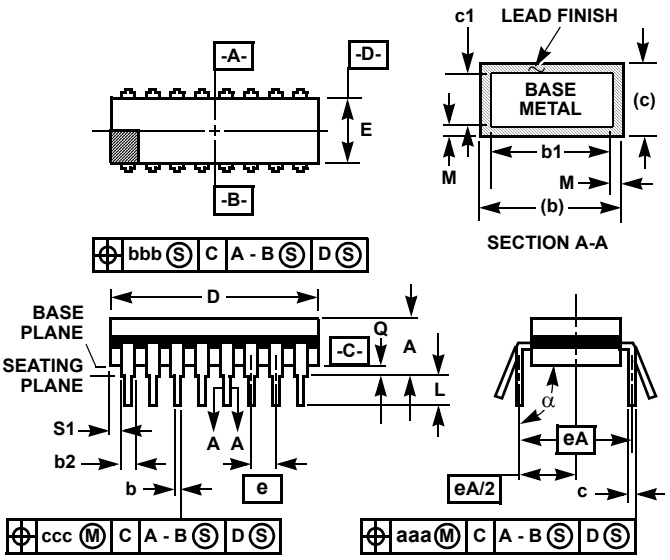


FIGURE 27. CROSSTALK vs FREQUENCY

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

Rev. 0 4/94