



Integrated Device Technology, Inc.

16-BIT BUS SWITCH

IDT74FST163245
IDT74FST163P245
ADVANCE INFORMATION

FEATURES:

- Bus switches provide zero delay paths
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- Low switch on-resistance:
FST163xxx – 5Ω
FST163Pxxx – 5Ω with precharge
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- Available in SSOP, TSSOP and TVSOP

DESCRIPTION:

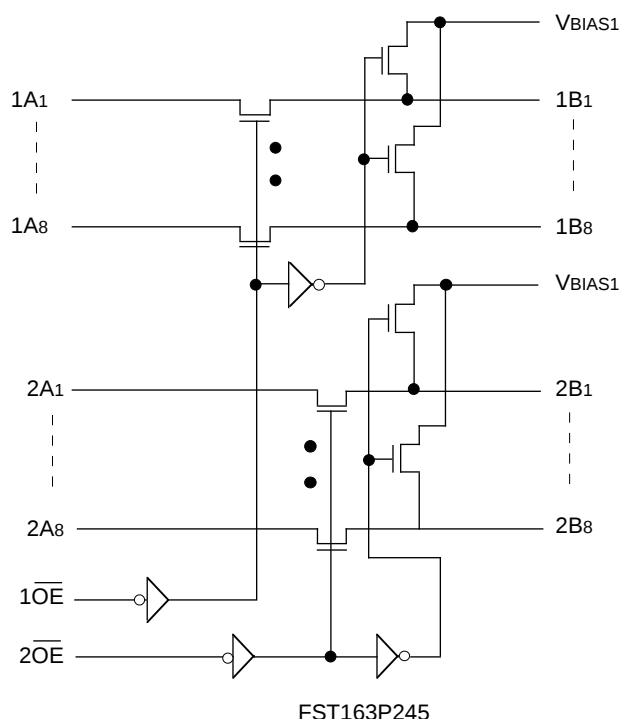
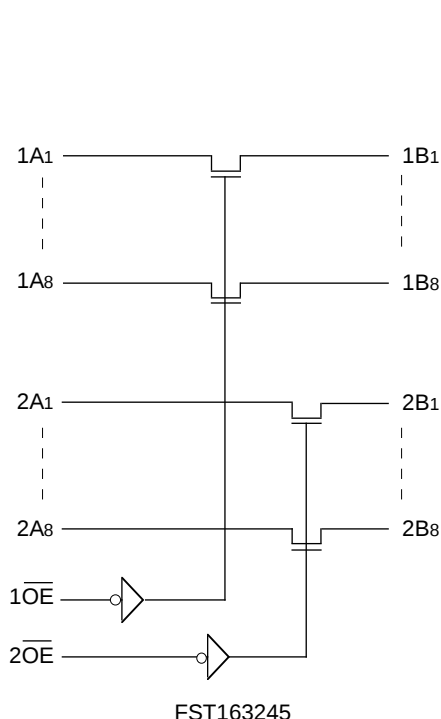
The FST163245/163P245 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or

no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no Vcc applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST163245 and FST163P245 are 16-bit TTL-compatible bus switches. The $\overline{\text{OE}}$ pins provide enable control. The FST163P245 supports precharge on the B port. So when $\overline{\text{OE}}$ is high, A and B ports are isolated and B outputs are precharged to the bias voltage through the equivalent of a $10\text{K}\Omega$ resistor (1B1-8 precharged to VBIAS1 and 2B1-8 precharged to VBIAS1).

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Names	I/O	Description
1A1-8, 2A1-8	I/O	Bus A
1B1-8, 2B1-8	I/O	Bus B
$1\overline{\text{OE}}$, $2\overline{\text{OE}}$	I	Bus Switch Enable (Active LOW)
VBIAS1	I	Precharge Reference Voltage

3513 tbl 01

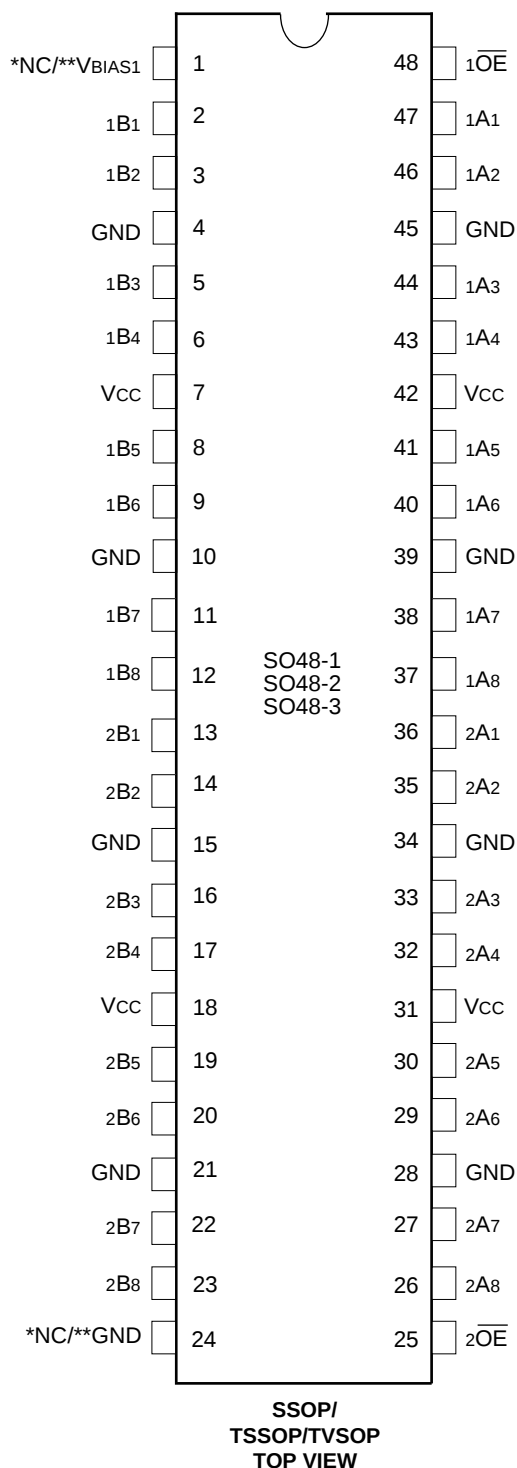
3513 drw 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE

FEBRUARY 1997

PIN CONFIGURATION



*FST163245
**FST163P245

3513 drw 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	Maximum Continuous Channel Current	128	mA

NOTES:

3513 tbl 02

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC}, Control and Switch terminals.

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Typ.	Unit
C _{IN}	Control Input Capacitance		4	pF
C _{I/O}	Switch Input/Output Capacitance	Switch Off		pF

NOTES:

3513 tbl 04

- Capacitance is characterized but not tested
- T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

FUNCTION TABLE

Inputs x $\overline{\text{OE}}$	Outputs
L	Bus B Data to Bus A
H	High Z State (163245) Precharge Bus B to VBIAS (163P245)

3513 tbl 03

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
I_{IL}	Input LOW Voltage		$V_I = \text{GND}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	± 1	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 1	
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		—	300	—	mA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
R_{ON}	Switch On Resistance ⁽⁴⁾	$V_{CC} = \text{Min.}, V_{IN} = 0.0\text{V}$ $I_{ON} = 30\text{mA}$	163xxx, 163Pxxx	—	5	7	Ω
		$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}$ $I_{ON} = 15\text{mA}$	163xxx, 163Pxxx	—	10	15	Ω
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN}$ or $V_O \leq 4.5\text{V}$		—	—	1	μA
I_O	Precharge Output Current ⁽⁵⁾	$V_{CC} = \text{Min.}, \text{BIASV} = 2.4\text{V}, V_O = 0\text{V}$		0.15	—	—	mA
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or V_{CC}		—	0.1	3	μA

NOTES:

3513 tbl 05

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Measured by voltage drop between ports at indicated current through the switch.
- This parameter applies to the FST163P245 only.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open Enable Pin Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	30	40	μA / MHz/ Switch
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open Enable Pins Toggling (16 Switches Toggling) $f_i = 10\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	4.8	6.4	mA
			$V_{IN} = 3.4$ $V_{IN} = GND$	—	5.3	7.9	

NOTES:

3513 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_i = \text{Input Frequency}$
 $N = \text{Number of Switches Toggling at } f_i$
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^\circ C$ to $+85^\circ C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Description	Condition ⁽¹⁾	Min. ⁽²⁾	Typ.	Max.	Unit
t_{PLH}	Data Propagation Delay A_i to B_i , B_i to A_i ^(3,4)	$C_L = 50pF$ $R_L = 500\Omega$	—	—	0.25	ns
t_{PZH}	Switch Turn on Delay $\overline{OE}$ to A_i , B_i		1.5	—	6.5	ns
t_{PHZ}	Switch Turn off Delay $\overline{OE}$ to A_i , B_i		1.5	—	5.5	ns
t_{PLZ}						
$ Q_{CI} $	Charge Injection ^(5,6)		—	1.5	—	pC

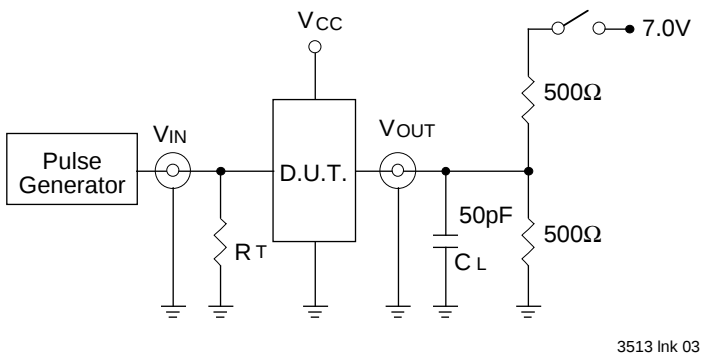
NOTES:

3513 tbl 07

- See test circuit and waveforms.
- Minimum limits guaranteed but not tested.
- This parameter is guaranteed by design but not tested.
- The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 2.5ns for 50pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay on the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- Measured at switch turn off, load = 50 pF in parallel with 10M Ω scope probe, $V_{IN} = 0.0$ volts.
- Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

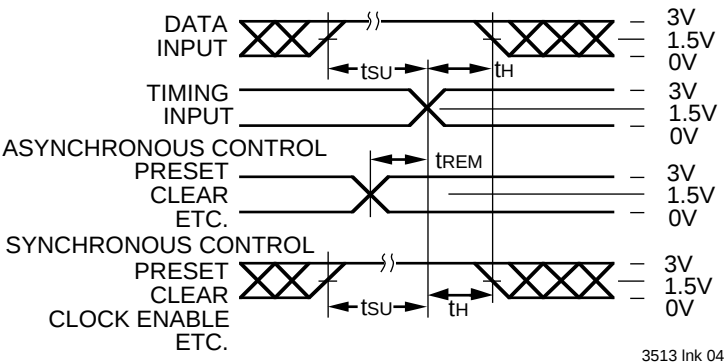
DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.

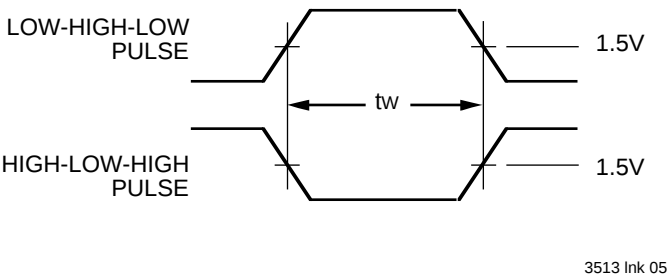
RT= Termination resistance: should be equal to ZOUT of the Pulse Generator.

3513 Ink 08

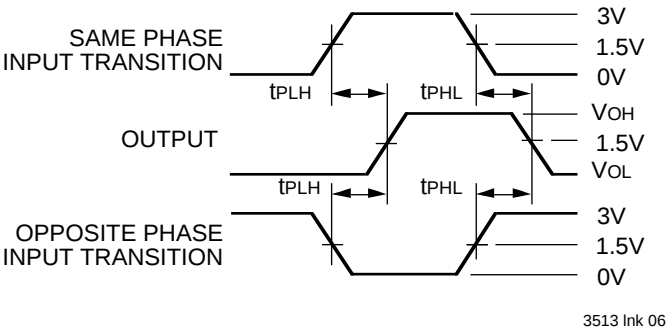
SET-UP, HOLD AND RELEASE TIMES



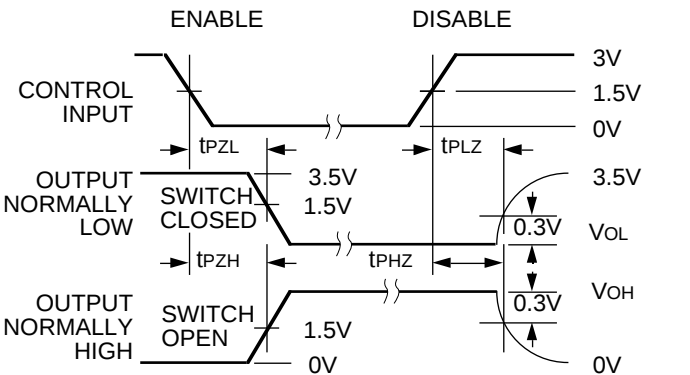
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH

2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns

3513 Ink 07

ORDERING INFORMATION

IDT	XX	FST	16 XX	X		
Temp. Range		Device Type		Package		
				PV	Shrink Small Outline Package (SO48-1)	
				PA	Thin Shrink Small Outline Package (SO48-2)	
				PF	Thin Very Small Outline Package (SO48-3)	
				163245	16-Bit Bus Switch	
				163P245	16-Bit Bus Switch with Precharge	
				74	−40°C to +85°C	

3513 drw 08