



74HC4067; 74HCT4067

16-channel analog multiplexer/demultiplexer

Rev. 10 — 25 July 2024

Product data sheet

1. General description

The 74HC4067; 74HCT4067 is a single-pole 16-throw analog switch (SP16T) suitable for use in analog or digital 16:1 multiplexer/demultiplexer applications. The switch features four digital select inputs (S0, S1, S2 and S3), sixteen independent inputs/outputs (Yn), a common input/output (Z) and a digital enable input (E). When E is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 10.0 V
- Input levels S0, S1, S2, S3 and $\bar{E}$ inputs:
 - For 74HC4067: CMOS level
 - For 74HCT4067: TTL level
- CMOS low power dissipation
- High noise immunity
- Low ON resistance:
 - 80 Ω (typical) at $V_{CC} = 4.5$ V
 - 70 Ω (typical) at $V_{CC} = 6.0$ V
 - 60 Ω (typical) at $V_{CC} = 9.0$ V
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Typical 'break before make' built-in

3. Applications

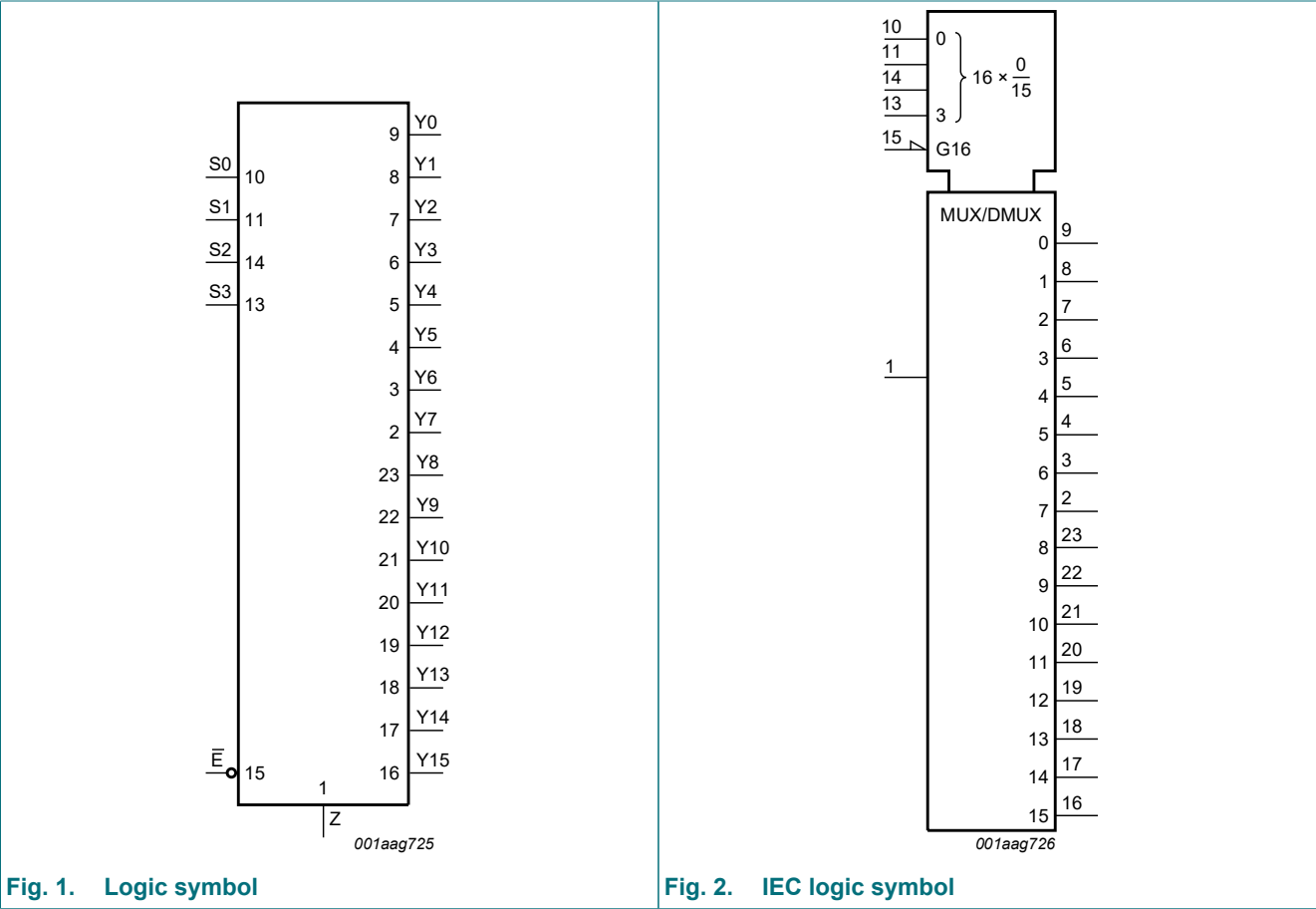
- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4067D	-40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74HC4067PW 74HCT4067PW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74HC4067BQ 74HCT4067BQ	-40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

5. Functional diagram



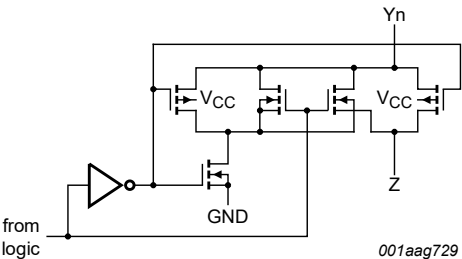


Fig. 3. Schematic diagram (one switch)

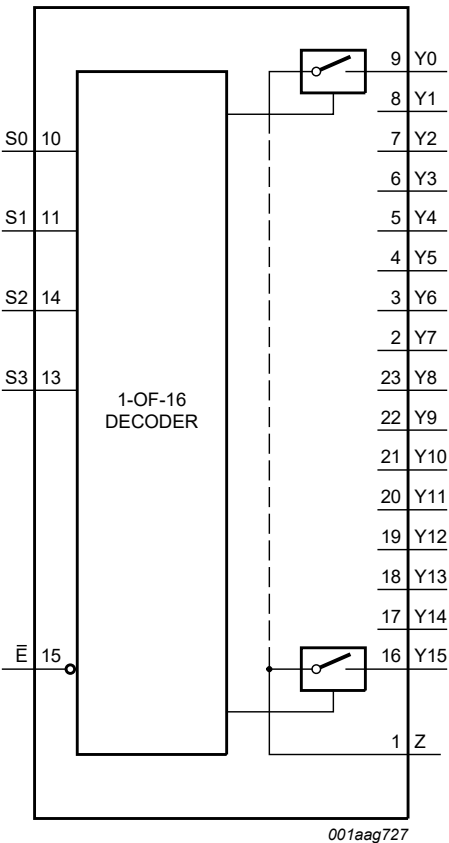


Fig. 4. Functional diagram

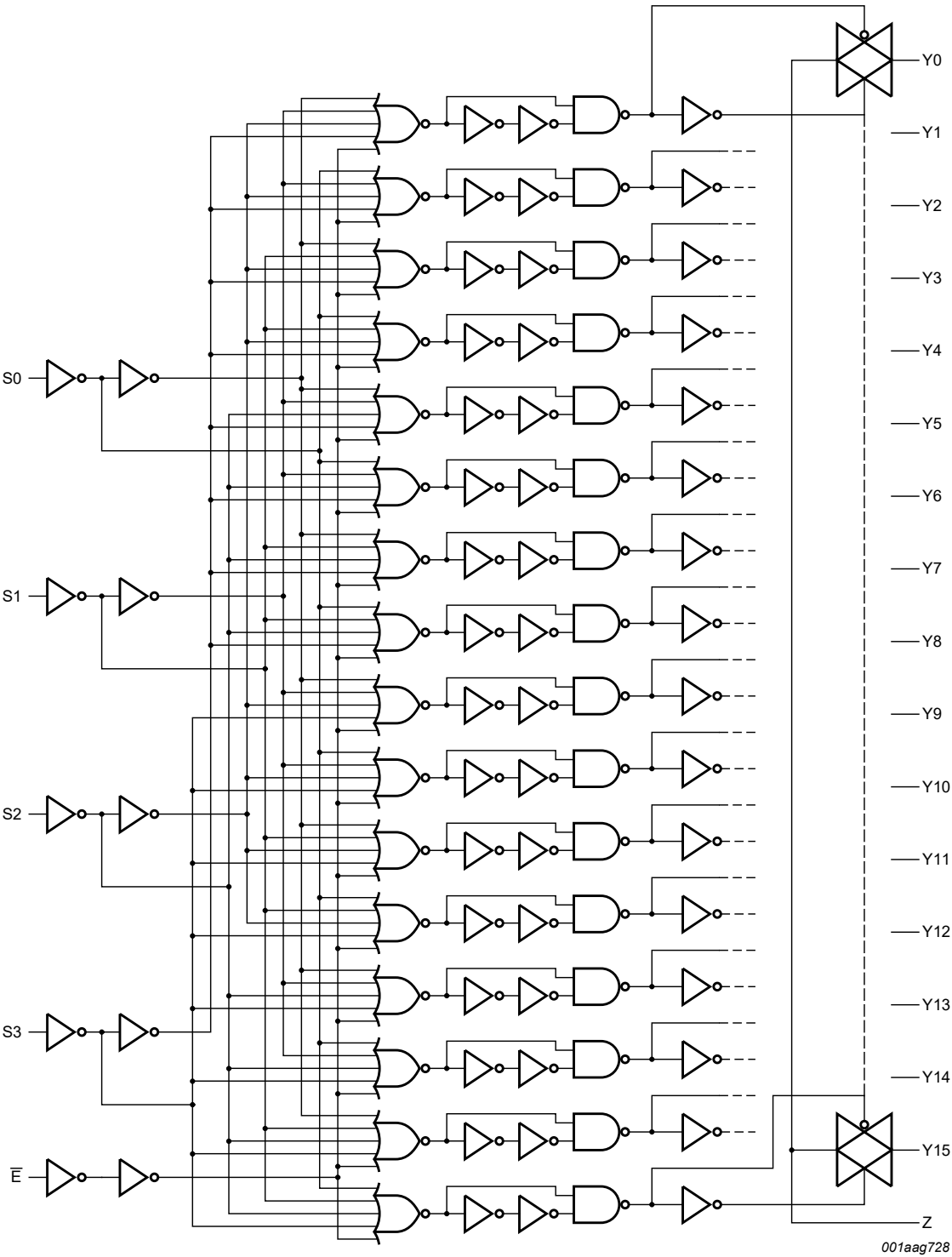


Fig. 5. Logic diagram

6. Pinning information

6.1. Pinning

D package
SOT137-1 (SO24)

Z 1 24 V_{CC}
Y7 2 23 Y8
Y6 3 22 Y9
Y5 4 21 Y10
Y4 5 20 Y11
Y3 6 19 Y12
Y2 7 18 Y13
Y1 8 17 Y14
Y0 9 16 Y15
S0 10 15 $\bar{E}$
S1 11 14 S2
GND 12 13 S3

aaa-034689

PW package
SOT355-1 (TSSOP24)

Z 1 24 V_{CC}
Y7 2 23 Y8
Y6 3 22 Y9
Y5 4 21 Y10
Y4 5 20 Y11
Y3 6 19 Y12
Y2 7 18 Y13
Y1 8 17 Y14
Y0 9 16 Y15
S0 10 15 $\bar{E}$
S1 11 14 S2
GND 12 13 S3

aaa-034667

BQ package
SOT815-1 (DHVQFN24)

terminal 1 index area

Z 1 24 V_{CC}
Y7 2 23 Y8
Y6 3 22 Y9
Y5 4 21 Y10
Y4 5 20 Y11
Y3 6 19 Y12
Y2 7 18 Y13
Y1 8 17 Y14
Y0 9 16 Y15
S0 10 15 $\bar{E}$
S1 11 14 S2
GND 12 13 S3

V_{CC}(1)

Transparent top view

aaa-034672

(1) This is not a V_{CC} pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to V_{CC}.

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Z	1	common input or output
Y7, Y6, Y5, Y4, Y3, Y2, Y1, Y0, Y15, Y14, Y13, Y12, Y11, Y10, Y9, Y8	2, 3, 4, 5, 6, 7, 8, 9, 16, 17, 18, 19, 20, 21, 22, 23	independent input or output
S0, S1, S2, S3	10, 11, 14, 13	address input
GND	12	ground (0 V)
$\overline{E}$	15	enable input (active LOW)
V _{CC}	24	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs					Channel ON
$\overline{E}$	S3	S2	S1	S0	
L	L	L	L	L	Y0 to Z
L	L	L	L	H	Y1 to Z
L	L	L	H	L	Y2 to Z
L	L	L	H	H	Y3 to Z
L	L	H	L	L	Y4 to Z
L	L	H	L	H	Y5 to Z
L	L	H	H	L	Y6 to Z
L	L	H	H	H	Y7 to Z
L	H	L	L	L	Y8 to Z
L	H	L	L	H	Y9 to Z
L	H	L	H	L	Y10 to Z
L	H	L	H	H	Y11 to Z
L	H	H	L	L	Y12 to Z
L	H	H	L	H	Y13 to Z
L	H	H	H	L	Y14 to Z
L	H	H	H	H	Y15 to Z
H	X	X	X	X	-

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage	[1]	-0.5	+11.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{SK}	switch clamping current	V _{SW} < -0.5 V or V _{SW} > V _{CC} + 0.5 V	-	±20	mA
I _{SW}	switch current	V _{SW} = -0.5 V to V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	500	mW
P	power dissipation	per switch	-	100	mW

- [1] To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_n. In this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or GND.
- [2] For SOT137-1 (SO24) package: P_{tot} derates linearly with 16.2 mW/K above 119 °C.
For SOT355-1 (TSSOP24) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT815-1 (DHVQFN24) package: P_{tot} derates linearly with 15.0 mW/K above 117 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4067			74HCT4067			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	10.0	4.5	5.0	5.5	V
V _I	input voltage		GND	-	V _{CC}	GND	-	V _{CC}	V
V _{SW}	switch voltage		GND	-	V _{CC}	GND	-	V _{CC}	V
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns
		V _{CC} = 10.0 V	-	-	31	-	-	-	ns
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

10. Static characteristics

Table 6. R_{ON} resistance per switch for types 74HC4067 and 74HCT4067

$V_I = V_{IH}$ or V_{IL} ; for test circuit see Fig. 6.

V_{is} is the input voltage at a Y_n or Z terminal, whichever is assigned as an input.

V_{os} is the output voltage at a Y_n or Z terminal, whichever is assigned as an output.

For 74HC4067: $V_{CC} - GND = 2.0\text{ V}$, 4.5 V , 6.0 V and 9.0 V .

For 74HCT4067: $V_{CC} - GND = 4.5\text{ V}$.

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
			Typ	Max	Max	Max	
R _{ON(peak)}	ON resistance (peak)	$V_{is} = V_{CC}$ to GND					
		$V_{CC} = 2.0\text{ V}$; $I_{SW} = 100\text{ }\mu\text{A}$ [1]	-	-	-	-	Ω
		$V_{CC} = 4.5\text{ V}$; $I_{SW} = 1000\text{ }\mu\text{A}$	110	180	225	270	Ω
		$V_{CC} = 6.0\text{ V}$; $I_{SW} = 1000\text{ }\mu\text{A}$	95	160	200	240	Ω
		$V_{CC} = 9.0\text{ V}$; $I_{SW} = 1000\text{ }\mu\text{A}$	75	130	165	195	Ω
R _{ON(rail)}	ON resistance (rail)	$V_{is} = GND$ or V_{CC}					
		$V_{CC} = 2.0\text{ V}$; $I_{SW} = 100\text{ }\mu\text{A}$ [1]	150	-	-	-	
		$V_{CC} = 4.5\text{ V}$; $I_{SW} = 1000\text{ }\mu\text{A}$	90	160	200	240	Ω
		$V_{CC} = 6.0\text{ V}$; $I_{SW} = 1000\text{ }\mu\text{A}$	80	140	175	210	Ω
		$V_{CC} = 9.0\text{ V}$; $I_{SW} = 1000\text{ }\mu\text{A}$	70	120	150	180	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_{is} = V_{CC}$ to GND					
		$V_{CC} = 2.0\text{ V}$ [1]	-	-	-	-	Ω
		$V_{CC} = 4.5\text{ V}$	9	-	-	-	Ω
		$V_{CC} = 6.0\text{ V}$	8	-	-	-	Ω
		$V_{CC} = 9.0\text{ V}$	6	-	-	-	Ω

[1] At supply voltages ($V_{CC} - GND$) approaching 2 V, the analog switch ON resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

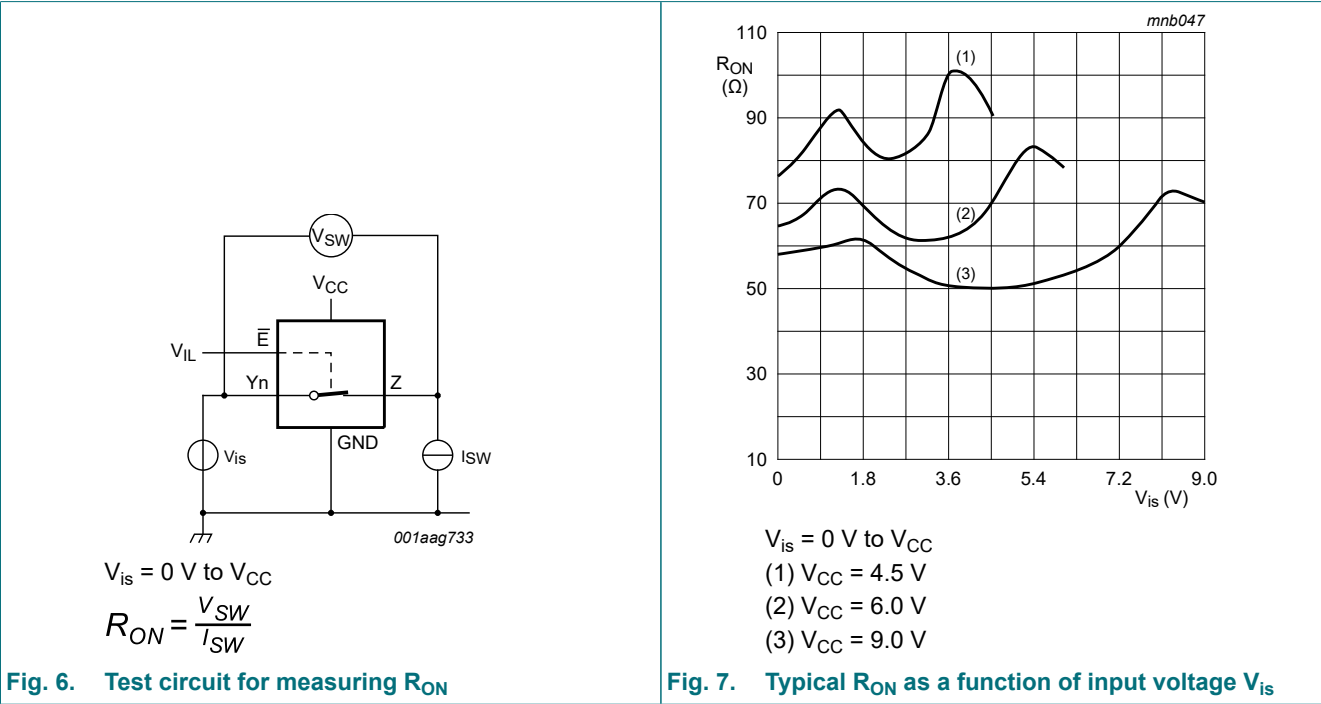


Table 7. Static characteristics 74HC4067

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	V
		V _{CC} = 9.0 V	6.3	4.7	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.80	V
		V _{CC} = 9.0 V	-	4.3	2.70	V
I _I	input leakage current	V _I = V _{CC} or GND				
		V _{CC} = 6.0 V	-	-	±0.1	µA
		V _{CC} = 10.0 V	-	-	±0.2	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 10.0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Fig. 8				
		per channel	-	-	±0.1	µA
		all channels	-	-	±0.8	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 10.0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Fig. 9	-	-	±0.8	µA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{is} = GND or V _{CC} ; V _{os} = V _{CC} or GND				
		V _{CC} = 6.0 V	-	-	8.0	µA
		V _{CC} = 10.0 V	-	-	16.0	µA
C _I	input capacitance		-	3.5	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
		V _{CC} = 9.0 V	6.3	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.50	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.80	V
		V _{CC} = 9.0 V	-	-	2.70	V
I _I	input leakage current	V _I = V _{CC} or GND				
		V _{CC} = 6.0 V	-	-	±1.0	µA
		V _{CC} = 10.0 V	-	-	±2.0	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 10.0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Fig. 8				
		per channel	-	-	±1.0	µA
		all channels	-	-	±8.0	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 10.0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Fig. 9	-	-	±8.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{is} = GND or V _{CC} ; V _{os} = V _{CC} or GND				
		V _{CC} = 6.0 V	-	-	80.0	µA
		V _{CC} = 10.0 V	-	-	160	µA
T _{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
		V _{CC} = 9.0 V	6.3	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.50	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.80	V
		V _{CC} = 9.0 V	-	-	2.70	V
I _I	input leakage current	V _I = V _{CC} or GND				
		V _{CC} = 6.0 V	-	-	±1.0	µA
		V _{CC} = 10.0 V	-	-	±2.0	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 10.0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Fig. 8				
		per channel	-	-	±1.0	µA
		all channels	-	-	±8.0	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 10.0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Fig. 9	-	-	±8.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{is} = GND or V _{CC} ; V _{os} = V _{CC} or GND				
		V _{CC} = 6.0 V	-	-	160	µA
		V _{CC} = 10.0 V	-	-	320	µA

Table 8. Static characteristics 74HCT4067

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

V_{IS} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

V_{OS} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 5.5 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Fig. 8				
		per channel	-	-	±0.1	µA
		all channels	-	-	±0.8	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 5.5 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Fig. 9	-	-	±0.8	µA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{IS} = GND or V _{CC} ; V _{OS} = V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V	-	-	8.0	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V				
		pin E	-	60	216	µA
		pin Sn	-	50	180	µA
C _I	input capacitance		-	3.5	-	pF
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1.0	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 5.5 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Fig. 8				
		per channel	-	-	±1.0	µA
		all channels	-	-	±8.0	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 5.5 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Fig. 9	-	-	±8.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{IS} = GND or V _{CC} ; V _{OS} = V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V	-	-	80.0	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V				
		pin E	-	-	270	µA
		pin Sn	-	-	225	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1.0	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 5.5 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Fig. 8				
		per channel	-	-	±1.0	µA
		all channels	-	-	±8.0	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 5.5 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Fig. 9	-	-	±8.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{IS} = GND or V _{CC} ; V _{OS} = V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V	-	-	160	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V				
		pin E	-	-	294	µA
		pin Sn	-	-	245	µA

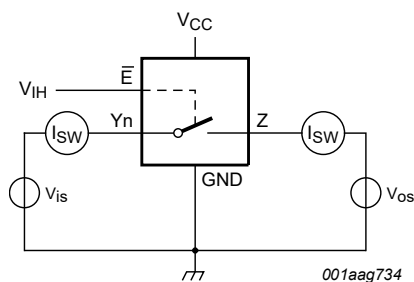
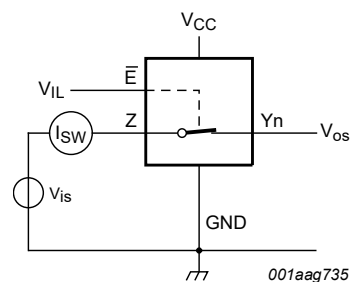

$$\begin{aligned} V_{is} &= V_{CC} \text{ and } V_{os} = \text{GND} \\ V_{is} &= \text{GND} \text{ and } V_{os} = V_{CC} \end{aligned}$$

Fig. 8. Test circuit for measuring OFF-state leakage current



$V_{is} = V_{CC}$ and $V_{os} = \text{open}$
 $V_{is} = \text{GND}$ and $V_{os} = \text{open}$

Fig. 9. Test circuit for measuring ON-state leakage current

11. Dynamic characteristics

Table 9. Dynamic characteristics 74HC4067

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$ unless specified otherwise; for test circuit see Fig. 12.

V_{is} is the input voltage at a Y_n or Z terminal, whichever is assigned as an input.

V_{os} is the output voltage at a Y_n or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
			Typ	Max	Max	Max	
t_{pd}	propagation delay	Y_n to Z ; see Fig. 10 [1][2]					
		$V_{CC} = 2.0\text{ V}$	25	75	95	110	ns
		$V_{CC} = 4.5\text{ V}$	9	15	19	22	ns
		$V_{CC} = 6.0\text{ V}$	7	13	16	19	ns
		$V_{CC} = 9.0\text{ V}$	5	9	11	14	ns
		Z to Y_n					
		$V_{CC} = 2.0\text{ V}$	18	60	75	90	ns
		$V_{CC} = 4.5\text{ V}$	6	12	15	18	ns
		$V_{CC} = 6.0\text{ V}$	5	10	13	15	ns
		$V_{CC} = 9.0\text{ V}$	4	8	10	12	ns
t_{off}	turn-off time	$\bar{E}$ to Y_n ; see Fig. 11 [3]					
		$V_{CC} = 2.0\text{ V}$	74	250	315	375	ns
		$V_{CC} = 4.5\text{ V}$	27	50	63	75	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	27	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	22	43	54	64	ns
		$V_{CC} = 9.0\text{ V}$	20	38	48	57	ns
		S_n to Y_n					
		$V_{CC} = 2.0\text{ V}$	83	250	315	375	ns
		$V_{CC} = 4.5\text{ V}$	30	50	63	75	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	29	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	24	43	54	64	ns
		$V_{CC} = 9.0\text{ V}$	21	38	48	57	ns
		$\bar{E}$ to Z					
		$V_{CC} = 2.0\text{ V}$	85	275	345	415	ns
		$V_{CC} = 4.5\text{ V}$	31	55	69	83	ns
		$V_{CC} = 6.0\text{ V}$	25	47	59	71	ns
		$V_{CC} = 9.0\text{ V}$	24	42	53	63	ns
		S_n to Z					
		$V_{CC} = 2.0\text{ V}$	94	290	365	435	ns
		$V_{CC} = 4.5\text{ V}$	34	58	73	87	ns
		$V_{CC} = 6.0\text{ V}$	27	47	62	74	ns
		$V_{CC} = 9.0\text{ V}$	25	45	56	68	ns

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
			Typ	Max	Max	Max	
t _{on}	turn-on time	$\overline{E}$ to Y _n ; see Fig. 11 [4]					
		V _{CC} = 2.0 V	80	275	345	415	ns
		V _{CC} = 4.5 V	29	55	69	83	ns
		V _{CC} = 5.0 V; C _L = 15 pF	26	-	-	-	ns
		V _{CC} = 6.0 V	23	47	59	71	ns
		V _{CC} = 9.0 V	17	42	53	63	ns
		Sn to Y _n					
		V _{CC} = 2.0 V	88	300	375	450	ns
		V _{CC} = 4.5 V	32	60	75	90	ns
		V _{CC} = 5.0 V; C _L = 15 pF	29	-	-	-	ns
		V _{CC} = 6.0 V	26	51	64	77	ns
		V _{CC} = 9.0 V	18	45	56	68	ns
		$\overline{E}$ to Z					
		V _{CC} = 2.0 V	85	275	345	415	ns
		V _{CC} = 4.5 V	31	55	69	83	ns
		V _{CC} = 6.0 V	25	47	59	71	ns
		V _{CC} = 9.0 V	18	42	53	63	ns
		Sn to Z					
		V _{CC} = 2.0 V	94	300	375	450	ns
		V _{CC} = 4.5 V	34	60	75	90	ns
		V _{CC} = 6.0 V	27	51	64	77	ns
		V _{CC} = 9.0 V	19	45	56	68	ns
C _{PD}	power dissipation capacitance	per switch; V _I = GND to V _{CC} [5]	29	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.
[3] t_{on} is the same as t_{PHZ} and t_{PLZ}.
[4] t_{off} is the same as t_{PZH} and t_{PZL}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
Σ{(C_L + C_{sw}) × V_{CC}² × f_o} = sum of outputs;
C_L = output load capacitance in pF;
C_{sw} = switch capacitance in pF;
V_{CC} = supply voltage in V.

Table 10. Dynamic characteristics 74HCT4067

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$ unless specified otherwise; for test circuit see Fig. 12.

V_{is} is the input voltage at a Y_n or Z terminal, whichever is assigned as an input.

V_{os} is the output voltage at a Y_n or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
			Typ	Max	Max	Max	
t_{pd}	propagation delay	Y_n to Z ; see Fig. 10 [1][2]					
		$V_{CC} = 4.5\text{ V}$	9	15	19	22	ns
		Z to Y_n					
		$V_{CC} = 4.5\text{ V}$	6	12	15	18	ns
t_{off}	turn-off time	$\bar{E}$ to Y_n ; see Fig. 11 [3]					
		$V_{CC} = 4.5\text{ V}$	26	55	69	83	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	26	-	-	-	ns
		S_n to Y_n					
		$V_{CC} = 4.5\text{ V}$	31	55	69	83	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	30	-	-	-	ns
		$\bar{E}$ to Z					
		$V_{CC} = 4.5\text{ V}$	30	60	75	90	ns
		S_n to Z					
		$V_{CC} = 4.5\text{ V}$	35	60	75	90	ns
t_{on}	turn-on time	$\bar{E}$ to Y_n ; see Fig. 11 [4]					
		$V_{CC} = 4.5\text{ V}$	32	60	75	90	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	32	-	-	-	ns
		S_n to Y_n					
		$V_{CC} = 4.5\text{ V}$	35	60	75	90	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	33	-	-	-	ns
		$\bar{E}$ to Z					
		$V_{CC} = 4.5\text{ V}$	38	65	81	98	ns
		S_n to Z					
		$V_{CC} = 4.5\text{ V}$	38	65	81	98	ns
C_{PD}	power dissipation capacitance	per switch; $V_i = GND$ to $(V_{CC} - 1.5\text{ V})$ [5]	29	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2] Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

[3] t_{on} is the same as t_{PHZ} and t_{PLZ} .

[4] t_{off} is the same as t_{PZH} and t_{PZL} .

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

$\sum \{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ = sum of outputs;

C_L = output load capacitance in pF;

C_{sw} = switch capacitance in pF;

V_{CC} = supply voltage in V.

11.1. Waveforms and test circuit

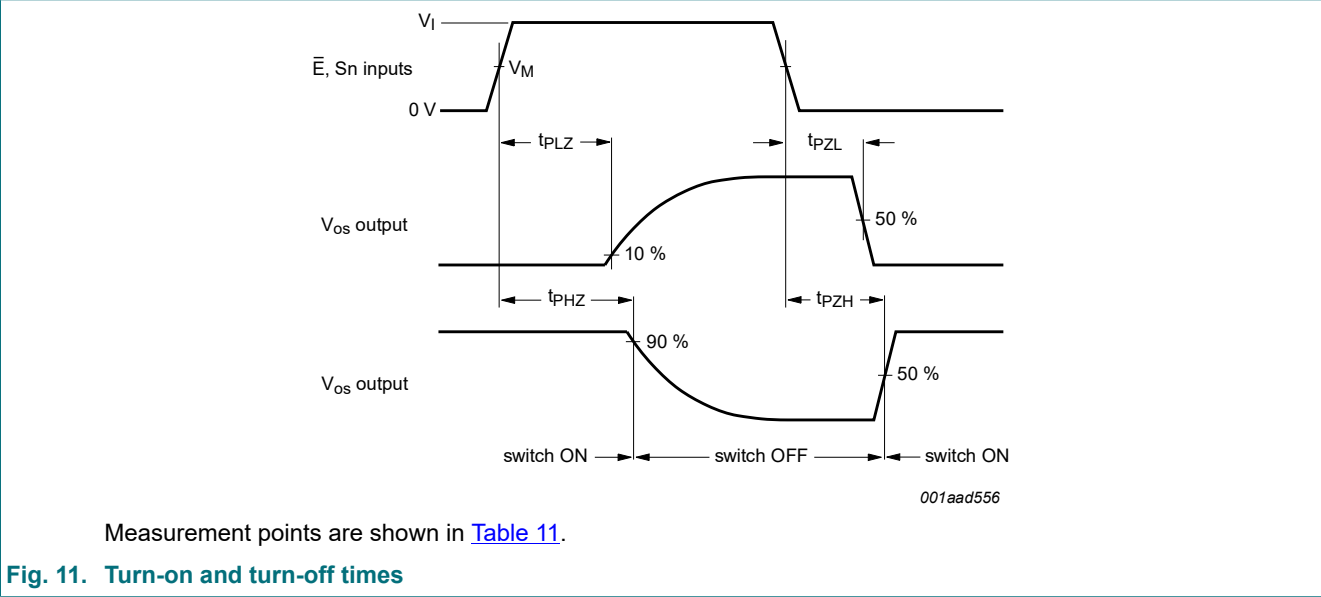
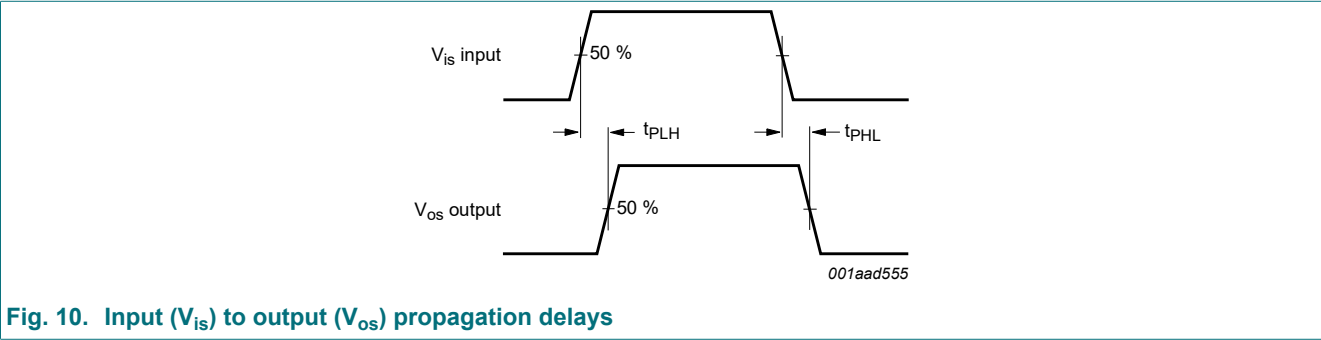


Table 11. Measurement points

Type	V_I	V_M
74HC4067	V_{CC}	$0.5V_{CC}$
74HCT4067	3.0 V	1.3 V

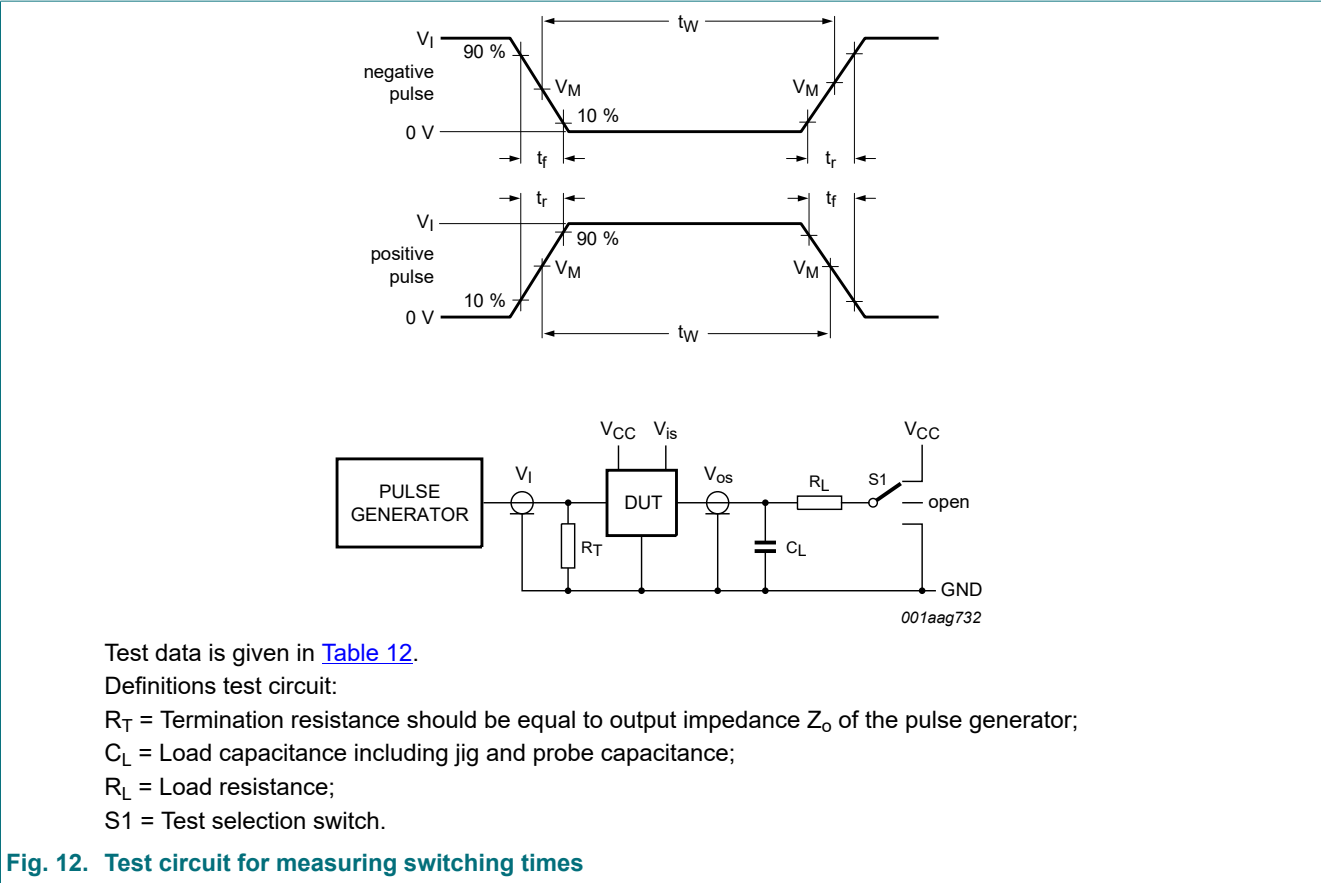


Table 12. Test data

Test	Input				Output		S1 position
	Control E	Address Sn	Switch Yn (Z)	t _r , t _f	Switch Z (Yn)		
	V _I [1]	V _I [1]	V _{is}		C _L	R _L	
t _{PHL} , t _{PLH}	GND	GND or V _{CC}	GND to V _{CC}	6 ns	50 pF	-	open
t _{PHZ} , t _{PZH}	GND to V _{CC}	GND to V _{CC}	V _{CC}	6 ns	50 pF, 15 pF	1 kΩ	GND
t _{PLZ} , t _{PZL}	GND to V _{CC}	GND to V _{CC}	GND	6 ns	50 pF, 15 pF	1 kΩ	V _{CC}

[1] For 74HCT4067: maximum input voltage $V_I = 3.0$ V.

12. Additional dynamic characteristics

Table 13. Additional dynamic characteristics

Recommended conditions and typical values; GND = 0 V.
V_{is} is the input voltage at a Y_n or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Y_n or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	25 °C			Unit
			Min	Typ	Max	
THD	total harmonic distortion	R _L = 10 kΩ; C _L = 50 pF; see Fig. 13				
		f _i = 1 kHz				
		V _{CC} = 4.5 V; V _{is(p-p)} = 4.0 V	-	0.04	-	%
		V _{CC} = 9.0 V; V _{is(p-p)} = 8.0 V	-	0.02	-	%
		f _i = 10 kHz				
		V _{CC} = 4.5 V; V _{is(p-p)} = 4.0 V	-	0.12	-	%
α _{iso}	isolation (OFF-state)	R _L = 600 Ω; C _L = 50 pF; see Fig. 14 [1]				
		V _{CC} = 4.5 V	-	-50	-	dB
		V _{CC} = 9.0 V	-	-50	-	dB
f _(-3dB)	-3 dB frequency response	R _L = 50 Ω; C _L = 10 pF; see Fig. 15 [2]				
		V _{CC} = 4.5 V	-	90	-	MHz
		V _{CC} = 9.0 V	-	100	-	MHz
C _{sw}	switch capacitance	independent pins Y	-	5	-	pF
		common pin Z	-	45	-	pF

- [1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
[2] Adjust input voltage V_{is} to 0 dBm level at V_{os} for f_i = 1 MHz (0 dBm = 1 mW into 50 Ω). After set-up, f_i is increased to obtain a reading of -3 dB at V_{os}.

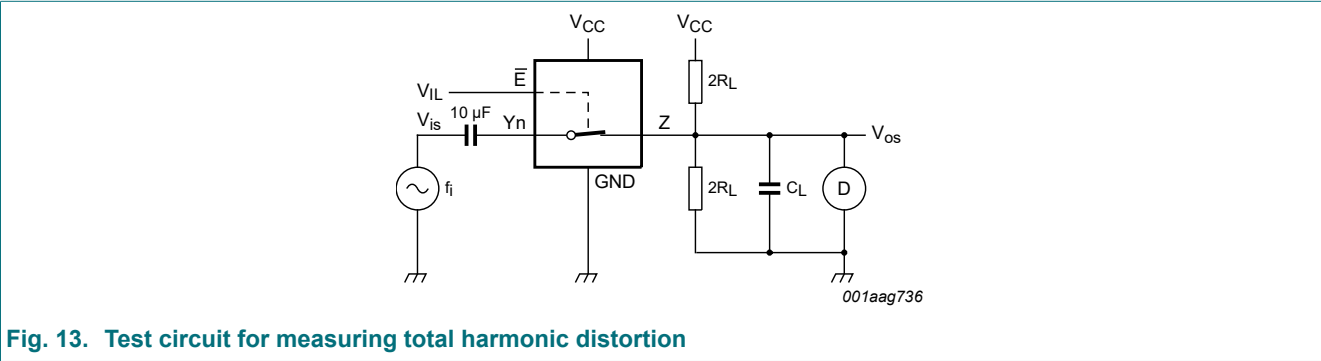
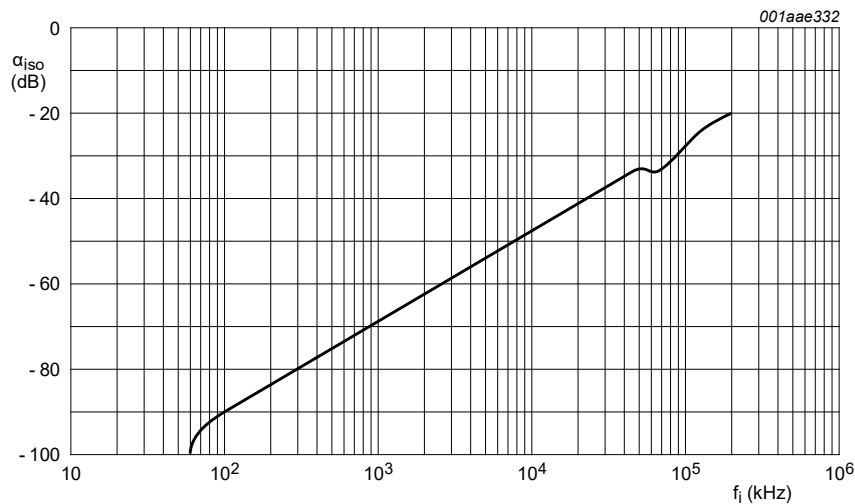
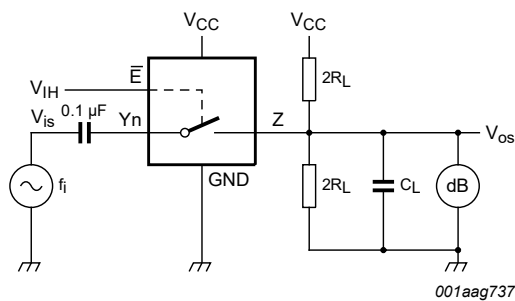


Fig. 13. Test circuit for measuring total harmonic distortion



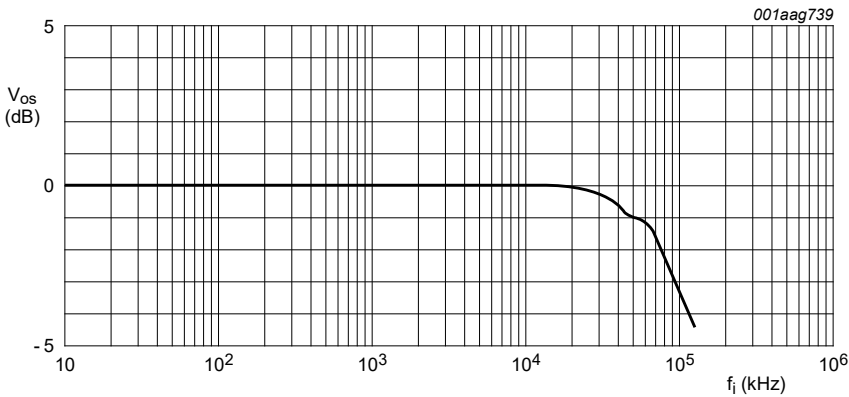
a. Isolation (OFF-state)



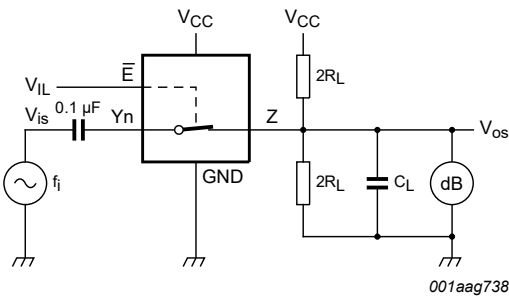
b. Test circuit

$V_{CC} = 4.5\text{ V}$; $GND = 0\text{ V}$; $R_L = 600\text{ }\Omega$; $R_{source} = 1\text{ k}\Omega$.

Fig. 14. Isolation (OFF-state) as a function of frequency



a. Typical -3 dB frequency response



b. Test circuit

$V_{CC} = 4.5\text{ V}$; $GND = 0\text{ V}$; $R_L = 50\text{ }\Omega$; $R_{source} = 1\text{ k}\Omega$.

Fig. 15. -3 dB frequency response

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

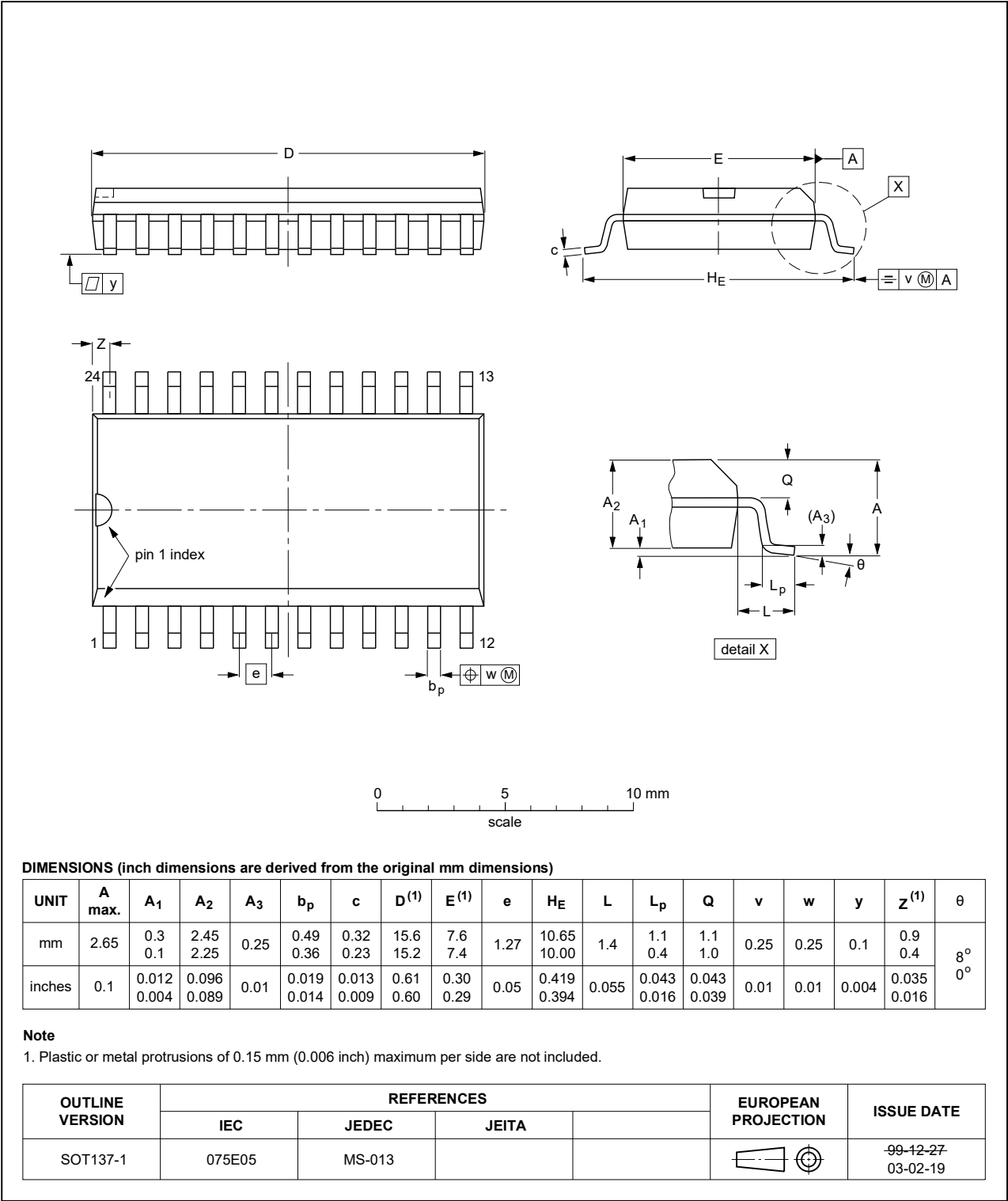


Fig. 16. Package outline SOT137-1 (SO24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

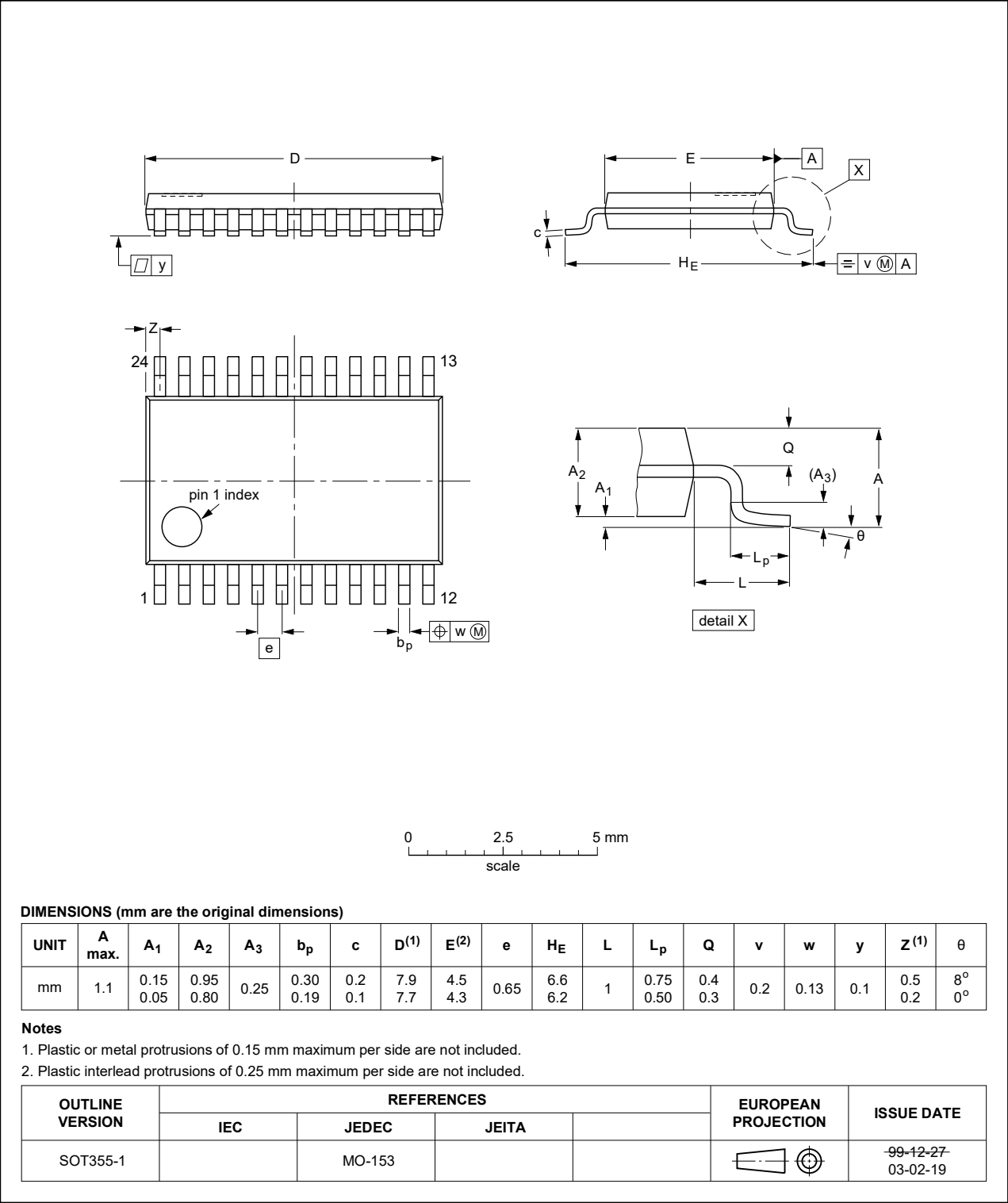


Fig. 17. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package;
no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

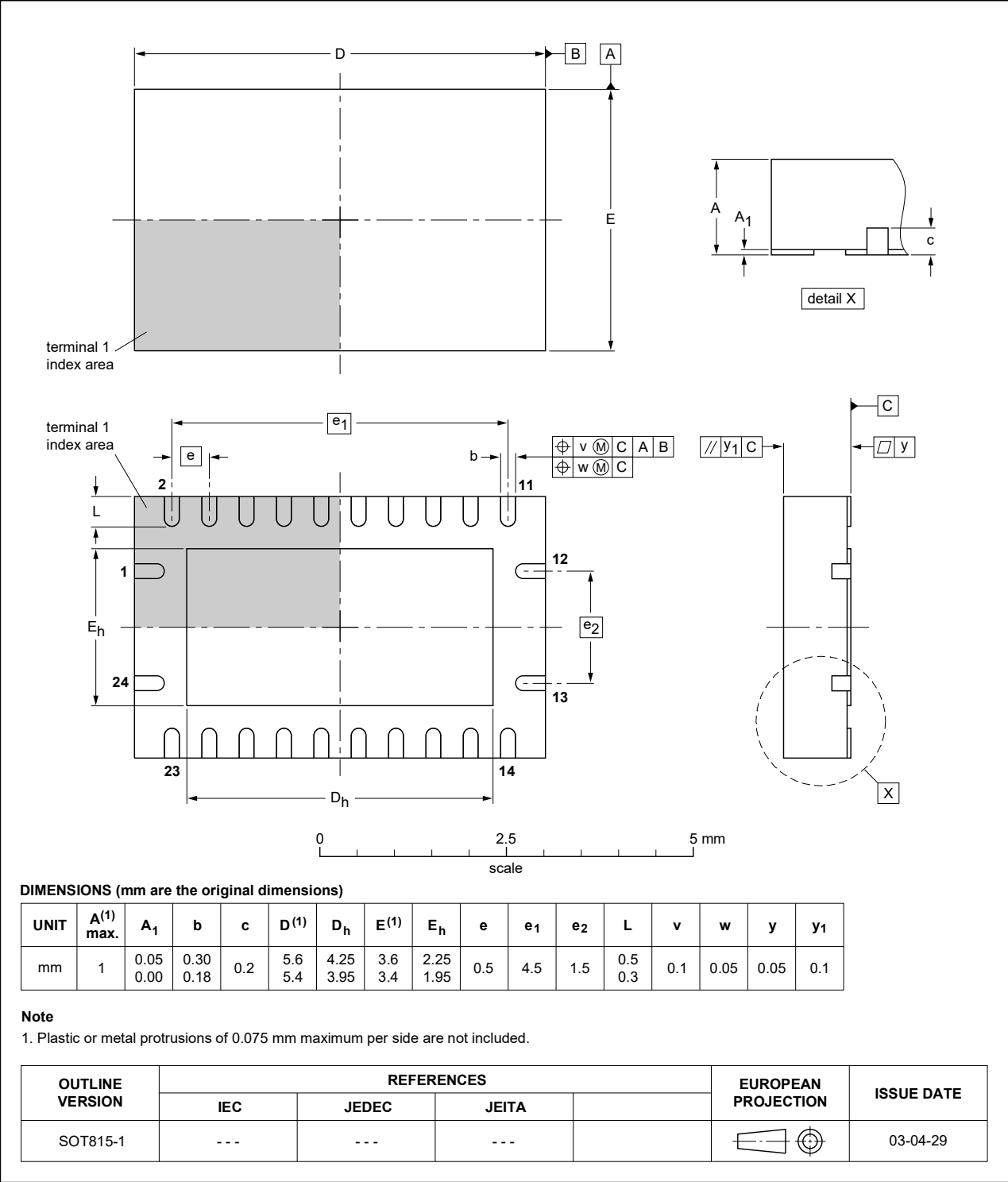


Fig. 18. Package outline SOT815-1 (DHVQFN24)

14. Abbreviations

Table 14. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

15. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4067 v.10	20240725	Product data sheet	-	74HC_HCT4067 v.9
Modifications:	Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT4067 v.9	20240429	Product data sheet	-	74HC_HCT4067 v.8
Modifications:	Type number 74HCT4067D (SOT137-1/SO24) removed.			
74HC_HCT4067 v.8	20210909	Product data sheet	-	74HC_HCT4067 v.7
Modifications:	Type numbers 74HC4067DB and 74HCT4067DB (SOT340-1/SSOP24) removed.			
74HC_HCT4067 v.7	20200602	Product data sheet	-	74HC_HCT4067 v.6
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation have been updated.			
74HC_HCT4067 v.6	20150522	Product data sheet	-	74HC_HCT4067 v.5
Modifications:	- Type numbers 74HC4067N and 74HCT4067N (SOT101-1) removed. Fig. 6, Fig. 7: Figure note V_{is} = 0 V to (V_{CC}-GND) changed to V_{is} = 0 V to V_{CC}			
74HC_HCT4067 v.5	20111213	Product data sheet	-	74HC_HCT4067 v.4
Modifications:	Legal pages updated.			
74HC_HCT4067 v.4	20110518	Product data sheet	-	74HC_HCT4067 v.3
74HC_HCT4067 v.3	20071015	Product data sheet	-	74HC_HCT4067_CNV v.2
74HC_HCT4067_CNV v.2	19970901	Product specification	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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