LM3478Q-Q1 High-Efficiency Controller for Boost, SEPIC and Flyback DC-DC Converters

1 Features

- LM3478Q-Q1 is AEC-Q100 qualified and manufactured on an automotive grade flow
- 8-lead VSSOP-8
- Internal push-pull driver with 1A peak current capability
- Current limit and thermal shutdown
- Frequency compensation optimized with a capacitor and a resistor
- Internal soft start
- Current mode operation
- Undervoltage lockout with hysteresis
- Key specifications:
  - Wide supply voltage range of 2.97V to 40V
  - 100kHz to 1MHz adjustable clock frequency
  - ±2.5% (overtemperature) internal reference
  - 10µA shutdown current (overtemperature)
- Create a custom design using the LM3478Q-Q1 with the WEBENCH Power Designer

2 Applications

- Isolated supply (flyback) in traction inverters and On-board chargers
- ADAS - Driver monitoring
- Digital cockpit and head unit

3 Description

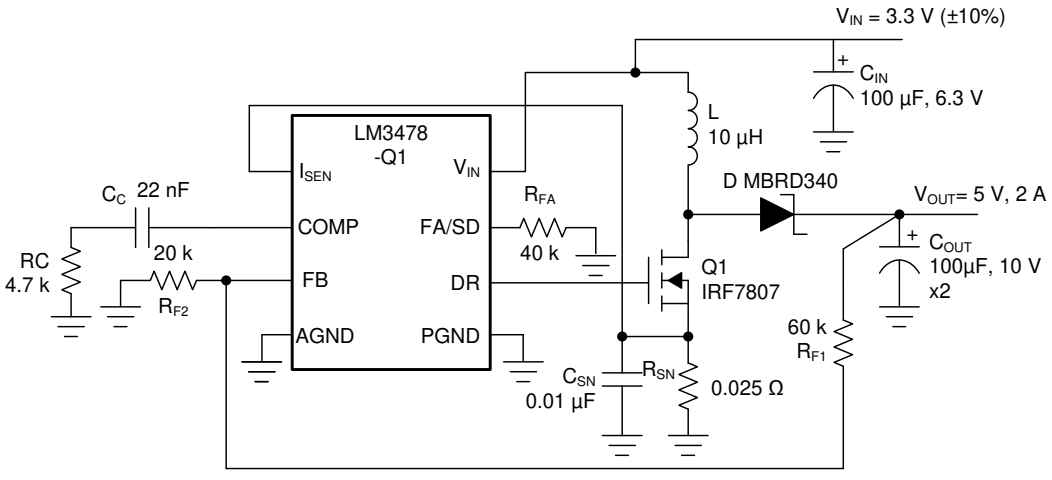
The LM3478Q-Q1 is a versatile Low-Side N-Channel MOSFET controller for switching regulators. It is suitable for use in topologies requiring a low side MOSFET, such as boost, flyback, SEPIC, etc. Moreover, the LM3478Q-Q1 can be operated at extremely high switching frequency in order to reduce the overall solution size. The switching frequency of the LM3478Q-Q1 can be adjusted to any value between 100kHz and 1MHz by using a single external resistor. Current mode control provides superior bandwidth and transient response, besides cycle-by-cycle current limiting. Output current can be programmed with a single external resistor.

The LM3478Q-Q1 has built in features such as thermal shutdown, short-circuit protection, over voltage protection, etc. Power saving shutdown mode reduces the total supply current to 5µA and allows power supply sequencing. Internal soft-start limits the inrush current at start-up.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LM3478Q-Q1	VSSOP (8)	3.00mm x 3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical High Efficiency Step-Up (Boost) Converter

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4 Pin Configuration and Functions

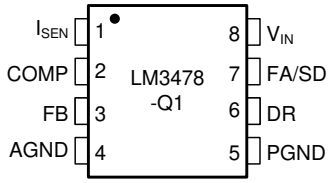


Figure 4-1. LM3478-Q1 DGK Package, VSSOP-8 (Top View)

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
I_{SEN}	1	I	Current sense input pin. Voltage generated across an external sense resistor is fed into this pin.
COMP	2	I	Compensation pin. A resistor, capacitor combination connected to this pin provides compensation for the control loop.
FB	3	I	Feedback pin. The output voltage should be adjusted using a resistor divider to provide 1.26V at this pin.
AGND	4	G	Analog ground pin.
PGND	5	G	Power ground pin.
DR	6	O	Drive pin. The gate of the external MOSFET should be connected to this pin.
FA/SD	7	I	Frequency adjust and Shutdown pin. A resistor connected to this pin sets the oscillator frequency. A high level on this pin for longer than 30µs will turn the device off. The device will then draw less than 10µA from the supply.
V_{IN}	8	P	Power Supply Input pin.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input Voltage			45	V
FB Pin Voltage		–0.4< V	V_{FB} < 7	V
FA/SD Pin Voltage		–0.4 < $V_{FA/SD}$	$V_{FA/SD}$< 7	V
Peak Driver Output Current (<10µs)			1	A
Power Dissipation		Internally Limited		
Junction Temperature			+150	°C
Lead Temperature	Vapor Phase (60 s)		215	°C
	Infrared (15 s)		260	°C
DR Pin Voltage		–0.4 ≤ VDR	VDR ≤ 8	V
I_{SEN} Pin Voltage			500	mV
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	Other pins	±750	
			Corner pins (1, 4, 5, and 8)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage	2.97 ≤ V_{IN}		V_{IN} ≤ 40	V
Junction Temperature Range	−40 ≤ T_J		T_J ≤ +125	°C
Switching Frequency	100 ≤ F_{SW}		F_{SW} ≤ 1000	kHz

5.4 Thermal Information

THERMAL METRIC(1)		LM3478Q-Q1 DGK 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

Unless otherwise specified, V_{IN} = 12V, R_{FA} = 40kΩ, T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback Voltage	V_{COMP} = 1.4V, 2.97 ≤ V_{IN} ≤ 40V	1.2416	1.26	1.2843	V
		V_{COMP} = 1.4V, 2.97 ≤ V_{IN} ≤ 40V, −40°C ≤ T_J ≤ 125°C	1.228		1.292	
ΔV_{LINE}	Feedback Voltage Line Regulation	2.97 ≤ V_{IN} ≤ 40V		0.001		%/V
ΔV_{LOAD}	Output Voltage Load Regulation	I_{EAO} Source/Sink			±0.5	%/A
V_{UVLO}	Input Undervoltage Lock-out			2.85		V
		−40°C ≤ T_J ≤ 125°C			2.97	
$V_{UV(HYS)}$	Input Undervoltage Lock-out Hysteresis			170		mV
		−40°C ≤ T_J ≤ 125°C	130		210	
F_{nom}	Nominal Switching Frequency	R_{FA} = 40KΩ		400		kHz
		R_{FA} = 40KΩ, −40°C ≤ T_J ≤ 125°C	350		440	
$R_{DS1\ (ON)}$	Driver Switch On Resistance (top)	I_{DR} = 0.2A, V_{IN}= 5V		16		Ω
$R_{DS2\ (ON)}$	Driver Switch On Resistance (bottom)	I_{DR} = 0.2A		4.5		
$V_{DR\ (max)}$	Maximum Drive Voltage Swing[1]	V_{IN} < 7.2V		V_{IN}		V
		V_{IN} ≥ 7.2V		7.2		
D_{max}	Maximum Duty Cycle[2]			100%		
T_{min} (on)	Minimum On Time			325		ns
		−40°C ≤ T_J ≤ 125°C	210		600	
I_{SUPPLY}	Supply Current (non-switching)	See [3]		2.7		mA
		See [3], −40°C ≤ T_J ≤ 125°C			3.3	
I_Q	Quiescent Current in Shutdown Mode	$V_{FA/SD}$ = 5V [4], V_{IN} = 5V		5		μA
		$V_{FA/SD}$ = 5V [4], V_{IN} = 5V, −40°C ≤ T_J ≤ 125°C			10	
V_{SENSE}	Current Sense Threshold Voltage	V_{IN} = 5V	135	156	180	mV
		V_{IN} = 5V, −40°C ≤ T_J ≤ 125°C	125		190	
V_{SC}	Short-Circuit Current Limit Sense Voltage	V_{IN} = 5V		343		mV
		V_{IN} = 5V, −40°C ≤ T_J ≤ 125°C	250		415	
V_{SL}	Internal Compensation Ramp Voltage	V_{IN} = 5V		92		mV
		V_{IN} = 5V, −40°C ≤ T_J ≤ 125°C	52		132	
V_{SL} ratio	V_{SL}/V_{SENSE}		0.30	0.49	0.70	
V_{OVP}	Output Over-voltage Protection (with respect to feedback voltage) [5]	V_{COMP} = 1.4V	32	50		mV
		V_{COMP} = 1.4V, −40°C ≤ T_J ≤ 125°C	25			
		VSSOP Package			78	
		VSSOP Package, −40°C ≤ T_J ≤ 125°C			85	
$V_{OVP(HYS)}$	Output Over-Voltage Protection Hysteresis[5]	V_{COMP} = 1.4V		60		mV
		V_{COMP} = 1.4V, −40°C ≤ T_J ≤ 125°C	20		110	
Gm	Error Amplifier Transconductance	V_{COMP} = 1.4V, I_{EAO} = 100μA (Source/Sink)	600	800	1000	μS
		V_{COMP} = 1.4V, I_{EAO} = 100μA (Source/Sink), −40°C ≤ T_J ≤ 125°C	365		1265	
A_{VOL}	Error Amplifier Voltage Gain	V_{COMP} = 1.4V, I_{EAO} = 100μA (Source/Sink)		38		V/V
		V_{COMP} = 1.4V, I_{EAO} = 100μA (Source/Sink), −40°C ≤ T_J ≤ 125°C	26		44	
I_{EAO}	Error Amplifier Output Current (Source/ Sink)	Source, V_{COMP} = 1.4V, V_{FB} = 0V	80	110	170	μA
		Source, V_{COMP} = 1.4V, V_{FB} = 0V, −40°C ≤ T_J ≤ 125°C	50		220	
		Sink, V_{COMP} = 1.4V, V_{FB} = 1.4V	−70	−140	−180	μA
		Sink, V_{COMP} = 1.4V, V_{FB} = 1.4V, −40°C ≤ T_J ≤ 125°C	−60		−185	

5.5 Electrical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12V, R_{FA} = 40kΩ, T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{EAO}	Error Amplifier Output Voltage Swing	Upper Limit, V_{FB} = 0V, COMP Pin = Floating		2.2		V
		Upper Limit, V_{FB} = 0V, COMP Pin = Floating, −40°C ≤ T_J ≤ 125°C	1.8		2.4	
		Lower Limit, V_{FB} = 1.4V		0.56		V
		Lower Limit, V_{FB} = 1.4V, −40°C ≤ T_J ≤ 125°C	0.2		1.0	
T_{SS}	Internal Soft-Start Delay	V_{FB} = 1.2V, V_{COMP} = Floating		4		ms
T_r	Drive Pin Rise Time	Cgs = 3000pf, V_{DR} = 0 to 3V		25		ns
T_f	Drive Pin Fall Time	Cgs = 3000pf, V_{DR} = 0 to 3V		25		ns
V_{SD}	Shutdown threshold (6)	Output = High		1.27		V
		Output = High, −40°C ≤ T_J ≤ 125°C			1.4	
		Output = Low		0.65		V
		Output = Low, −40°C ≤ T_J ≤ 125°C	0.3			
I_{SD}	Shutdown Pin Current	V_{SD} = 5V		−1		µA
		V_{SD} = 0V		+1		
I_{FB}	Feedback Pin Current			15		nA
T_{SD}	Thermal Shutdown			165		°C
T_{sh}	Thermal Shutdown Hysteresis			10		°C

(1) The voltage on the drive pin, V_{DR} is equal to the input voltage when input voltage is less than 7.2 V. V_{DR} is equal to 7.2 V when the input voltage is greater than or equal to 7.2 V.
(2) The limits for the maximum duty cycle can not be specified since the part does not permit less than 100% maximum duty cycle operation.
(3) For this test, the FA/SD pin is pulled to ground using a 40-K resistor.
(4) For this test, the FA/SD pin is pulled to 5 V using a 40-K resistor.
(5) The over-voltage protection is specified with respect to the feedback voltage. This is because the over-voltage protection tracks the feedback voltage. The overvoltage protection threshold is given by adding the feedback voltage, V_{FB} to the over-voltage protection specification.
(6) The FA/SD pin should be pulled to V_{IN} through a resistor to turn the regulator off. The voltage on the FA/SD pin must be above the maximum limit for Output = High to keep the regulator off and must be below the limit for Output = Low to keep the regulator on.

5.6 Typical Characteristics

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

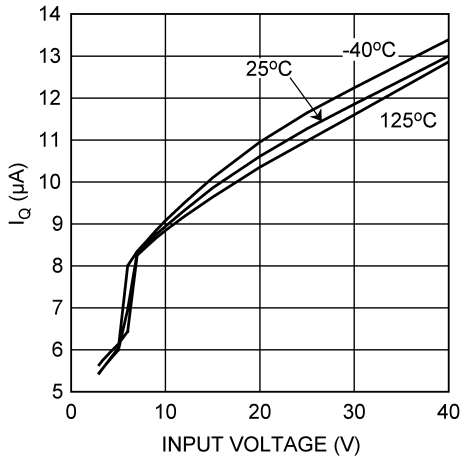


Figure 5-1. I_Q vs Input Voltage (Shutdown)

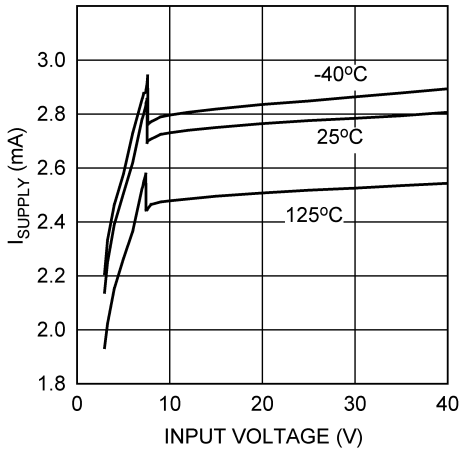


Figure 5-2. I_{Supply} vs Input Voltage (Non-Switching)

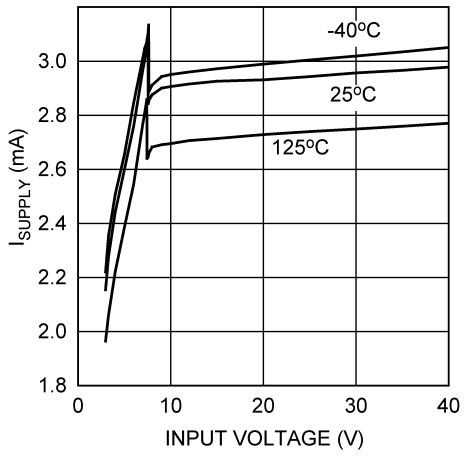


Figure 5-3. I_{Supply} vs V_{IN} (Switching)

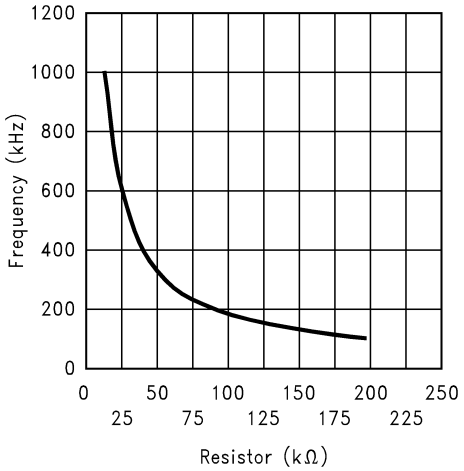


Figure 5-4. Switching Frequency vs R_{FA}

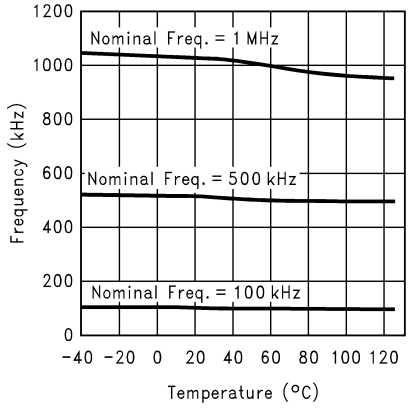


Figure 5-5. Frequency vs Temperature

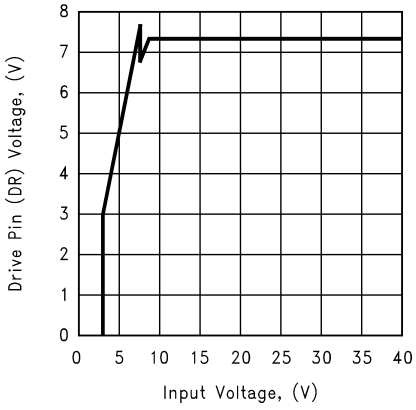


Figure 5-6. Drive Voltage vs Input Voltage

5.6 Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

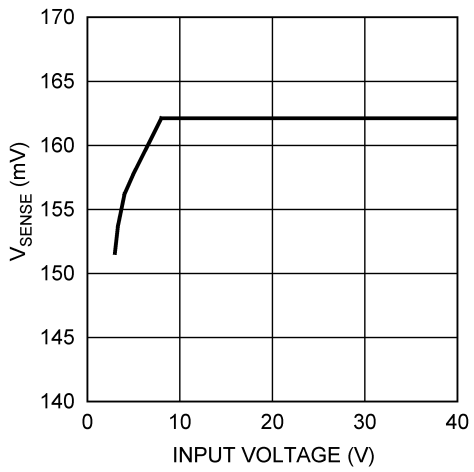


Figure 5-7. Current Sense Threshold vs Input Voltage

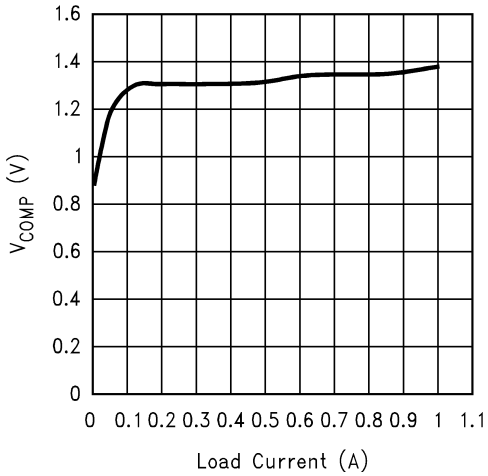


Figure 5-8. COMP Pin Voltage vs Load Current

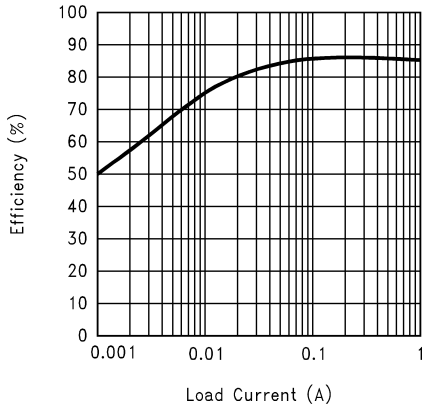


Figure 5-9. Efficiency vs Load Current (3.3-V Input and 12-V Output)

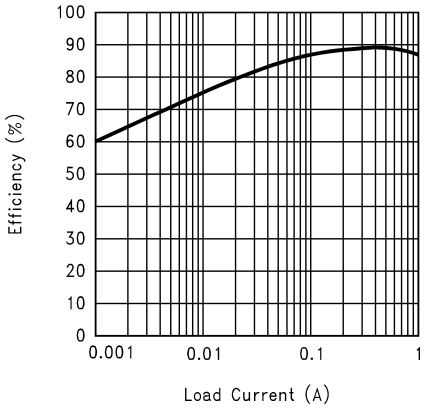


Figure 5-10. Efficiency vs Load Current (5-V Input and 12-V Output)

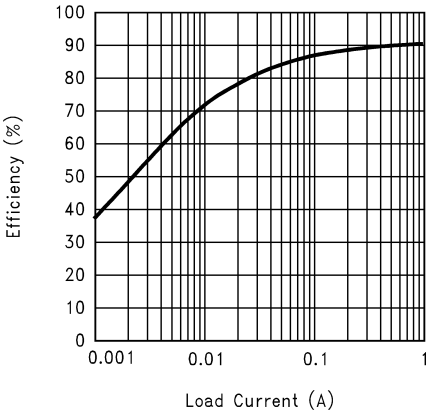


Figure 5-11. Efficiency vs Load Current (9-V Input and 12-V Output)

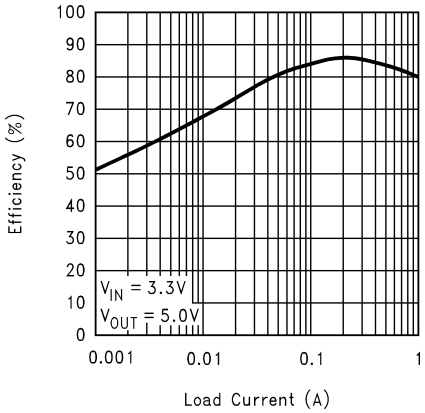


Figure 5-12. Efficiency vs Load Current (3.3-V Input and 5-V Output)

5.6 Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

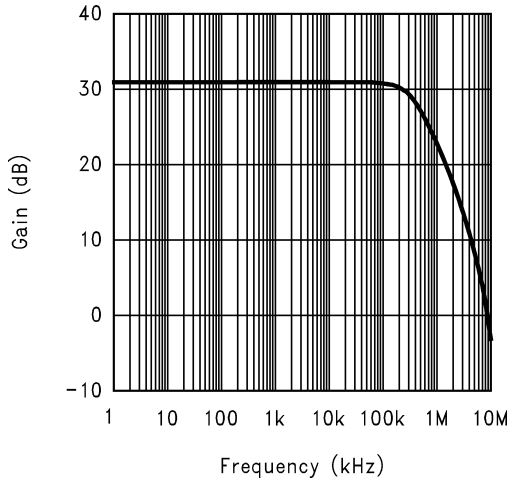


Figure 5-13. Error Amplifier Gain

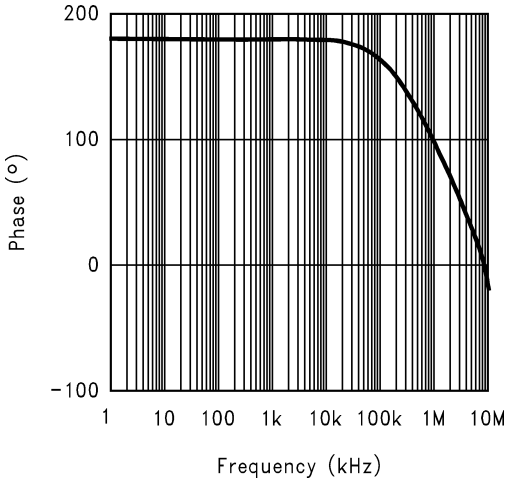


Figure 5-14. Error Amplifier Phase

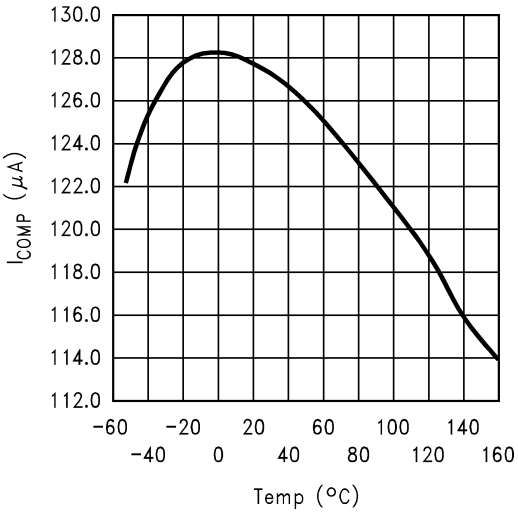


Figure 5-15. COMP Pin Source Current vs Temperature

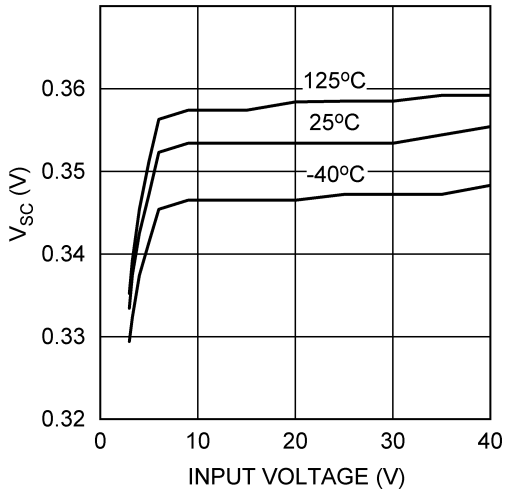


Figure 5-16. Short Circuit Sense Voltage vs Input Voltage

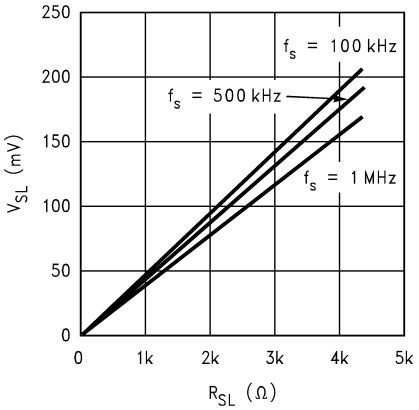


Figure 5-17. Compensation Ramp vs Compensation Resistor

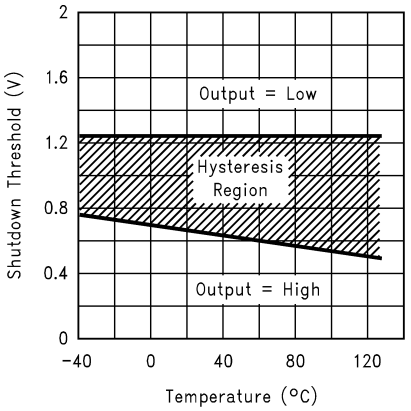


Figure 5-18. Shutdown Threshold Hysteresis vs Temperature

5.6 Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

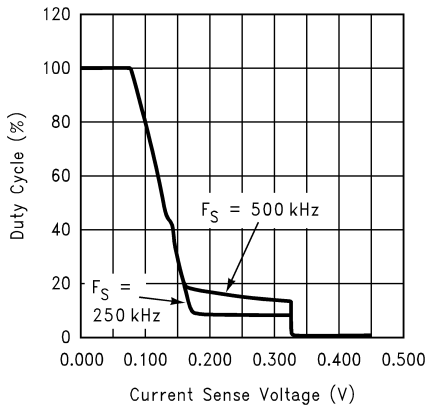


Figure 5-19. Duty Cycle vs Current Sense Voltage

6 Detailed Description

6.1 Overview

TheLM3478Q-Q1 device uses a fixed frequency, Pulse Width Modulated (PWM) current mode control architecture. The *Section 6.2* shows the basic functionality. In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the I_{SEN} pin. This voltage is fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input (feedback pin, FB). The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator. At the start of any switching cycle, the oscillator sets the RS latch using the switch logic block. This forces a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off.

The voltage sensed across the sense resistor generally contains spurious noise spikes, as shown in Figure 6-1. These spikes can force the PWM comparator to reset the RS latch prematurely. To prevent these spikes from resetting the latch, a blank-out circuit inside the IC prevents the PWM comparator from resetting the latch for a short duration after the latch is set. This duration is about 325ns and is called the blanking interval and is specified as minimum on-time in the Electrical Characteristics section. Under extremely light-load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET in on during the blanking interval is more than what is delivered to the load. An over-voltage comparator inside theLM3478Q-Q1 prevents the output voltage from rising under these conditions. The over-voltage comparator senses the feedback (FB pin) voltage and resets the RS latch. The latch remains in reset state until the output decays to the nominal value.

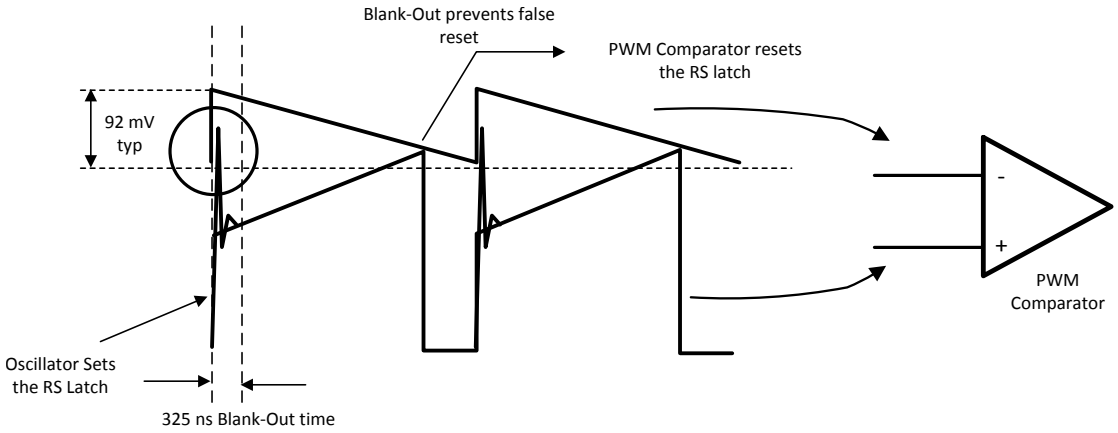
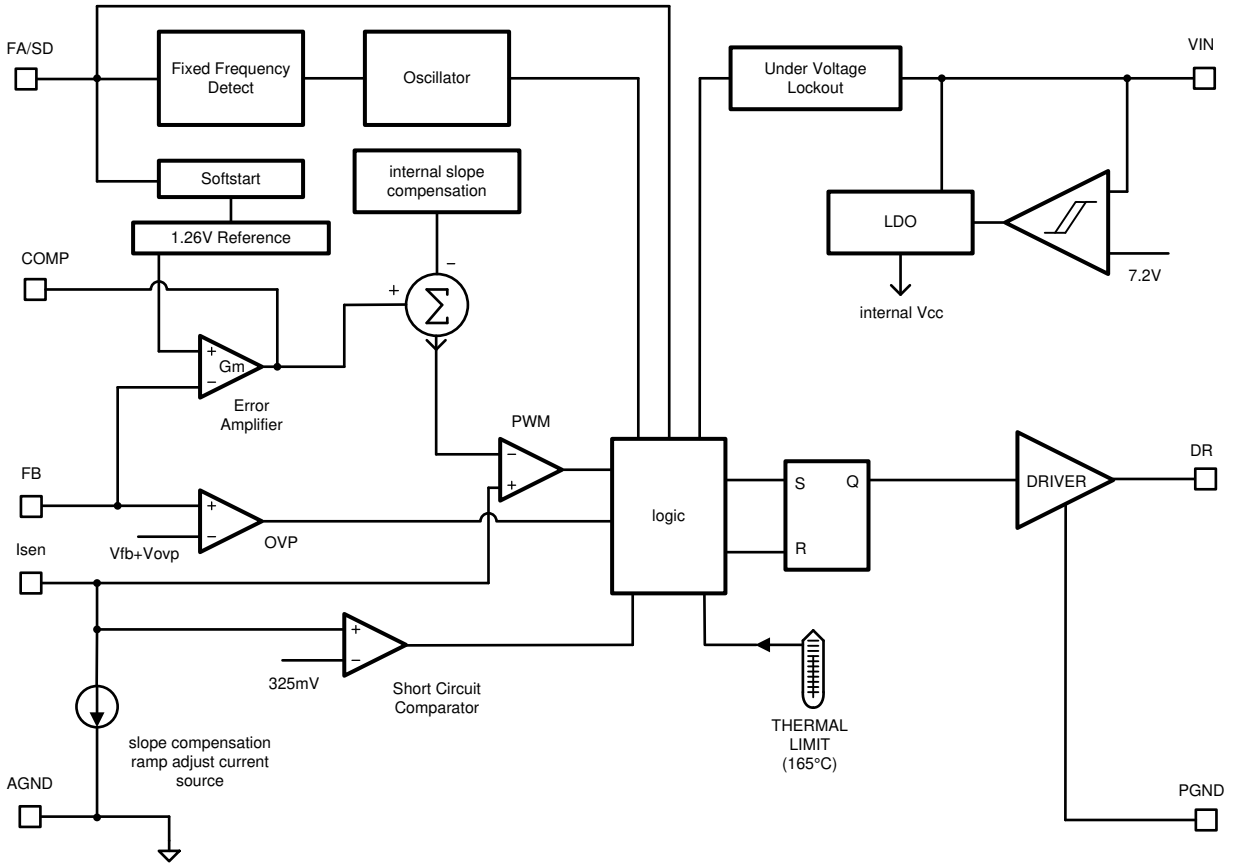


Figure 6-1. Basic Operation of the PWM Comparator

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Overvoltage Protection

The LM3478Q-Q1 has over voltage protection (OVP) for the output voltage. OVP is sensed at the feedback pin (pin 3). If at anytime the voltage at the feedback pin rises to V_{FB}+ V_{OVP}, OVP is triggered. See *Section 5.5* section for limits on V_{FB} and V_{OVP}.

OVP will cause the drive pin to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. TheLM3478Q-Q1 begins switching again when the feedback voltage reaches V_{FB} + (V_{OVP} - $V_{OVP(HYS)}$). See *Section 5.5* for limits on $V_{OVP(HYS)}$.

OVP can be triggered if the unregulated input voltage crosses 7.2 V, the output voltage will react as shown in Figure 6-2. The internal bias of the LM3478Q-Q1 comes from either the internal LDO as shown in the block diagram or the voltage at the Vin pin is used directly. At Vin voltages lower than 7.2 V the internal IC bias is the Vin voltage and at voltages above 7.2V the internal LDO of the LM3478Q-Q1 provides the bias. At the switch over threshold at 7.2 V a sudden small change in bias voltage is seen by all the internal blocks of the LM3478Q-Q1. The control voltage shifts because of the bias change, the PWM comparator tries to keep regulation. To the PWM comparator, the scenario is identical to a step change in the load current, so the response at the output voltage is the same as would be observed in a step load change. Hence, the output voltage overshoot here can also trigger OVP. The LM3478Q-Q1 will regulate in hysteretic mode for several cycles, or may not recover and simply stay in hysteretic mode until the load current drops or Vin is not crossing the 7.2 V threshold anymore. Note that the output is still regulated in hysteretic mode.

Depending on the requirements of the application, there is some influence one has over this effect. The threshold of 7.2 V can be shifted to higher voltages by adding a resistor in series with V_{IN}. In case V_{IN} is

right at the threshold of 7.2 V, the threshold could cross over and over due to some slight ripple on V_{IN}. To minimize the effect on the output voltage one can filter the V_{IN} pin with an RC filter.

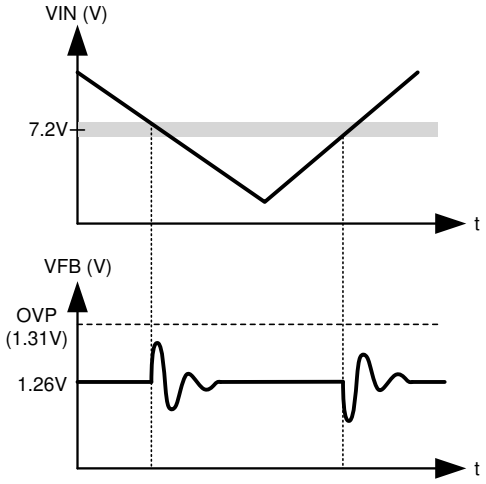


Figure 6-2. The Feedback Voltage Experiences an Oscillation if the Input Voltage crosses the 7.2-V Internal Bias Threshold

6.3.2 Slope Compensation Ramp

The LM3478Q-Q1 uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch and simpler control loop characteristics. It is also easy to parallel power stages using current mode control since current sharing is automatic. However, current mode control has an inherent instability for duty cycles greater than 50%, as shown in Figure 6-3.

A small increase in the load current causes the switch current to increase by ΔI_0. The effect of this load change is ΔI_1.

The two solid waveforms shown are the waveforms compared at the internal pulse width modulator, used to generate the MOSFET drive signal. The top waveform with the slope S_e is the internally generated control waveform V_C. The bottom waveform with slopes S_n and S_f is the sensed inductor current waveform V_{SEN}.

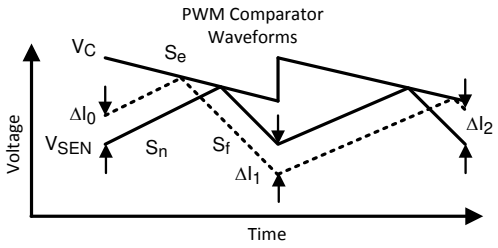


Figure 6-3. Sub-Harmonic Oscillation for D>0.5 and Compensation Ramp to Avoid Sub-Harmonic Oscillation

Sub-harmonic Oscillation can be easily understood as a geometric problem. If the control signal does not have slope, the slope representing the inductor current ramps up until the control signal is reached and then slopes down again. If the duty cycle is above 50%, any perturbation will not converge but diverge from cycle to cycle and causes sub-harmonic oscillation.

It is apparent that the difference in the inductor current from one cycle to the next is a function of S_n, S_f and S_e as shown in Equation 1.

$$\Delta I_n = \frac{S_f - S_e}{S_n + S_e} \Delta I_{n-1} \quad (1)$$

Hence, if the quantity $(S_f - S_e)/(S_n + S_e)$ is greater than 1, the inductor current diverges and sub-harmonic oscillation results. This counts for all current mode topologies. The LM3478Q-Q1 has some internal slope compensation V_{SL} which is enough for many applications above 50% duty cycle to avoid sub-harmonic oscillation .

For boost applications, the slopes S_e, S_f and S_n can be calculated with Equation 2, Equation 3, and Equation 4.

$$S_e = V_{SL} \times f_s \quad (2)$$

$$S_f = R_{sen} \times (V_{OUT} - V_{IN})/L \quad (3)$$

$$S_n = V_{IN} \times R_{sen}/L \quad (4)$$

When S_e increases, then the factor that determines if sub-harmonic oscillation will occur decreases. When the duty cycle is greater than 50%, and the inductance becomes less, the factor increases.

For more flexibility, slope compensation can be increased by adding one external resistor, R_{SL}, in the I_{SEN}'s path. Figure 6-4 shows the setup. The externally generated slope compensation is then added to the internal slope compensation of the LM3478Q-Q1. When using external slope compensation, the formula for S_e becomes:

$$S_e = (V_{SL} + (K \times R_{SL})) \times f_s \quad (5)$$

A typical value for factor K is 40 µA.

The factor changes with switching frequency. Figure 6-5 is used to determine the factor K for individual applications and Equation 6 gives the factor K.

$$K = \Delta V_{SL} / R_{SL} \quad (6)$$

It is a good design practice to only add as much slope compensation as needed to avoid sub-harmonic oscillation. Additional slope compensation minimizes the influence of the sensed current in the control loop. With very large slope compensation the control loop characteristics are similar to a voltage mode regulator which compares the error voltage to a saw tooth waveform rather than the inductor current.

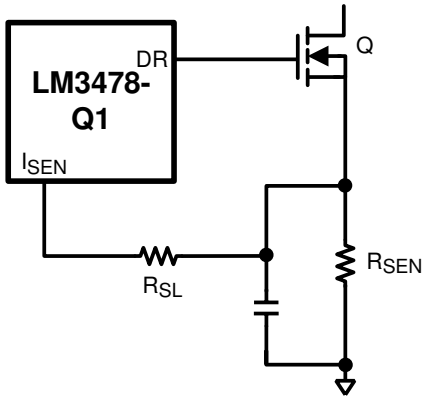


Figure 6-4. Adding External Slope Compensation

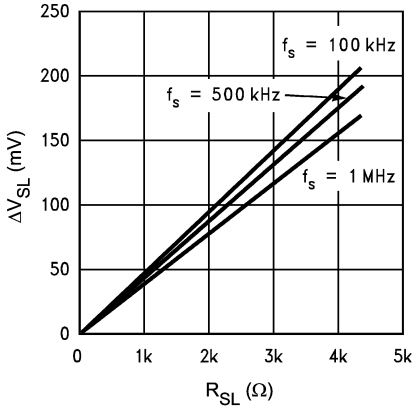


Figure 6-5. External Slope Compensation ΔV_{SL} vs R_{SL}

6.3.3 Frequency Adjust/Shutdown

The switching frequency of the LM3478Q-Q1 can be adjusted between 100 kHz and 1 MHz using a single external resistor. This resistor must be connected between FA/SD pin and ground, as shown in Figure 6-6. To determine the value of the resistor required for a desired switching frequency, refer to *Section 5.6* or use Equation 7:

$$R_{FA} = 4.503 \times 10^{11} \times f_S^{-1.26} \quad (7)$$

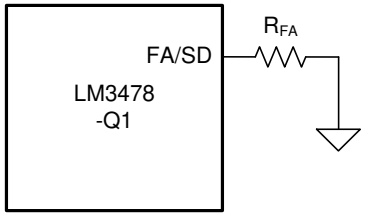


Figure 6-6. Frequency Adjust

The FA/SD pin also functions as a shutdown pin. If a high signal (>1.35 V) appears on the FA/SD pin, the LM3478Q-Q1 stops switching and goes into a low current mode. The total supply current of the IC reduces to less than 10 µA under these conditions. Figure 6-7 shows implementation of the shutdown function when operating in frequency adjust mode. In this mode a high signal for more than 30 us shuts down the IC. However, the voltage on the FA/SD pin should be always less than the absolute maximum of 7 V to avoid any damage to the device.

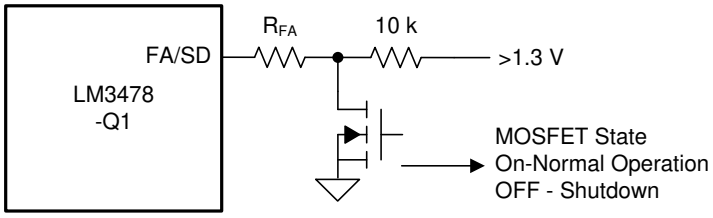


Figure 6-7. Shutdown Operation in Frequency Adjust Mode

6.3.4 Short-Circuit Protection

When the voltage across the sense resistor measured on the I_{SEN} pin exceeds 343 mV, short circuit current limit protection gets activated. A comparator inside the LM3478Q-Q1 reduces the switching frequency by a factor of 5 and maintains this condition until the short is removed. In normal operation the sensed current will trigger the power MOSFET to turn off. During the blanking interval the PWM comparator will not react to an over current so that this additional 343 mV current limit threshold is implemented to protect the device in a short circuit or severe overload condition.

6.4 Device Functional Modes

The device is set to run as soon as the input voltage crosses above the UVLO set point and at a frequency set according to the FA/SD pin pull-down resistor. If the FA/SD pin is pulled high, the LM3478Q-Q1 enters shut-down mode.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The LM3478Q-Q1 may be operated in either the continuous conduction mode (CCM) or the discontinuous current conduction mode (DCM). The following applications are designed for the CCM operation. This mode of operation has higher efficiency and usually lower EMI characteristics than the DCM.

7.2 Typical Applications

7.2.1 Typical High Efficiency Step-Up (Boost) Converter

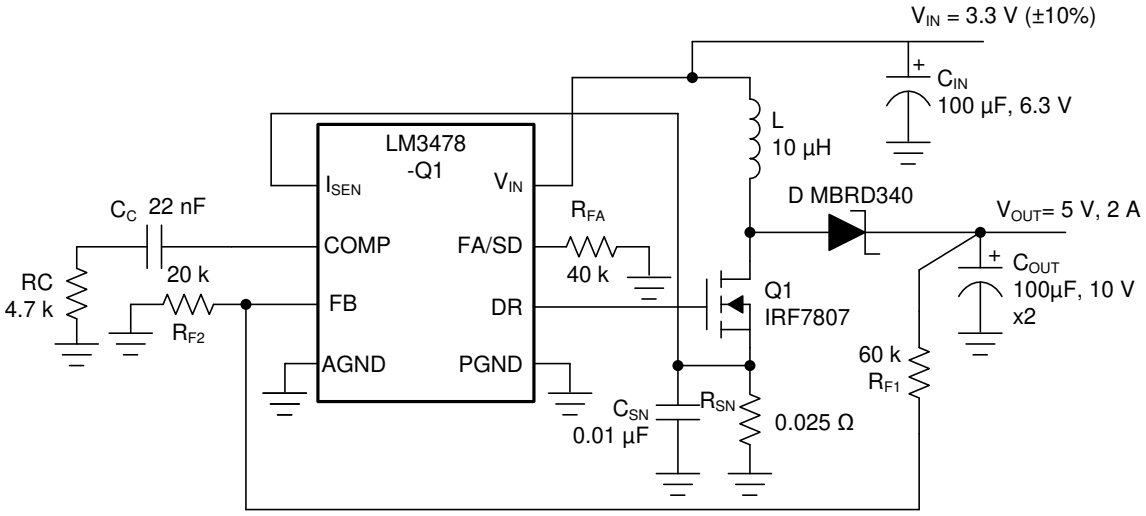


Figure 7-1. Typical High Efficiency Step-Up (Boost) Converter Schematic

The boost converter converts a low input voltage into a higher output voltage. The basic configuration for a boost converter is shown in Figure 7-2. In the CCM (when the inductor current never reaches zero at steady state), the boost regulator operates in two states. In the first state of operation, MOSFET Q is turned on and energy is stored in the inductor. During this state, diode D is reverse biased and load current is supplied by the output capacitor, C_{OUT}.

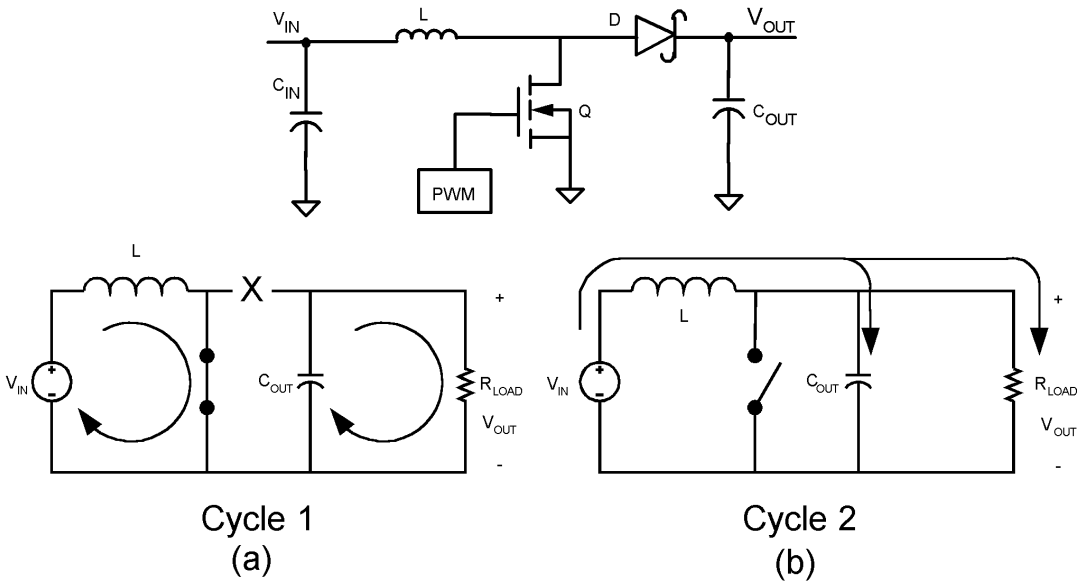
In the second state, MOSFET Q is off and the diode is forward biased. The energy stored in the inductor is transferred to the load and the output capacitor. The ratio of the switch on time to the total period is the duty cycle D as shown in Equation 8.

$$D = 1 - (V_{in} / V_{out}) \quad (8)$$

Including the voltage drop across the MOSFET and the diode the definition for the duty cycle is shown in Equation 9.

$$D = 1 - ((V_{in} - V_q)/(V_{out} + V_d)) \quad (9)$$

V_d is the forward voltage drop of the diode and V_q is the voltage drop across the MOSFET when it is on.



A. First Cycle Operation
B. Second Cycle of Operation

Figure 7-2. Simplified Boost Converter

7.2.1.1 Design Requirements

To properly size the components for the application, the designer needs the following parameters: input voltage range, output voltage, output current range, and required switching frequency. These four main parameters affect the choices of component available to achieve a proper system behavior.

For the power supply, the input impedance of the supply rail should be low enough that the input current transient does not drop below the UVLO value. The factors determining the choice of inductor used should be the average inductor current, and the inductor current ripple. If the switching frequency is set high, the converter can be operated with very small inductor values. The maximum current that can be delivered to the load is set by the sense resistor, RSEN. Current limit occurs when the voltage generated across the sense resistor equals the current sense threshold voltage, VSENSE. Also, a resistor RSL adds additional slope compensation, if required.

The following sections describe the design requirements for a typical LM3478Q-Q1 boost application.

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LM3478Q-Q1 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

7.2.1.2.2 Power Inductor Selection

The inductor is one of the two energy storage elements in a boost converter. Figure 7-3 shows how the inductor current varies during a switching cycle. The current through an inductor is quantified using Equation 10, which shows the relationship of L, I_L and V_L.

$$V_L(t) = L \frac{di_L(t)}{dt} \tag{10}$$

The important quantities in determining a proper inductance value are I_L (the average inductor current) and ΔI_L (the inductor current ripple). If ΔI_L is larger than I_L, the inductor current will drop to zero for a portion of the cycle and the converter will operate in the DCM. All the analysis in this datasheet assumes operation in the CCM. To operate in the CCM, the following condition must be met by using Equation 11.

$$L > \frac{D(1-D)V_{IN}}{2I_{OUT}f_S} \tag{11}$$

Choose the minimum I_{OUT} to determine the minimum inductance value. A common choice is to set ΔI_L to 30% of I_L. Choosing an appropriate core size for the inductor involves calculating the average and peak currents expected through the inductor. Use Equation 12, Equation 13, and Equation 14 to the peak inductor current in a boost converter.

$$I_{LPEAK} = \text{Average } I_{L(max)} + \Delta I_{L(max)} \tag{12}$$

$$\text{Average } I_{L(max)} = I_{out} / (1-D) \tag{13}$$

$$\Delta I_{L(max)} = D \times V_{in} / (2 \times f_s \times L) \tag{14}$$

An inductor size with ratings higher than these values has to be selected. If the inductor is not properly rated, saturation will occur and may cause the circuit to malfunction.

The LM3478Q-Q1 can be set to switch at very high frequencies. When the switching frequency is high, the converter can be operated with very small inductor values. The LM3478Q-Q1 senses the peak current through the switch which is the same as the peak inductor current as calculated in the previous equation.

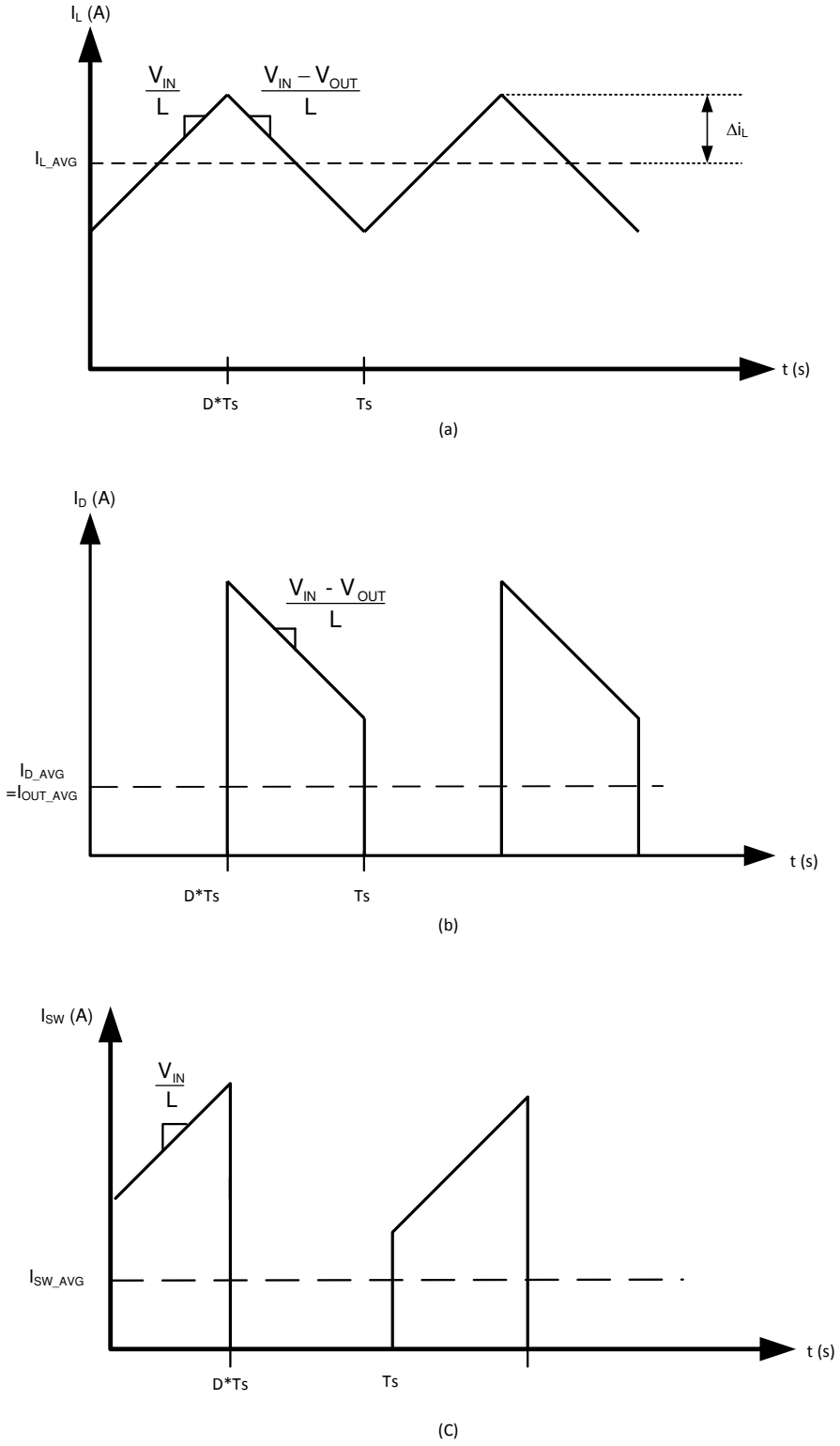


Figure 7-3. Inductor Current and Diode Current

7.2.1.2.3 Programming the Output Voltage

The output voltage can be programmed using a resistor divider between the output and the FB pin. The resistors are selected such that the voltage at the FB pin is 1.26 V. Pick R_{F1} (the resistor between the output voltage

and the feedback pin) and R_{F2} (the resistor between the feedback pin and ground) can be selected using the following equation,

$$R_{F2} = (1.26\ V \times R_{F1}) / (V_{out} - 1.26\ V) \quad (15)$$

A 100-pF capacitor may be connected between the feedback and ground pins to reduce noise.

7.2.1.2.4 Setting the Current Limit

The maximum amount of current that can be delivered to the load is set by the sense resistor, R_{SEN}. Current limit occurs when the voltage that is generated across the sense resistor equals the current sense threshold voltage, V_{SENSE}. When this threshold is reached, the switch will be turned off until the next cycle. Limits for V_{SENSE} are specified in the electrical characteristics section. V_{SENSE} represents the maximum value of the internal control signal V_{CS} as shown in Figure 7-4. This control signal, however, is not a constant value and changes over the course of a period as a result of the internal compensation ramp (V_{SL}). Therefore the current limit threshold will also change. The actual current limit threshold is a function of the sense voltage (V_{SENSE}) and the internal compensation ramp:

$$R_{SEN} \times ISW_{LIMIT} = VCS_{MAX} = V_{SENSE} - (D \times V_{SL}) \quad (16)$$

Where ISW_{LIMIT} is the peak switch current limit, defined by Equation 17.

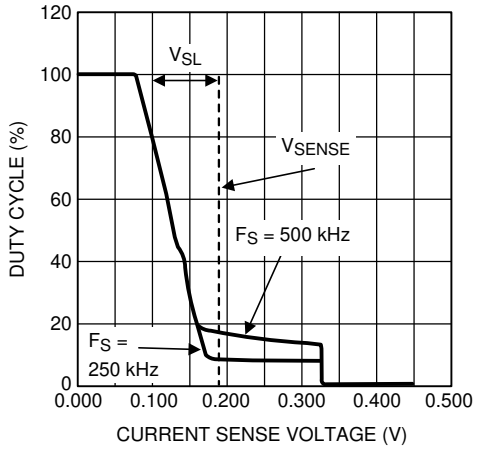


Figure 7-4. Current Sense Voltage vs Duty Cycle

Figure 7-4 shows how V_{CS} (and current limit threshold voltage) change with duty cycle. The curve is equivalent to the internal compensation ramp slope (S_e) and is bounded at low duty cycle by V_{SENSE}, shown as a dotted line. As duty cycle increases, the control voltage is reduced as V_{SL} ramps up. The graph also shows the short circuit current limit threshold of 343mV (typical) during the 325 ns (typical) blanking time. For higher frequencies this fixed blanking time obviously occupies more duty cycle, percentage wise. Since current limit threshold varies with duty cycle, the use Equation 17 to select R_{SEN} and set the desired current limit threshold:

$$R_{SEN} = \frac{V_{SENSE} - (D \times V_{SL})}{ISW_{LIMIT}} \quad (17)$$

The numerator of Equation 17 is V_{CS}, and ISW_{LIMIT} using Equation 18.

$$ISW_{LIMIT} = \left[\frac{I_{OUT}}{(1-D)} + \frac{(D \times V_{IN})}{(2 \times f_S \times L)}\right] \quad (18)$$

To avoid false triggering, the current limit value should have some margin above the maximum operating value, typically 120%. Values for both V_{SENSE} and V_{SL} are specified in *Section 5.5*. However, calculating with the limits of these two specs could result in an unrealistically wide current limit or R_{SEN} range. Therefore, Equation 19 is recommended, using the V_{SL} ratio value given in *Section 5.5*.

$$R_{SEN} = \frac{V_{SENSE} - (D \times V_{SENSE} \times V_{SL}ratio)}{ISW_{LIMIT}} \quad (19)$$

R_{SEN} is part of the current mode control loop and has some influence on control loop stability. Therefore, once the current limit threshold is set, loop stability must be verified. As described in the slope compensation section, Equation 20 must hold true for a current mode converter to be stable.

$$S_f - S_e < S_n + S_e \quad (20)$$

To verify that this equation holds true, use Equation 21.

$$R_{SEN} < \frac{2 \times V_{SL} \times f_S \times L}{Vo - (2 \times V_{IN})} \quad (21)$$

If the selected RSEN is greater than this value, additional slope compensation must be added to ensure stability, as described in the section below.

7.2.1.2.5 Current Limit with External Slope Compensation

R_{SL} is used to add additional slope compensation when required. It is not necessary in most designs and R_{SL} should be no larger than necessary. Select RSL according to Equation 22.

$$R_{SL} > \frac{\frac{R_{SEN} \times (Vo - 2V_{IN})}{2 \times f_S \times L} - V_{SL}}{40\ \mu A} \quad (22)$$

Where R_{SEN} is the selected value based on current limit. With RSL installed, the control signal includes additional external slope to stabilize the loop, which will also have an effect on the current limit threshold. Therefore, the current limit threshold must be re-verified, as illustrated in Equation 23, Equation 24, and Equation 25 below.

$$V_{CS} = V_{SENSE} – (D \times (V_{SL} + \Delta V_{SL})) \quad (23)$$

Where ΔV_{SL} is the additional slope compensation generated as discussed in the slope compensation ramp section and calculated using Equation 24.

$$\Delta V_{SL} = 40\ \mu A \times R_{SL} \quad (24)$$

This changes the equation for current limit (or R_{SEN}) as shown in Equation 25.

$$ISW_{LIMIT} = \frac{V_{SENSE} - (D \times (V_{SL} + \Delta V_{SL}))}{R_{SEN}} \quad (25)$$

The R_{SEN} and R_{SL} values may have to be calculated iteratively in order to achieve both the desired current limit and stable operation. In some designs R_{SL} can also help to filter noise on the I_{SEN} pin.

If the inductor is selected such that ripple current is the recommended 30% value, and the current limit threshold is 120% of the maximum peak, a simpler method can be used to determine R_{SEN}. Equation 26 below will provide optimum stability without RSL, provided that the above 2 conditions are met.

$$R_{SEN} = \frac{V_{SENSE}}{ISW_{LIMIT} + \left(\frac{Vo - Vi}{L \times f_S}\right) \times D} \quad (26)$$

7.2.1.2.6 Power Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than its peak current. The peak diode current can be calculated using Equation 27.

$$I_{D(Peak)} = I_{OUT} / (1-D) + \Delta I_L \quad (27)$$

Thermally the diode must be able to handle the maximum average current delivered to the output. The peak reverse voltage for boost converters is equal to the regulated output voltage. The diode must be capable of handling this voltage. To improve efficiency, a low forward drop schottky diode is recommended.

7.2.1.2.7 Power MOSFET Selection

The drive pin of the LM3478Q-Q1 must be connected to the gate of an external MOSFET. The drive pin (DR) voltage depends on the input voltage (see *Section 5.6*). In most applications, a logic level MOSFET can be used. For very low input voltages, a sub logic level MOSFET should be used. The selected MOSFET has a great influence on the system efficiency. The critical parameters for selecting a MOSFET are:

1. Minimum threshold voltage, V_{TH}(MIN)
2. On-resistance, $R_{DS(ON)}$
3. Total gate charge, Q_g
4. Reverse transfer capacitance, C_{RSS}
5. Maximum drain to source voltage, $V_{DS(MAX)}$

The off-state voltage of the MOSFET is approximately equal to the output voltage. Vds(max) must be greater than the output voltage. The power losses in the MOSFET can be categorized into conduction losses and switching losses. $R_{DS(ON)}$ is needed to estimate the conduction losses, Pcond:

$$Pcond = I^2 \times R_{DS(ON)} \times D \quad (28)$$

The temperature effect on the $R_{DS(ON)}$ usually is quite significant. Assume 30% increase at hot.

For the current I in Equation 28 the average inductor current may be used.

Especially at high switching frequencies the switching losses may be the largest portion of the total losses.

The switching losses are very difficult to calculate due to changing parasitics of a given MOSFET in operation. Often the individual MOSFET's data sheet does not give enough information to yield a useful result. Equation 29 and Equation 30 give a rough idea how the switching losses are calculated:

$$P_{SW} = \frac{I_{Lmax} \times V_{out}}{2} \times f_{SW} \times (t_{LH} + t_{HL}) \quad (29)$$

$$t_{LH} = \left(Qgd + \frac{Qgs}{2}\right) \times \frac{Rdr_{On}}{Vdr - Vgs_{th}} \quad (30)$$

7.2.1.2.8 Input Capacitor Selection

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous and triangular as shown in Figure 7-3. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The RMS current in the input capacitor is given using Equation 31.

$$I_{CIN(RMS)} = \Delta i_L / \sqrt{3} = \frac{1}{2\sqrt{3}} \left(\frac{V_{OUT} - V_{IN}}{V_{OUT} L f_S} \right) X\ V_{in} \quad (31)$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 10 µF to 20 µF. If a value lower than 10 µF is used, then problems with impedance interactions or switching noise can affect the LM3478Q-Q1. To improve performance, especially with Vin below 8 volts, it is recommended to use a 20 Ohm resistor at the input to provide an RC filter. The resistor is placed in series with the VIN pin with only a bypass capacitor attached to the VIN pin directly (see Figure 7-5). A 0.1-µF or 1-µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor at the input power supply.

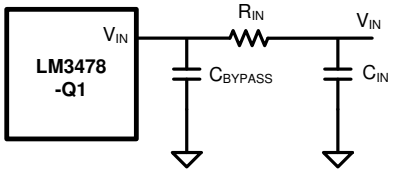


Figure 7-5. Reducing IC Input Noise

7.2.1.2.9 Output Capacitor Selection

The output capacitor in a boost converter provides all the output current when the inductor is charging. As a result it sees very large ripple currents. The output capacitor should be capable of handling the maximum RMS current. Equation 32 shows the RMS current in the output capacitor.

$$I_{COUT(RMS)} = \sqrt{(1\text{-}D) \left[I_{OUT}^2 \frac{D}{(1\text{-}D)^2} + \frac{\Delta i_L^2}{3} \right]} \quad (32)$$

Where

$$\Delta i_L = \frac{D V_{IN}}{2 L f_S} \quad (33)$$

The ESR and ESL of the capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic, polymer tantalum, or multi-layer ceramic capacitors are recommended at the output.

For applications that require very low output voltage ripple, a second stage LC filter often is a good solution. Most of the time it is lower cost to use a small second Inductor in the power path and an additional final output capacitor than to reduce the output voltage ripple by purely increasing the output capacitor without an additional LC filter.

7.2.1.2.10 Compensation

For detailed explanation on how to select the right compensation components to attach to the compensation pin for a boost topology, please see *AN-1286 Compensation For The LM3748 Boost Controller* SNVA067.

7.2.1.3 Application Curves

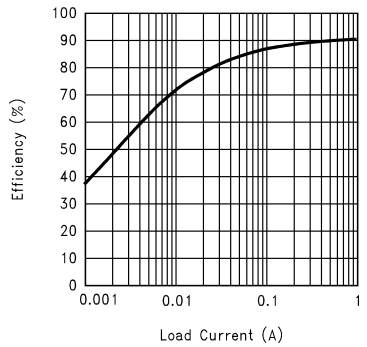


Figure 7-6. Efficiency vs Load Current (9-V In and 12-V Out)

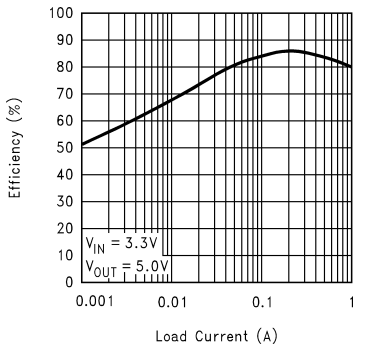


Figure 7-7. Efficiency vs Load Current (3.3-V In and 5-V Out)

7.2.2 Typical SEPIC Converter

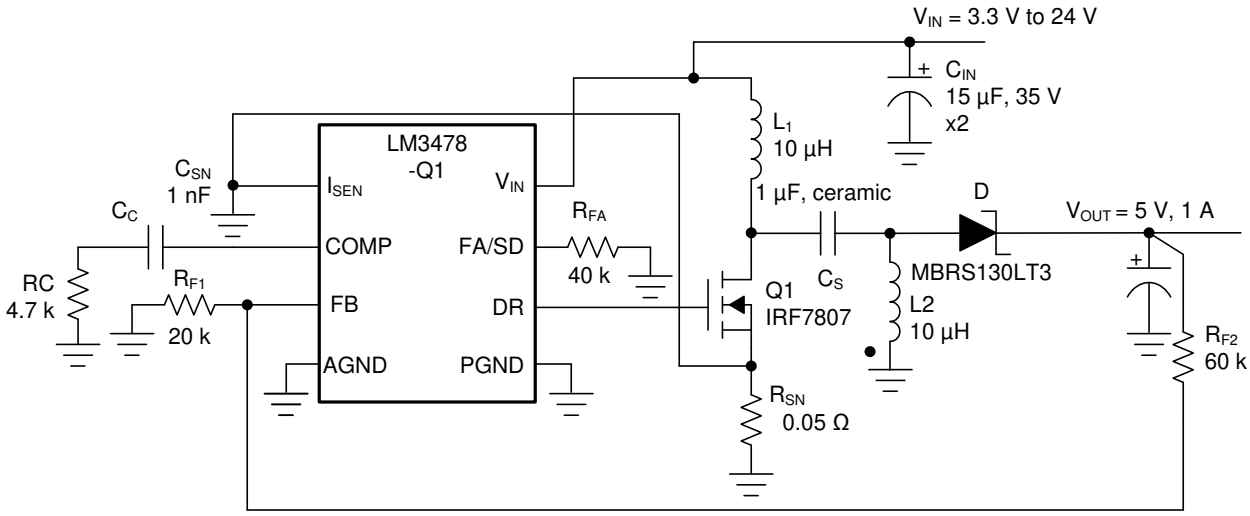


Figure 7-8. Typical SEPIC Converter

Since the LM3478Q-Q1 controls a low-side N-Channel MOSFET, it can also be used in SEPIC (Single Ended Primary Inductance Converter) applications. An example of a SEPIC using the LM3478Q-Q1 is shown in Figure 7-8. Note that the output voltage can be higher or lower than the input voltage. The SEPIC uses two inductors to step-up or step-down the input voltage. The inductors L1 and L2 can be two discrete inductors or two windings of a coupled inductor since equal voltages are applied across the inductor throughout the switching cycle. Using two discrete inductors allows use of catalog magnetics, as opposed to a custom inductor. The input ripple can be reduced along with size by using the coupled windings for L1 and L2.

Due to the presence of the inductor L1 at the input, the SEPIC inherits all the benefits of a boost converter. One main advantage of a SEPIC over a boost converter is the inherent input to output isolation. The capacitor CS isolates the input from the output and provides protection against a shorted or malfunctioning load. Hence, the SEPIC is useful for replacing boost circuits when true shutdown is required. This means that the output voltage falls to 0V when the switch is turned off. In a boost converter, the output can only fall to the input voltage minus a diode drop.

The duty cycle of a SEPIC is given using Equation 34.

$$D = \frac{V_{OUT} + V_{DIODE}}{V_{OUT} + V_{IN} - V_Q + V_{DIODE}} \quad (34)$$

In Equation 34, V_Q is the on-state voltage of the MOSFET, Q, and V_{DIODE} is the forward voltage drop of the diode.

7.2.2.1 Design Requirements

To properly size the components for the application, the designer needs the following parameters: input voltage range, output voltage, output current range, and required switching frequency. These four main parameters affect the choices of component available to achieve a proper system behavior.

For the power supply, the input impedance of the supply rail should be low enough that the input current transient does not drop below the UVLO value. The factors determining the choice of inductor used should be the average inductor current, and the inductor current ripple. If the switching frequency is set high, the converter can be operated with very small inductor values. The maximum current that can be delivered to the load is set by the sense resistor, RSEN. Current limit occurs when the voltage generated across the sense resistor equals the current sense threshold voltage, VSENSE. Also, a resistor RSL adds additional slope compensation, if required.

The following sections describe the design requirements for a typical LM3478Q-Q1 boost application.

7.2.2.2 Detailed Design Procedure

7.2.2.2.1 Power MOSFET Selection

As in a boost converter, parameters governing the selection of the MOSFET are the minimum threshold voltage, $V_{TH(MIN)}$, the on-resistance, $R_{DS(ON)}$, the total gate charge, Q_g, the reverse transfer capacitance, C_{RSS}, and the maximum drain to source voltage, $V_{DS(MAX)}$. The peak switch voltage in a SEPIC is given using Equation 35.

$$V_{SW(PEAK)} = V_{IN} + V_{OUT} + V_{DIODE} \quad (35)$$

The selected MOSFET should satisfy the condition:

$$V_{DS(MAX)} > V_{SW(PEAK)} \quad (36)$$

The peak switch current is given using Equation 37.

$$I_{SW(PEAK)} = I_{L1(AVG)} + I_{OUT} + \frac{\Delta I_{L1} + \Delta I_{L2}}{2} \quad (37)$$

The RMS current through the switch is given using Equation 38.

$$I_{SWRMS} = \sqrt{\left[I_{SWPEAK}^2 - I_{SWPEAK}\left(\Delta I_{L1} + \Delta I_{L2}\right) + \frac{\left(\Delta I_{L1} + \Delta I_{L2}\right)^2}{3}\right] D} \quad (38)$$

7.2.2.2.2 Power Diode Selection

The Power diode must be selected to handle the peak current and the peak reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current. The off-state voltage or peak reverse voltage of the diode is V_{IN} + V_{OUT}. Similar to the boost converter, the average diode current is equal to the output current. Schottky diodes are recommended.

7.2.2.2.3 Selection of Inductors L1 and L2

Proper selection of inductors L1 and L2 to maintain continuous current conduction mode requires calculations of the following parameters.

Average current in the inductors can be calculated using Equation 39.

$$I_{L1AVE} = \frac{DI_{OUT}}{1-D} \quad (39)$$

$$I_{L2AVE} = I_{OUT} \quad (40)$$

Peak to peak ripple current, to calculate core loss if necessary using Equation 41 and Equation 42.

$$\Delta I_{L1} = \frac{(V_{IN} - V_Q)\, D}{(L1) f_S} \quad (41)$$

$$\Delta I_{L2} = \frac{(V_{IN} - V_Q)\, D}{(L2) f_S} \quad (42)$$

Maintaining the condition $I_L > \Delta i_L/2$ to ensure continuous current conduction yields Equation 43 and Equation 44.

$$L1 > \frac{(V_{IN} - V_Q)(1-D)}{2 I_{OUT} f_S} \quad (43)$$

$$L2 > \frac{(V_{IN} - V_Q) D}{2 I_{OUT} f_S} \quad (44)$$

Peak current in the inductor, use Equation 45 and Equation 46 to ensure the inductor does not saturate.

$$I_{L1PK} = \frac{DI_{OUT}}{1-D} + \frac{\Delta I_{L1}}{2} \quad (45)$$

$$I_{L2PK} = I_{OUT} + \frac{\Delta I_{L2}}{2} \quad (46)$$

I_{L1PK} must be lower than the maximum current rating set by the current sense resistor.

The value of L1 can be increased above the minimum recommended to reduce input ripple and output ripple. However, once D_{IL1} is less than 20% of I_{L1AVE}, the benefit to output ripple is minimal.

By increasing the value of L2 above the minimum recommended, Δ_{IL2} can be reduced, which in turn will reduce the output ripple voltage:

$$\Delta V_{OUT} = \left(\frac{I_{OUT}}{1-D} + \frac{\Delta I_{L2}}{2} \right) \text{ESR} \quad (47)$$

where ESR is the effective series resistance of the output capacitor.

If L1 and L2 are wound on the same core, then L1 = L2 = L. All of the previous equations will hold true if the inductance is replaced by 2L.

7.2.2.2.4 Sense Resistor Selection

The peak current through the switch, $I_{SW(PEAK)}$ can be adjusted using the current sense resistor, R_{SEN}, to provide a certain output current. Resistor R_{SEN} can be selected using Equation 48

$$R_{SEN} = \frac{V_{SENSE} - D(V_{SL} + \Delta V_{SL})}{I_{SWPEAK}} \quad (48)$$

7.2.2.2.5 Sepic Capacitor Selection

The selection of the SEPIC capacitor, CS, depends on the RMS current. The RMS current of the SEPIC capacitor is given by Equation 49.

$$I_{CSRMS} = \sqrt{I_{SWRMS}^2 + \left(I_{L1PK}^2 - I_{L1PK}\Delta I_{L1} + \Delta I_{L1}^2\right)\left(1\text{-}D\right)} \tag{49}$$

The SEPIC capacitor must be rated for a large ACrms current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the RMS current through the capacitor is relatively small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. There is an energy balance between CS and L1, which can be used to determine the value of the capacitor. Equation 50 shows the basic energy balance.

$$\frac{1}{2} C_S \Delta V_S^2 = \frac{1}{2} L_1 \Delta I_{L1}^2 \tag{50}$$

where

$$\Delta V_S = \left(\frac{V_{OUT}}{V_{OUT} + V_{IN} - V_Q + V_{DIODE}}\right) \frac{I_{OUT}}{f_S C_S} \tag{51}$$

is the ripple voltage across the SEPIC capacitor, and

$$\Delta I_{L1} = \frac{(V_{IN} - V_Q)\, D}{L_1 f_S} \tag{52}$$

is the ripple current through the inductor L1. The energy balance equation can be solved using Equation 53 to provide a minimum value for C_S.

$$C_S \geq L_1 \frac{I_{OUT}^2}{(V_{IN} - V_Q)^2} \tag{53}$$

7.2.2.2.6 Input Capacitor Selection

Similar to a boost converter, the SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The RMS current in the input capacitor is given using Equation 54.

$$I_{CIN(RMS)} = \Delta I_{L1} / \sqrt{12} = \frac{D}{2\sqrt{3}} \left(\frac{V_{IN} - V_Q}{L_1 f_S}\right) \tag{54}$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 10µF to 20µF. If a value lower than 10µF is used, then problems with impedance interactions or switching noise can affect the LM3478Q-Q1. To improve performance, especially with V_{IN} below 8V, TI recommends that the user uses a 20Ω resistor at the input to provide a RC filter. The resistor is placed in series with the V_{IN} pin with only a bypass capacitor attached to the V_{IN} pin directly (see Figure 7-5). A 0.1µF or 1µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor with the input power supply.

7.2.2.2.7 Output Capacitor Selection

The output capacitor of the SEPIC sees very large ripple currents (similar to the output capacitor of a boost converter). The RMS current through the output capacitor is given using Equation 55.

$$I_{RMS} = \sqrt{\left[I_{SWPK}^2 - I_{SWPK}\left(\Delta I_{L1} + \Delta I_{L2}\right) + \frac{\left(\Delta I_{L1} + \Delta I_{L2}\right)^2}{3}\right](1-D) - I_{OUT}^2} \quad (55)$$

The ESR and ESL of the output capacitor directly control the output ripple. Use low capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic and polymer tantalum, Sanyo-OSCON, or multi-layer ceramic capacitors are recommended at the output for low ripple.

7.2.2.3 Application Curves

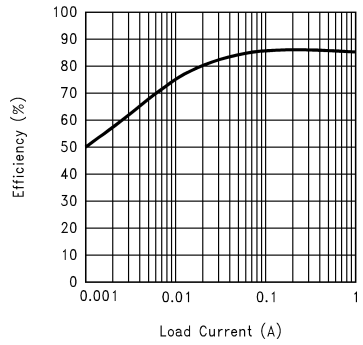


Figure 7-9. Efficiency vs Load Current (3.3V In and 12V Out)

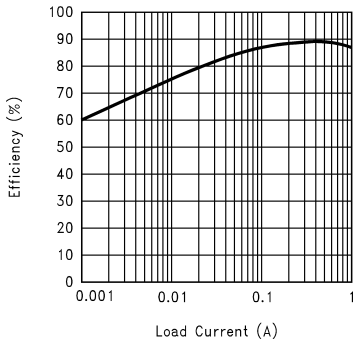


Figure 7-10. Efficiency vs Load Current (5V In and 12V Out)

7.3 Power Supply Recommendations

The LM3478Q-Q1 is designed to operate from various DC power supply including a car battery. If so, VIN input should be protected from reversal voltage and voltage dump over 40V. The impedance of the input supply rail should be low enough that the input current transient does not cause drop below VIN UVLO level. If the input supply is connected by using long wires, additional bulk capacitance may be required in addition to normal input capacitor.

7.4 Layout

7.4.1 Layout Guidelines

Good board layout is critical for switching controllers. First the ground plane area must be sufficient for thermal dissipation purposes and second, appropriate guidelines must be followed to reduce the effects of switching noise. Switching converters are very fast switching devices. In such devices, the rapid increase of input current combined with the parasitic trace inductance generates unwanted Ldi/dt noise spikes. The magnitude of this noise tends to increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI), and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise. The current sensing circuit in current mode devices can be easily affected by switching noise. This noise can cause duty cycle jittering which leads to increased spectral noise. Although the LM3478Q-Q1 has 325ns blanking time at the beginning of every cycle to ignore this noise, some noise may remain after the blanking time.

The most important layout rule is to keep the AC current loops as small as possible. Figure 7-11 shows the current flow of a boost converter. The top schematic shows a dotted line which represents the current flow during on-state and the middle schematic shows the current flow during off-state. The bottom schematic shows the currents we refer to as AC currents. They are the most critical ones since current is changing in very short time periods. The dotted lined traces of the bottom schematic are the once to make as short as possible.

The PGND and AGND pins have to be connected to the same ground very close to the device. To avoid ground loop currents, attach all the grounds of the system only at one point.

A ceramic input capacitor should be connected as close as possible to the VIN pin and grounded close to the GND pin.

For more information about layout in switch mode power supplies, please refer to AN-1229 Simple Switcher PCB Layout Guidelines application report.

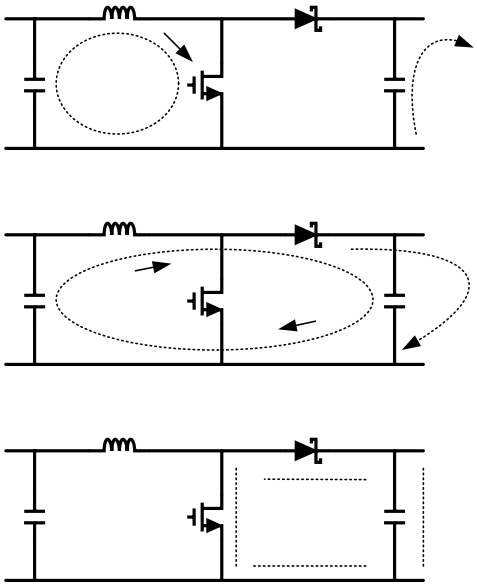
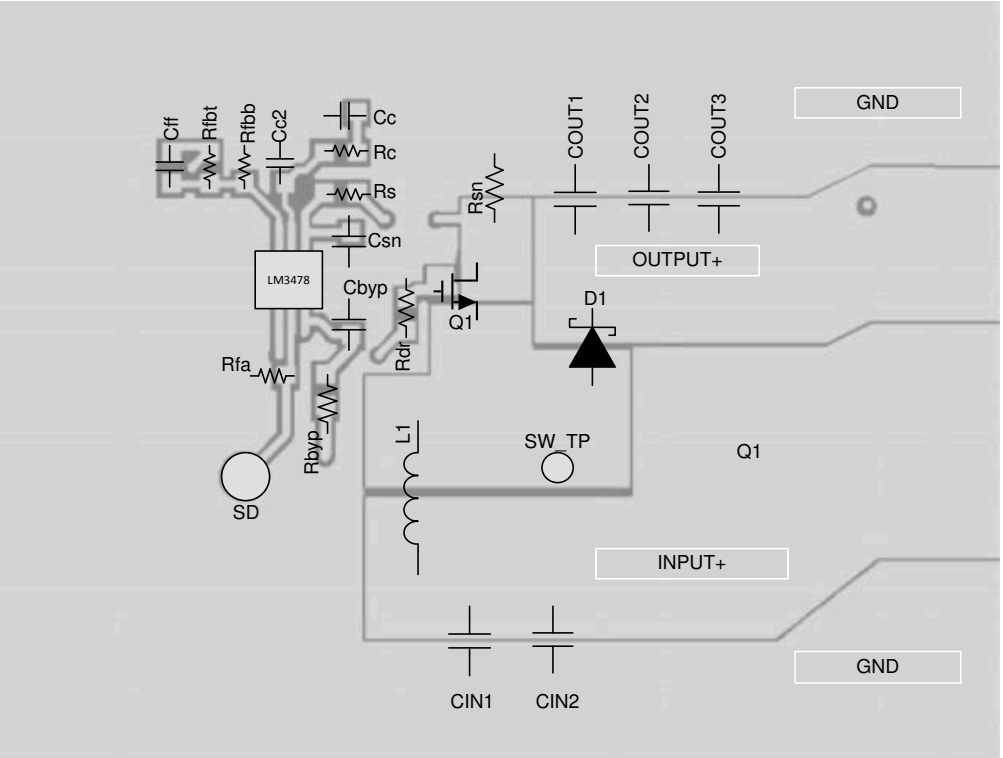


Figure 7-11. Current Flow in a Boost Application

7.4.2 Layout Example



See evaluation modules for more detailed examples.

Figure 7-12. Typical Layout for a Boost Converter

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.2 Development Support

For development support on this product, see the following:

8.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LM3478Q-Q1 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

8.3 Documentation Support

Create a custom design using LM3478 with WEBENCH Power Designer.

8.3.1 Related Documentation

For related documentation see the following:

- *AN-1286 Compensation for the LM3748 Boost Controller* SNVA067
- *AN-1229 Simple Switcher PCB Layout Guidelines* SNVA054

8.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2018) to Revision A (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated values of thermal table	4
• Updated values of I_{EAO}	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3478QMM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SSFB
LM3478QMM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SSFB
LM3478QMM/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SSFB
LM3478QMMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SSFB
LM3478QMMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SSFB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

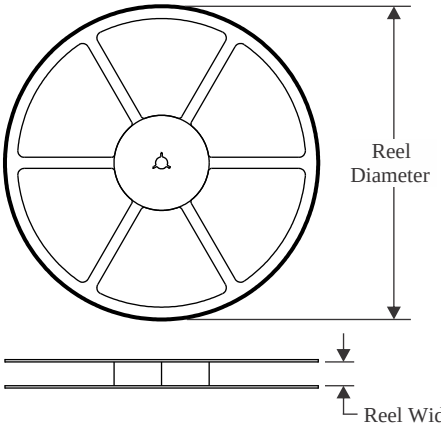
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

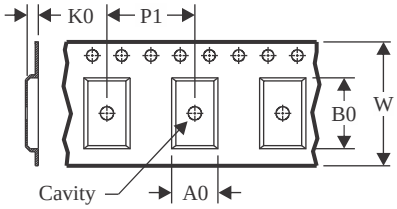
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

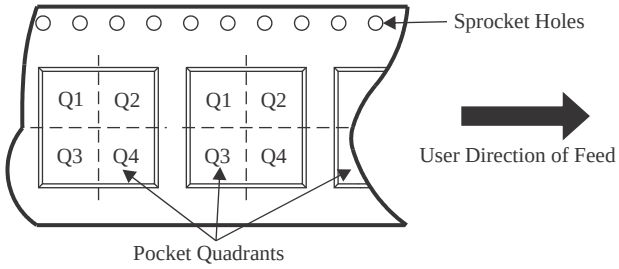


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

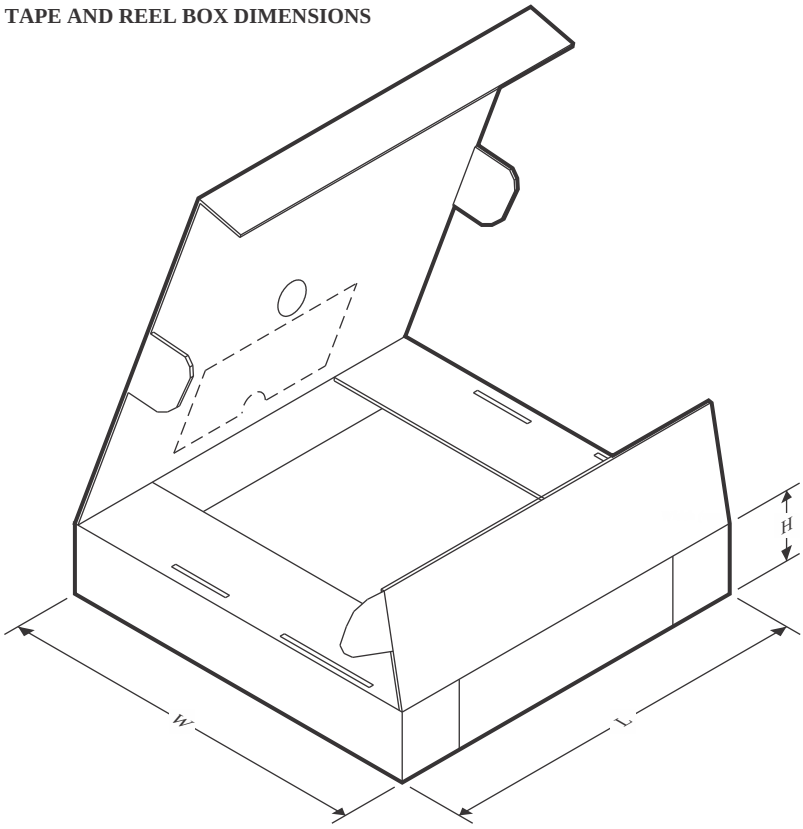
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3478QMM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3478QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

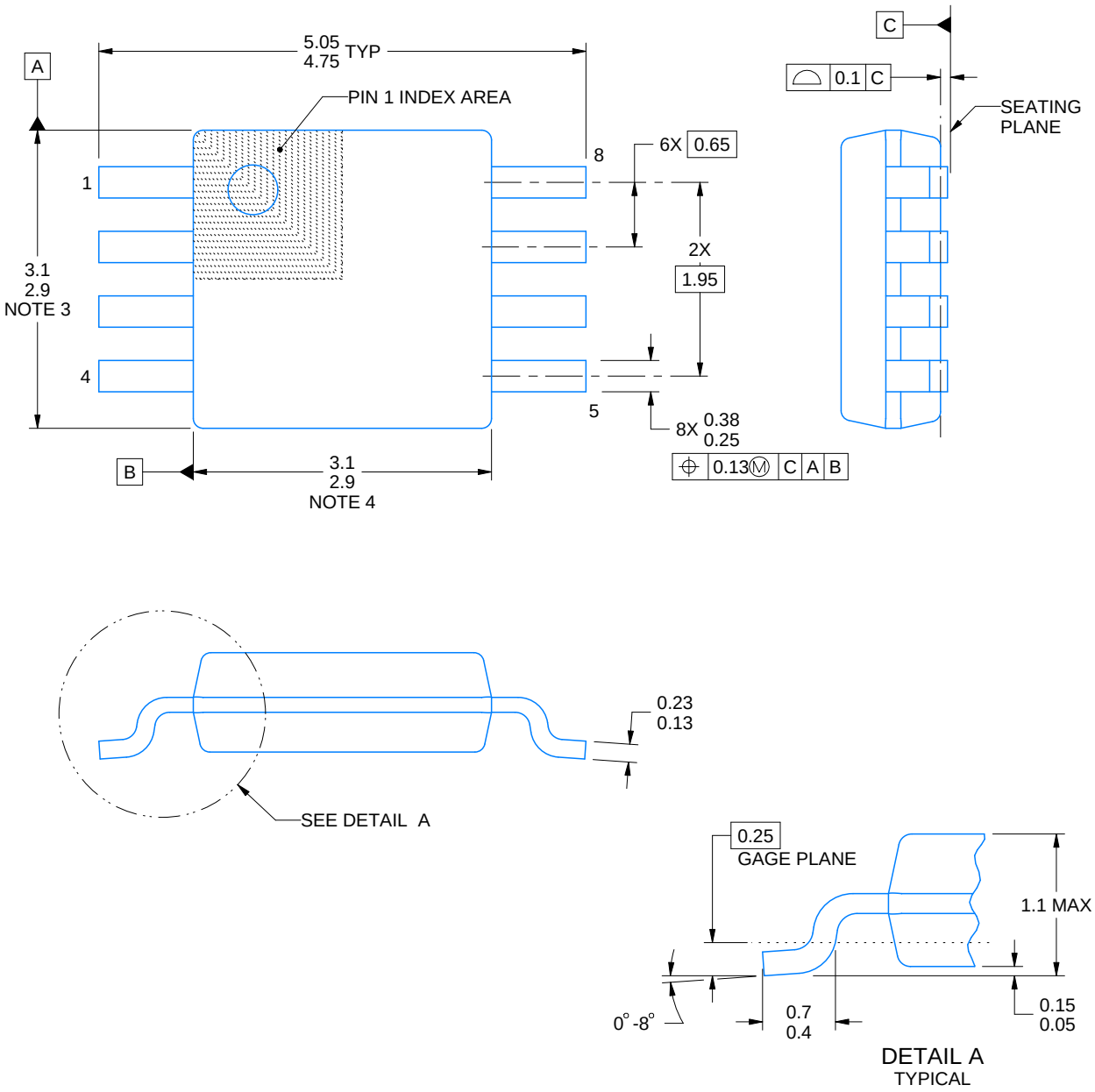
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3478QMM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM3478QMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

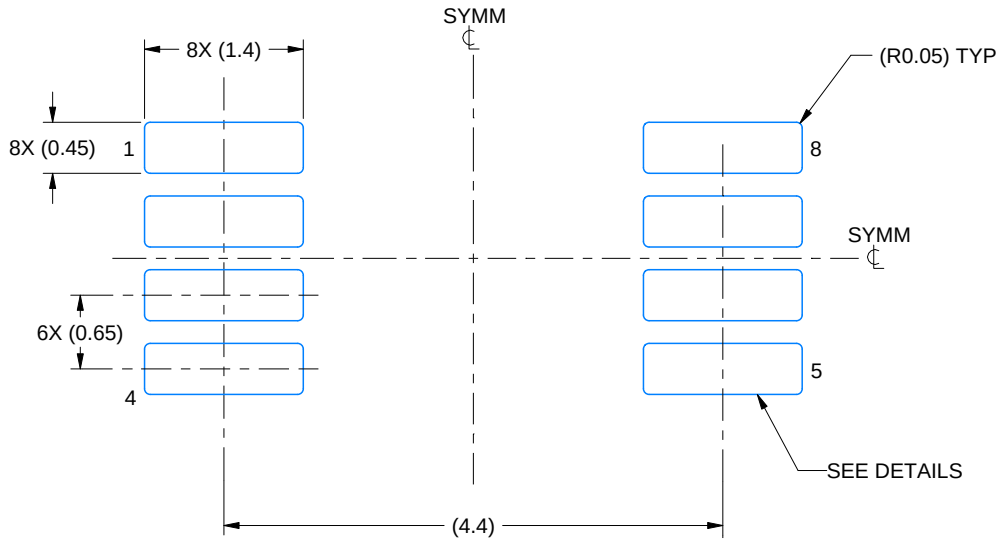
SMALL OUTLINE PACKAGE



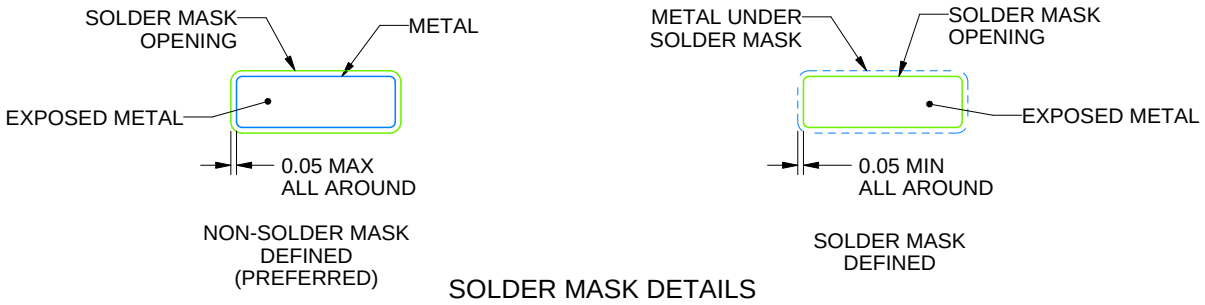
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

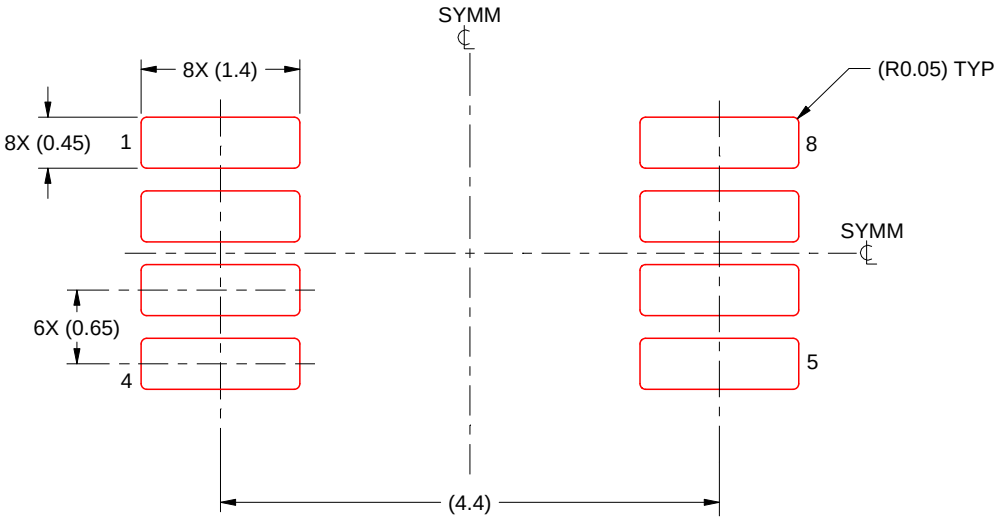


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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