- **Wide Bandwidth (BW = 500 MHz Typ)**
- **Low Crosstalk (X_{TALK} = –30 dB Typ)**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low and Flat ON-State Resistance (r_{on} = 4 Ω Typ, $r_{on(flat)}$ = 1 Ω)**
- **Switching on Data I/O Ports (0 to 5 V)**
- **V_{CC} Operating Range From 3 V to 3.6 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**

- **Data and Control Inputs Have Undershoot Clamp Diodes**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Suitable for Both 10 Base-T/100 Base-T Signaling**

**D, DBQ, DGV, OR PW PACKAGE
(TOP VIEW)**

S	1		16	V_{CC}
IA_0	2		15	$\overline{E}$
IA_1	3		14	ID_0
YA	4		13	ID_1
IB_0	5		12	YD
IB_1	6		11	IC_0
YB	7		10	IC_1
GND	8		9	YC

**RGY PACKAGE
(TOP VIEW)**

S — 1
V_{CC} — 16

IA_0	2		15	$\overline{E}$
IA_1	3		14	ID_0
YA	4		13	ID_1
IB_0	5		12	YD
IB_1	6		11	IC_0
YB	7		10	IC_1

GND — 8
YC — 9
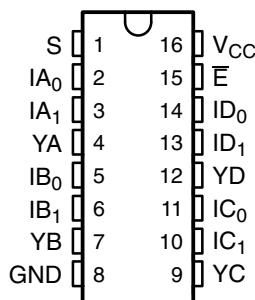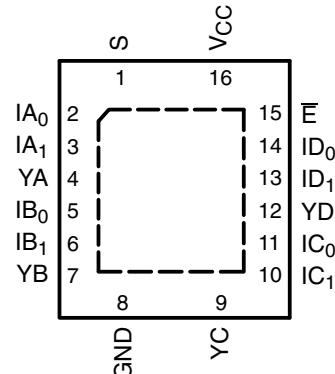
description/ordering information

The TI TS3L110 LAN switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable ($\overline{E}$) input. When $\overline{E}$ is low, the switch is enabled, and the I port is connected to the Y port. When $\overline{E}$ is high, the switch is disabled, and the high-impedance state exists between the I and Y ports. The select (S) input controls the data path of the multiplexer/demultiplexer.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	TS3L110RGYR	TK110
	SOIC – D	Tube	TS3L110D	TS3L110
		Tape and reel	TS3L110DR	
	SSOP (QSOP) – DBQ	Tape and reel	TS3L110DBQR	TK110
	TSSOP – PW	Tube	TS3L110PW	TK110
		Tape and reel	TS3L110PWR	
	TVSOP – DGV	Tape and reel	TS3L110DGVR	TK110

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

description/ordering information (continued)

This device can be used to replace mechanical relays in LAN applications. This device has low and flat r_{on}, wide bandwidth, and low crosstalk, making it suitable for 10 Base-T, 100 Base-T, and various other LAN applications. The device can be used to route signals from a 10/100 Base-T ethernet transceiver to the RJ-45 LAN connectors in laptops or in docking stations. The device is designed for low channel-to-channel skew and low crosstalk.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{E}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

INPUTS		INPUT/OUTPUT YX	FUNCTION
$\overline{E}$	S		
L	L	IX_0	$YX = IX_0$
L	H	IX_1	$YX = IX_1$
H	X	Z	Disconnect

PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
IAn–IDn	Data I/Os
S	Select input
$\overline{E}$	Enable input
YA–YD	Data I/Os

TEXAS
INSTRUMENTS

logic diagram (positive logic)
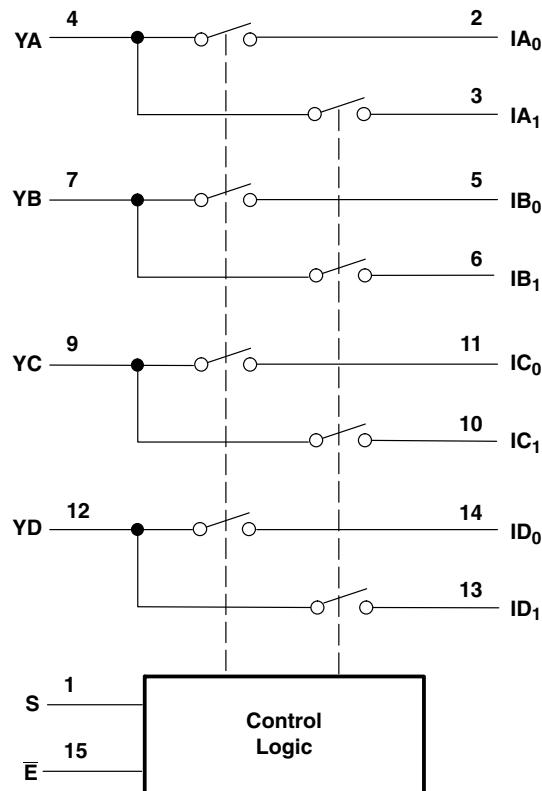
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} . . . . –0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . –0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . –0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$) . . . . –50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$) . . . . –50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . ±128 mA
Continuous current through V_{CC} or GND terminals . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): D package . . . . 73°C/W
(see Note 5): DBQ package . . . . 90°C/W
(see Note 5): DGV package . . . . 120°C/W
(see Note 5): PW package . . . . 108°C/W
(see Note 6): RGY package . . . . 39°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground, unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage ($\overline{E}$, S)	2	5.5	V
V_{IL}	Low-level control input voltage ($\overline{E}$, S)	0	0.8	V
$V_{I/O}$	Input/output voltage	0	5.5	V
T_A	Operating free-air temperature	–40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3$ V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{E}$, S	$V_{CC} = 3.6$ V,	$I_{IN} = -18$ mA				−1.8	V
I_{IH}	$\overline{E}$, S	$V_{CC} = 3.6$ V,	$V_{IN} = 5.5$ V				±1	µA
I_{IL}	$\overline{E}$, S	$V_{CC} = 3.6$ V,	$V_{IN} = $ GND				±1	µA
I_{off}		$V_{CC} = 0$,	$V_O = 0$ to 5.5 V ,	$V_I = 0$			1	µA
I_{CC}		$V_{CC} = 3.6$ V,	$I_{I/O} = 0$,	Switch ON or OFF		0.7	1.5	mA
C_{in}	$\overline{E}$, S	f = 1 MHz,	$V_{IN} = 0$			2.5	3.5	pF
$C_{io(OFF)}$	I port	$V_I = 0$,	f = 1 MHz, Outputs open,	Switch OFF		3.5	5	pF
	Y port	$V_I = 0$,	f = 1 MHz, Outputs open,	Switch OFF		5.5	7	
$C_{io(ON)}$	I or Y port	$V_I = 0$,	f = 1 MHz, Outputs open,	Switch ON		10.5	13	pF
r_{on}		$V_{CC} = 3$ V	1.25 V $\leq V_I \leq V_{CC}$,	$I_I = -10$ mA to −30 mA		4	8	Ω
$r_{on(flat)}$‡		$V_{CC} = 3$ V	$V_I = 1.25$ V and V_{CC},	$I_I = -10$ mA to −30 mA		1		Ω
Δr_{on}§		$V_{CC} = 3$ V,	1.25 V $\leq V_I \leq V_{CC}$,	$I_I = -10$ mA to −30 mA		0.9	2	Ω

V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
† All typical values are at $V_{CC} = 3.3$ V (unless otherwise noted), $T_A = 25°$C.
‡ $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
§ Δr_{on} is the difference of r_{on} in a given device.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3$ V ± 0.3 V, $R_L = 200$ Ω, $C_L = 10$ pF (unless otherwise noted) (see Figures 5 and 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{pd}¶	I or Y	Y or I		0.25		ns
t_{PZH}, t_{PZL}	$\overline{E}$ or S	I or Y	0.5		7	ns
t_{PHZ}, t_{PLZ}	$\overline{E}$ or S	I or Y	0.5		5	ns
$t_{sk(p)}$#	I or Y	Y or I		0.1	0.2	ns

† All typical values are at $V_{CC} = 3.3$ V (unless otherwise noted), $T_A = 25°$C.
¶ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
# Skew between opposite transitions of the same output $|t_{PHL} - t_{PLH}|$. This parameter is not production tested.

dynamic characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3$ V ± 0.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
X_{TALK}	$R_L = 100$ Ω,	f = 250 MHz, see Figure 7		−26		dB
O_{IRR}	$R_L = 100$ Ω,	f = 250 MHz, see Figure 8		−28		dB
BW	$R_L = 100$ Ω, see Figure 6			500		MHz

† All typical values are at $V_{CC} = 3.3$ V (unless otherwise noted), $T_A = 25°$C.

OPERATING CHARACTERISTICS

■ Phase at 627 MHz, –36 Degrees
▲ Gain –3 dB at 627 MHz
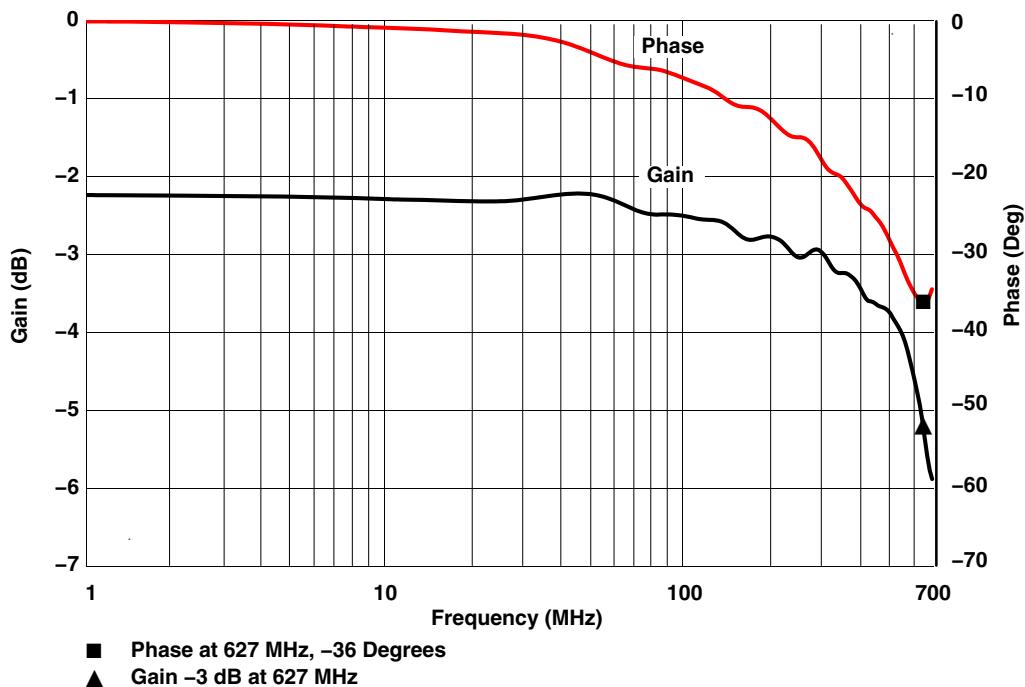
Figure 1. Gain/Phase vs Frequency

■ Phase at 250 MHz, 88.2 Degrees
▲ Gain –28.5 dB at 250 MHz
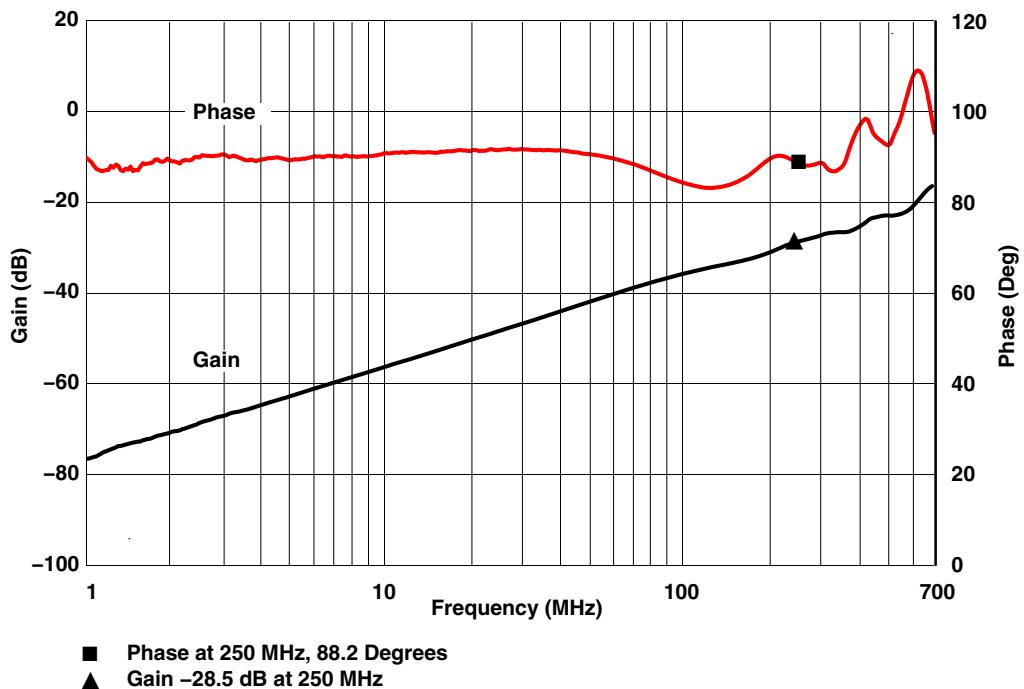
Figure 2. OFF Isolation vs Frequency

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OPERATING CHARACTERISTICS

■   **Phase at 250 MHz, 137.92 Degrees**
▲   **Gain –26 dB at 250 MHz**
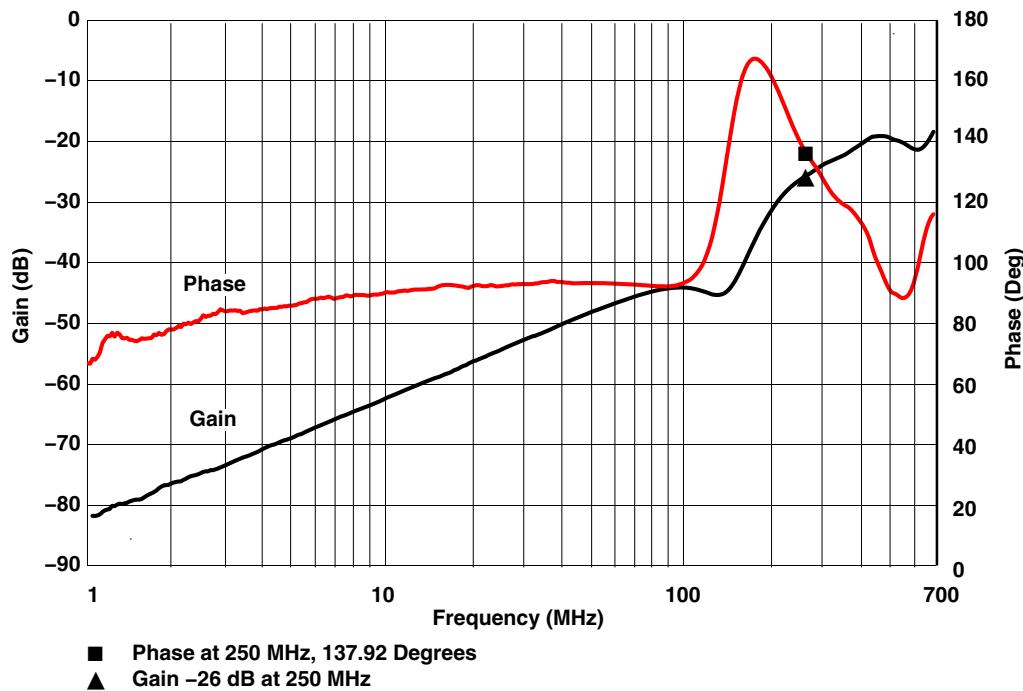
Figure 3. Crosstalk vs Frequency
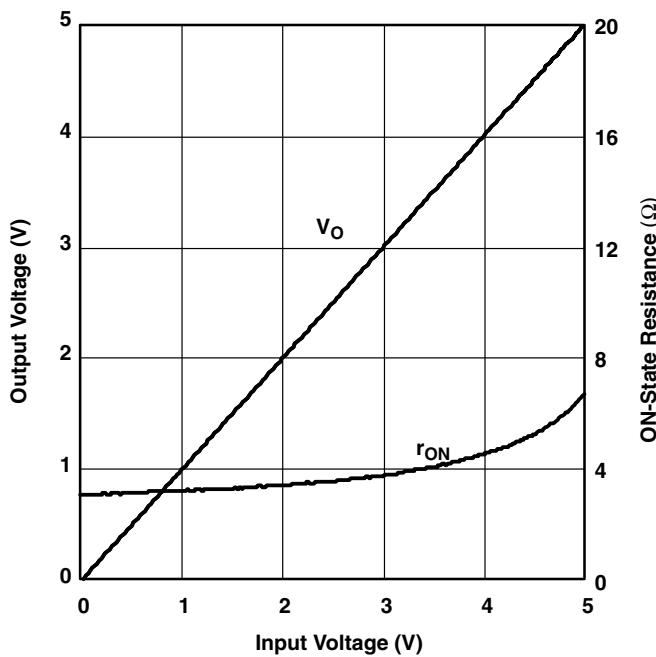
Figure 4. Output Voltage/ON-State Resistance vs Input Voltage

PARAMETER MEASUREMENT INFORMATION
FOR ENABLE AND DISABLE TIMES
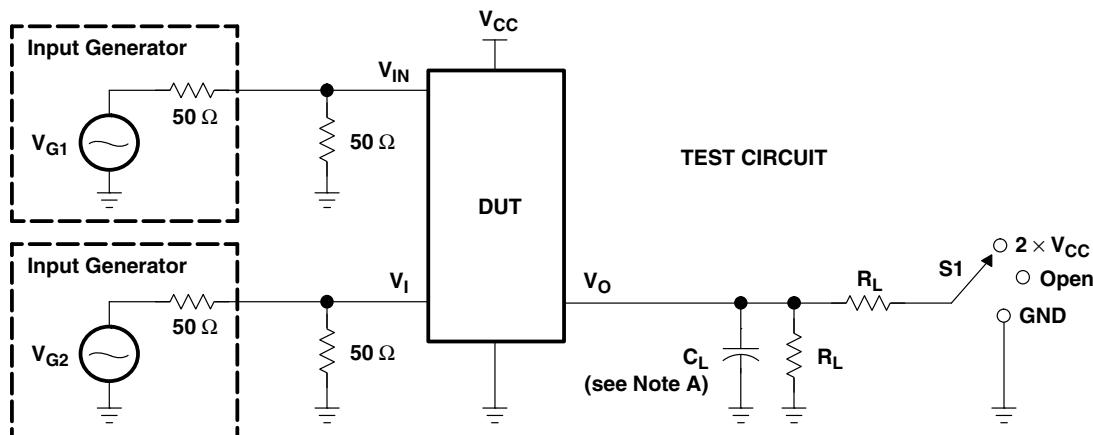
TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V $\pm$ 0.3 V	$2 \times V_{CC}$	200 Ω	GND	10 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V $\pm$ 0.3 V	GND	200 Ω	V_{CC}	10 pF	0.3 V
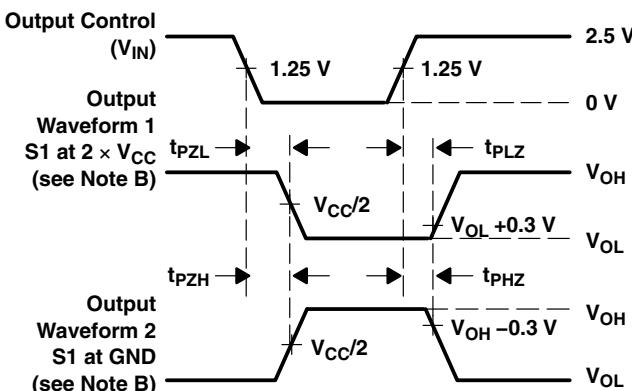
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
         Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
      D. The outputs are measured one at a time, with one transition per measurement.
      E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
      F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 5. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
FOR SKEW
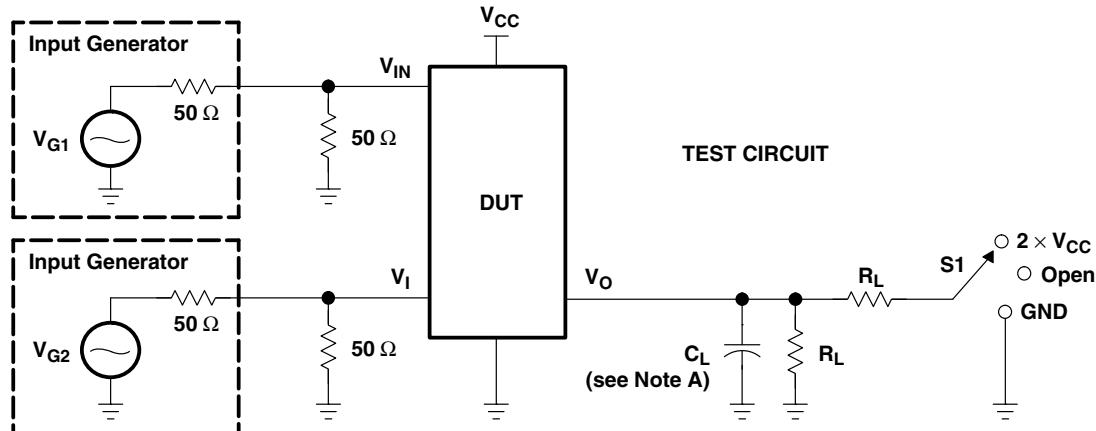
TEST	V_{CC}	S1	R_L	V_{IN} (see Note B)	C_L
$t_{sk(p)}$	3.3 V $\pm$ 0.3 V	GND	200 Ω	V_{CC} or GND	10 pF

$$t_{sk(p)} = |t_{PHL} - t_{PLH}|$$

VOLTAGE WAVEFORMS
PULSE SKEW ($t_{sk(p)}$)
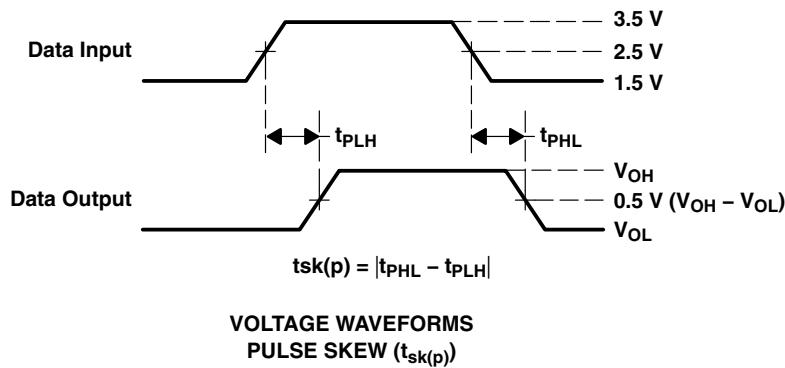
NOTES: A. C_L includes probe and jig capacitance.
        B. Switch is ON during the measurement of $t_{sk(p)}$, i.e., voltage at $\overline{E}$ = 0 and S = V_{CC} or GND

Figure 6. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
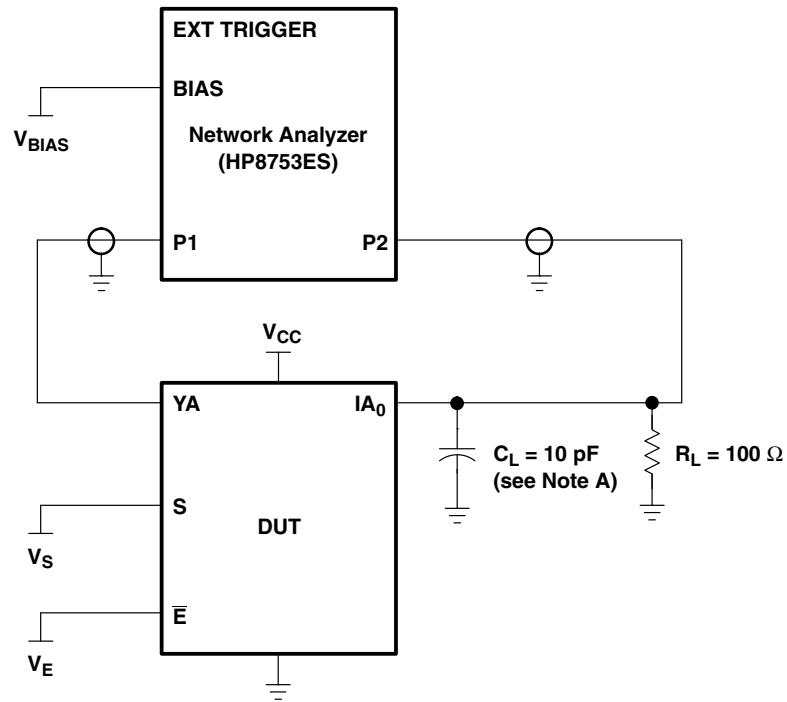
NOTE A: C_L includes probe and jig capacitance.

Figure 7. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when $V_S = 0$, $V_E = 0$, and YA is the input, the output is measured at IA_0. All unused analog I/O ports are left open.

HP8753ES setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION
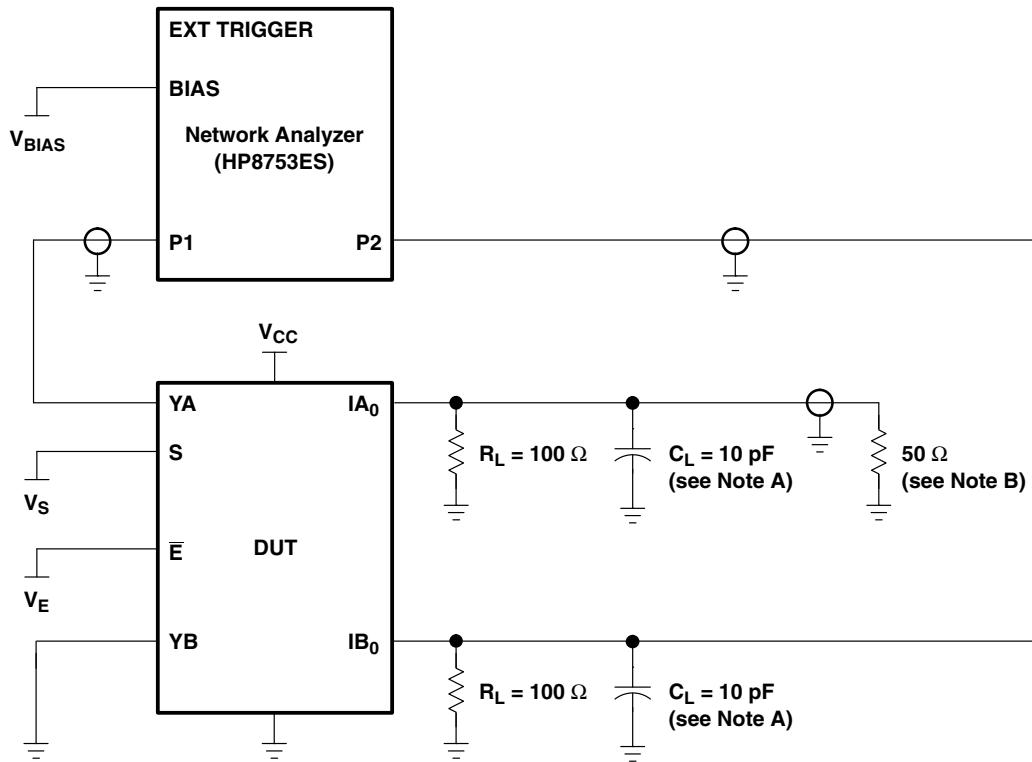
NOTES: A. C_L includes probe and jig capacitance.
        B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

Figure 8. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_S = 0$, $V_E = 0$, and YA is the input, the output is measured at IB_0. All unused analog input (Y) ports are connected to GND, and output (I) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES setup

    Average = 4
    RBW = 3 kHz
    V_{BIAS} = 0.35 V
    ST = 2 s
    P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION
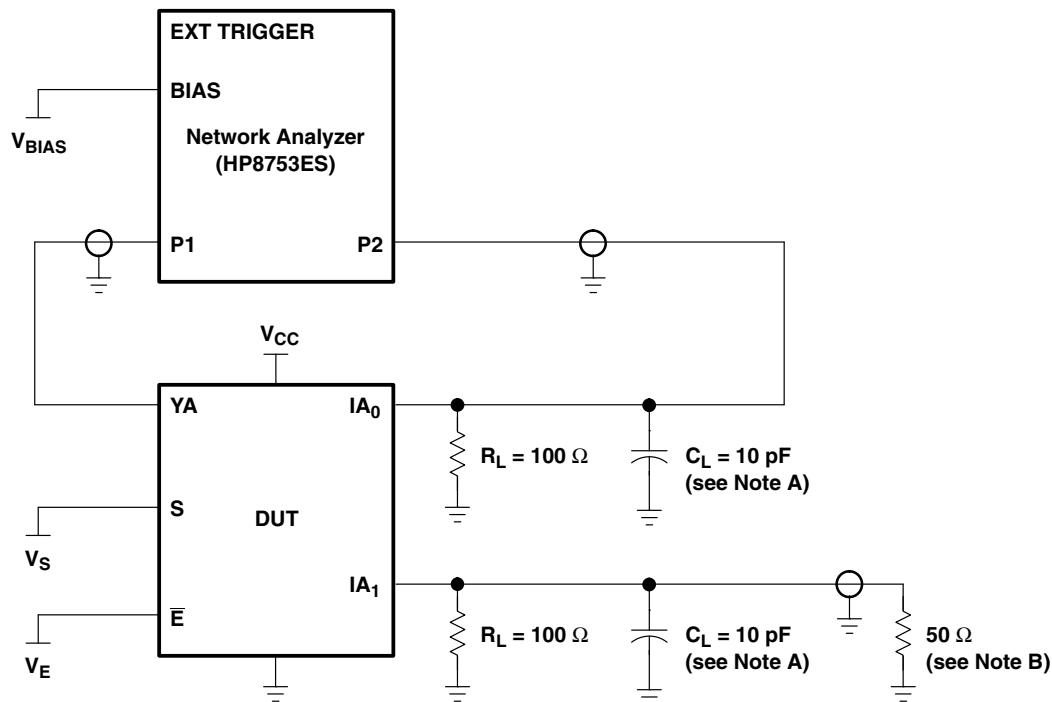
NOTES: A. C_L includes probe and jig capacitance.
        B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

Figure 9. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when $V_S = V_{CC}$, $V_E = 0$, and YA is the input, the output is measured at IA_0. All unused analog input (Y) ports are left open, and output (I) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBm

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TS3L110D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TS3L110DBQRE4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TS3L110DBQRG4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TS3L110DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110DGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110DGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TS3L110PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3L110RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TS3L110RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
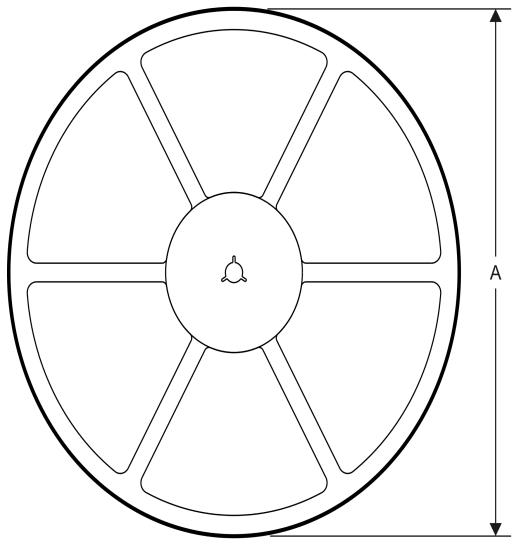
TAPE DIMENSIONS
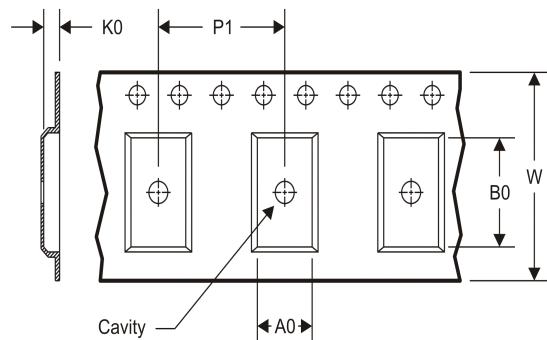
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
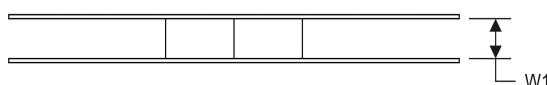
TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3L110DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
TS3L110DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TS3L110PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3L110RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3L110DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
TS3L110DR	SOIC	D	16	2500	333.2	345.9	28.6
TS3L110PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TS3L110RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN
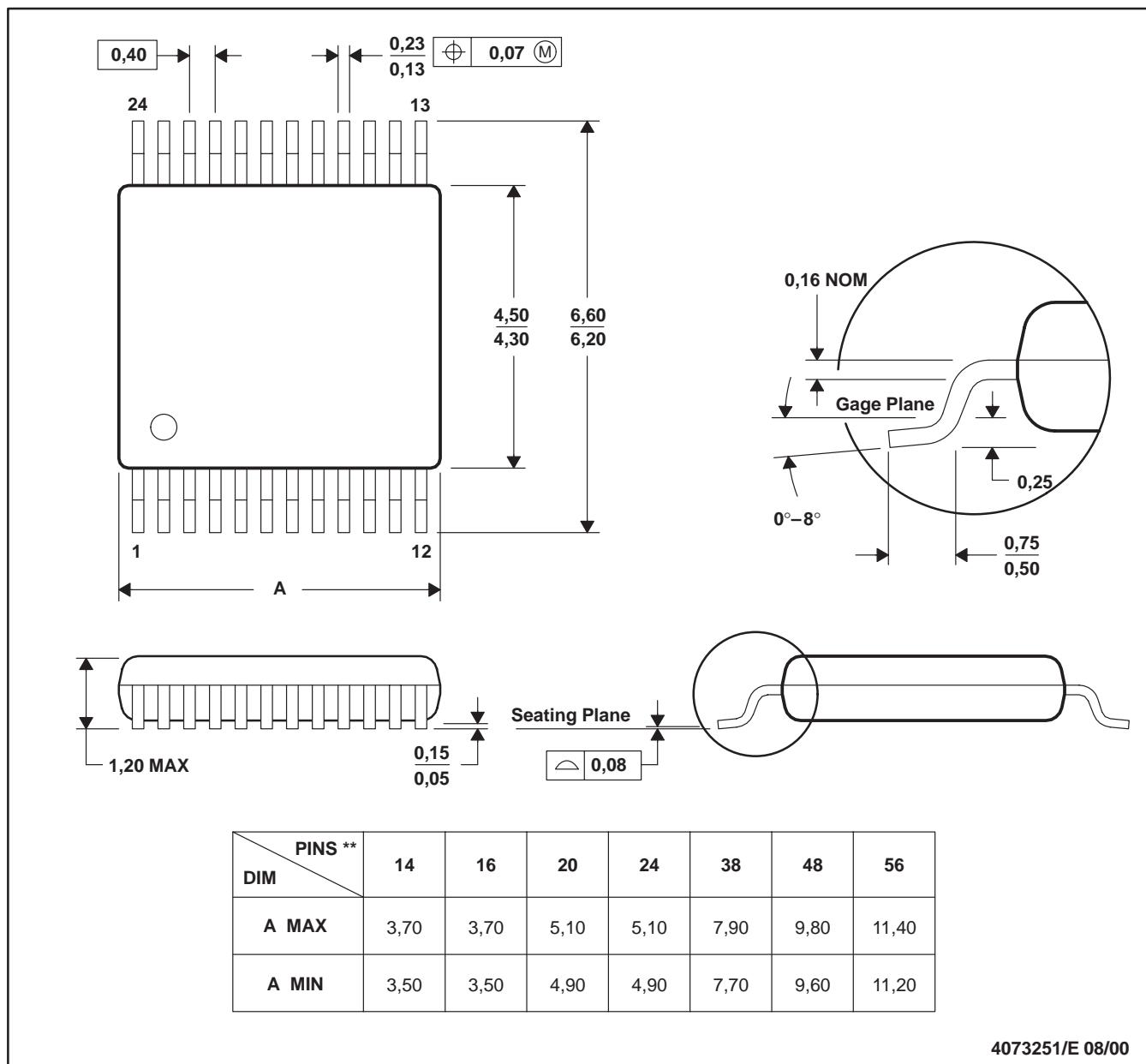
PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
           B. This drawing is subject to change without notice.
           C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
           D. Falls within JEDEC: 24/48 Pins – MO-153
                                14/16/20/56 Pins – MO-194

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE
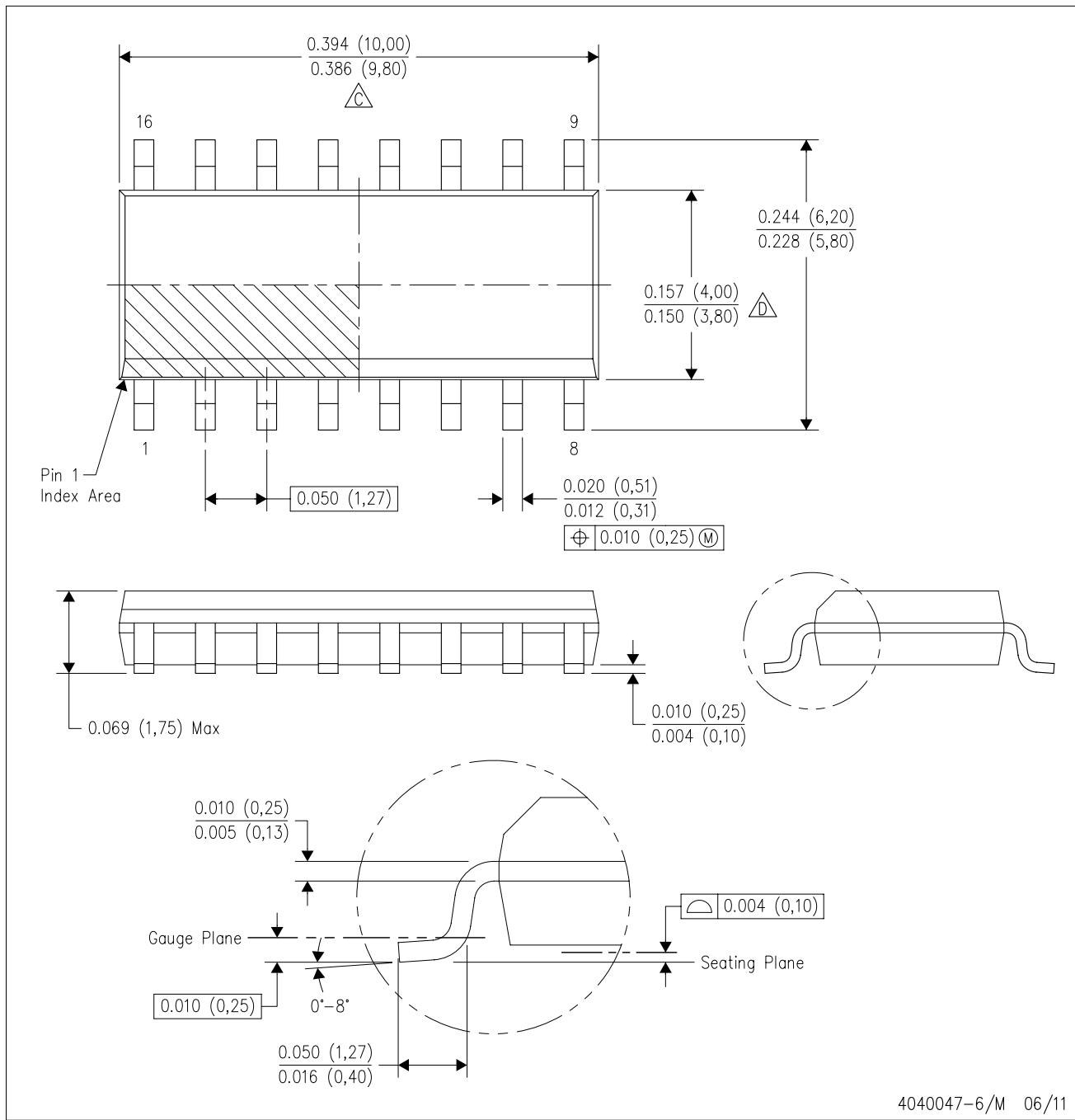
0.394 (10,00)
0.386 (9,80)
⟨C⟩

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⟨D⟩

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         ⟨C⟩ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
         ⟨D⟩ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AC.

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PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

16   9

⬦D 4,50
4,30

6,60
6,20

1   8

5,10
4,90

△C

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ 0,10
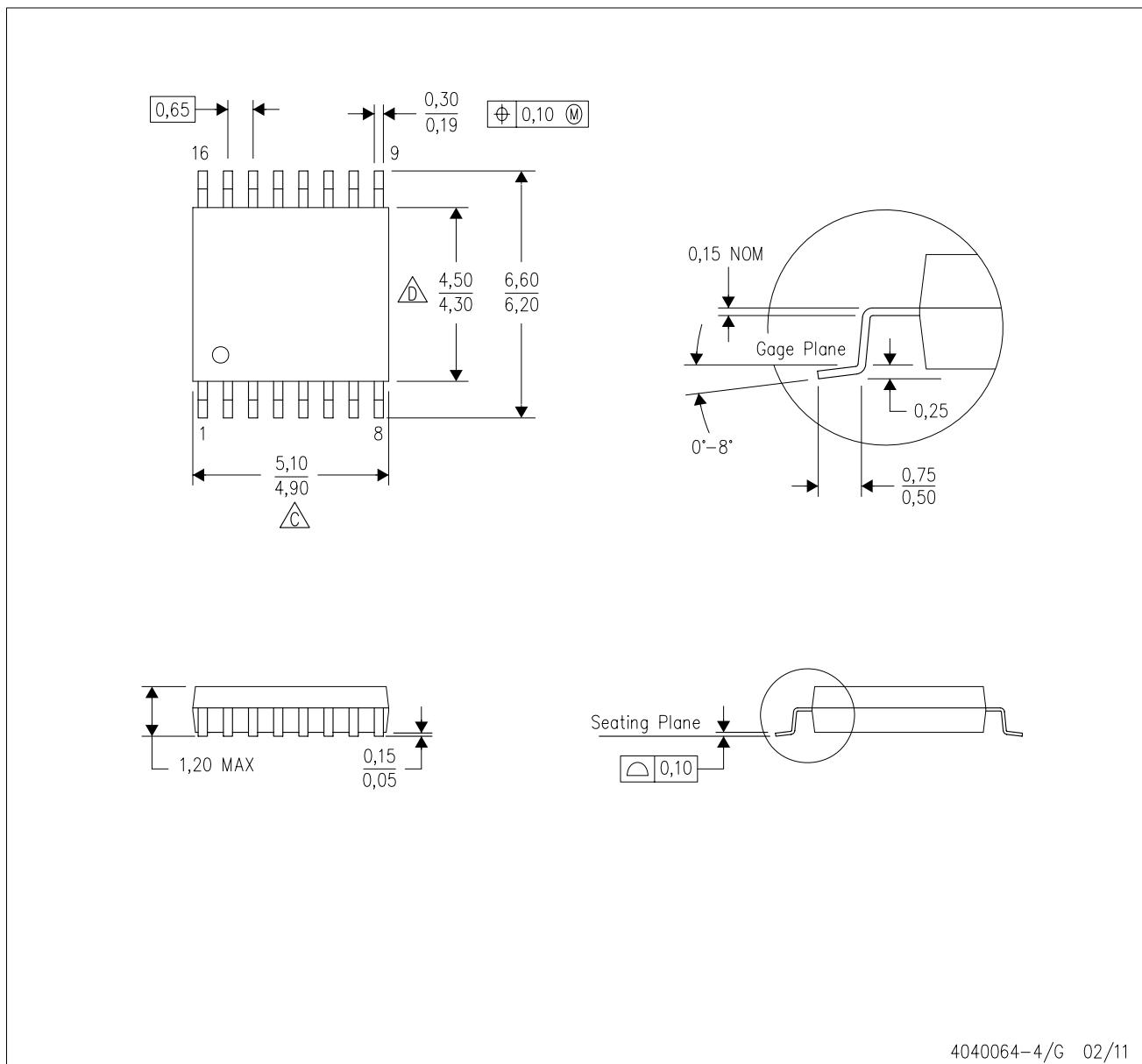
4040064−4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
        △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0,15 each side.
        △D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E. Falls within JEDEC MO−153

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

←─14x0,65

5,60

Stencil Openings
(Note D)

←─16x0,30

←─14x0,65

16x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

Example
Solder Mask Opening
(See Note E)

0,07
All Around
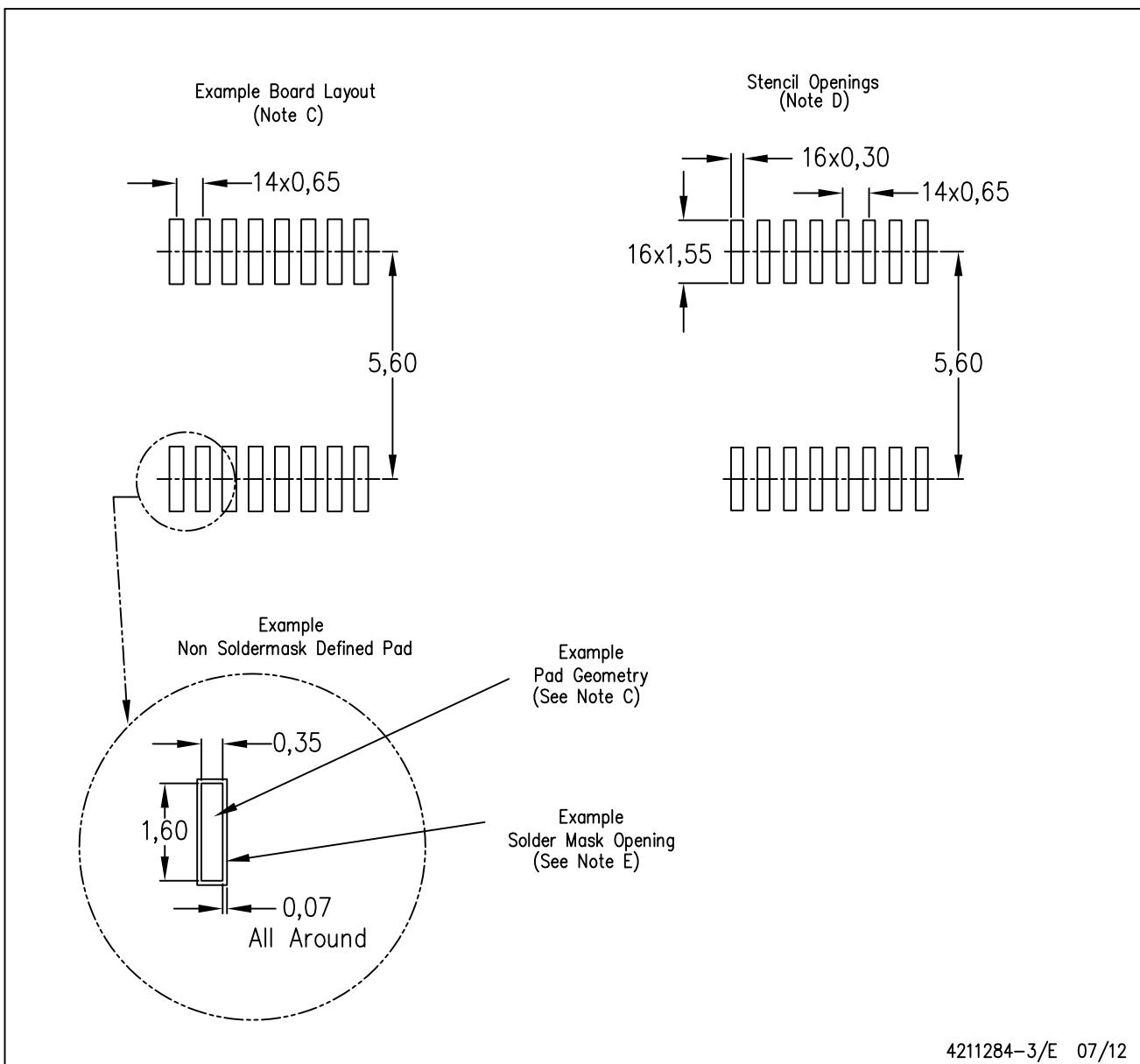
4211284−3/E 07/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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RGY (R-PVQFN-N16)   PLASTIC QUAD FLATPACK NO-LEAD

$\frac{4,15}{3,85}$ A

B

15   10

16   9

$\frac{3,65}{3,35}$

1   8

Pin 1 Index Area
Top and Bottom

2   7

F

0,20 Nominal
Lead Frame

$\frac{1,00}{0,80}$

Seating Plane

0,08 C

$\frac{0,05}{0,00}$
Seating Height

C

2,50

0,50

16X $\frac{0,50}{0,30}$

2   7

1   THERMAL PAD   8

1,50   SIZE AND SHAPE
SHOWN ON SEPRATE SHEET

16   9

15   10

16X $\frac{0,30}{0,18}$

⊕	0,10 Ⓜ	C	A	B
	0,05 Ⓜ	C		
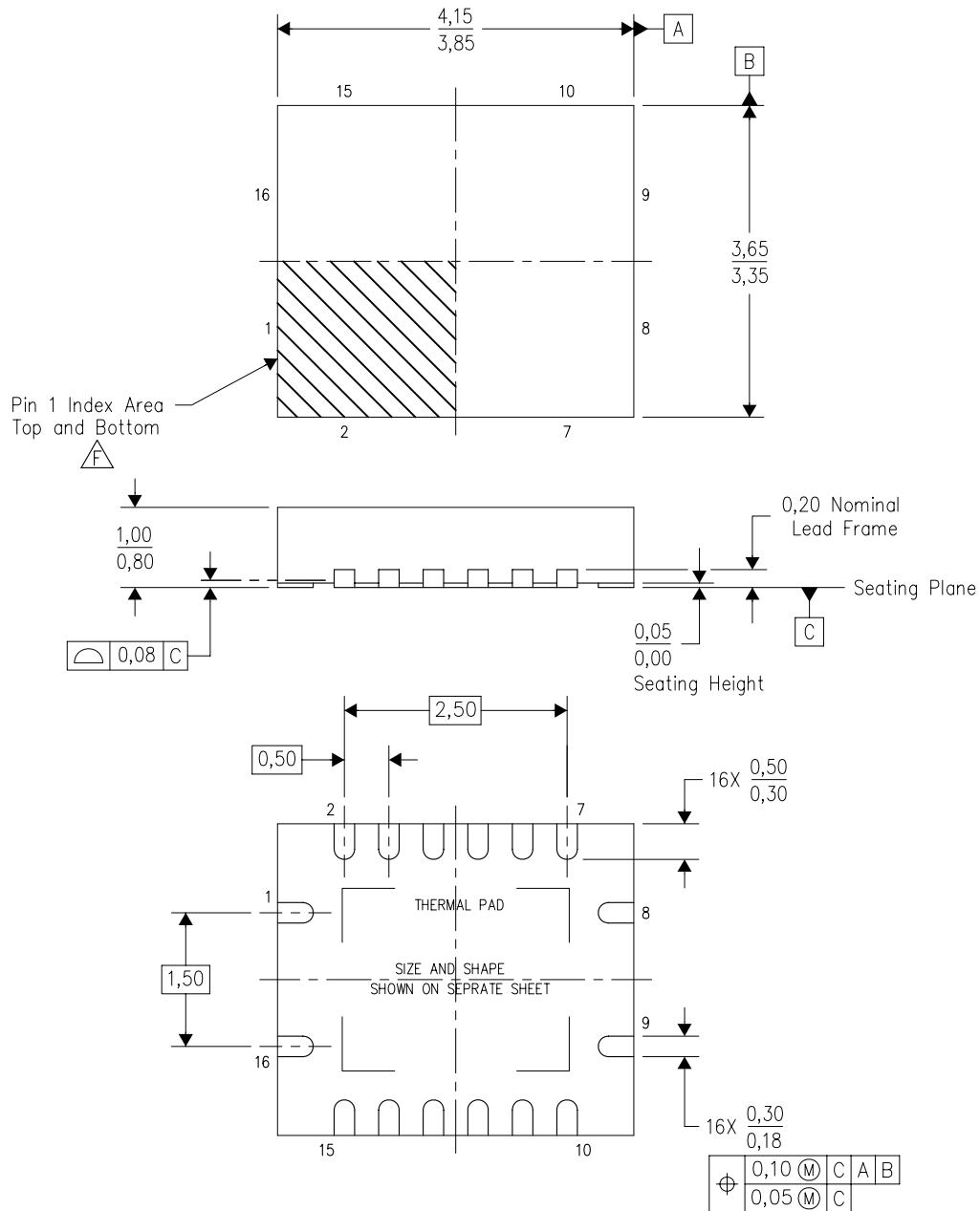
Bottom View   4203539-3/I   06/2011

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
          B.   This drawing is subject to change without notice.
          C.   QFN (Quad Flatpack No-Lead) package configuration.
          D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
          E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
          F.   Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
                The Pin 1 identifiers are either a molded, marked, or metal feature.
          G.   Package complies to JEDEC MO-241 variation BA.

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RGY (R−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
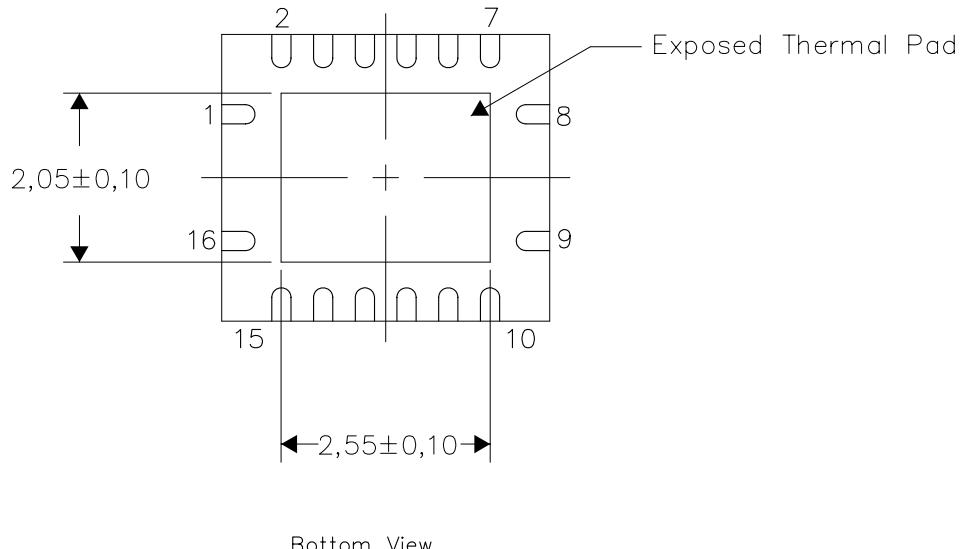

Bottom View

Exposed Thermal Pad Dimensions

4206353−3/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)   PLASTIC QUAD FLATPACK NO-LEAD

Example Board Layout

4,80

4,30

2,60

1,50

2,55

2,05

Note D

0,85 X 16 PL.

0,28 X 16 PL.

10x0,50

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4,75

4,25

2,65

1,50

0,82

1,07

0,30 x 2 PL.

0,80 x 16 PL.

0,23 x 16 PL.

10x0,50

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,28

0,07

All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

1,00

1,00

6x∅0,3

4208122-3/0 11/11
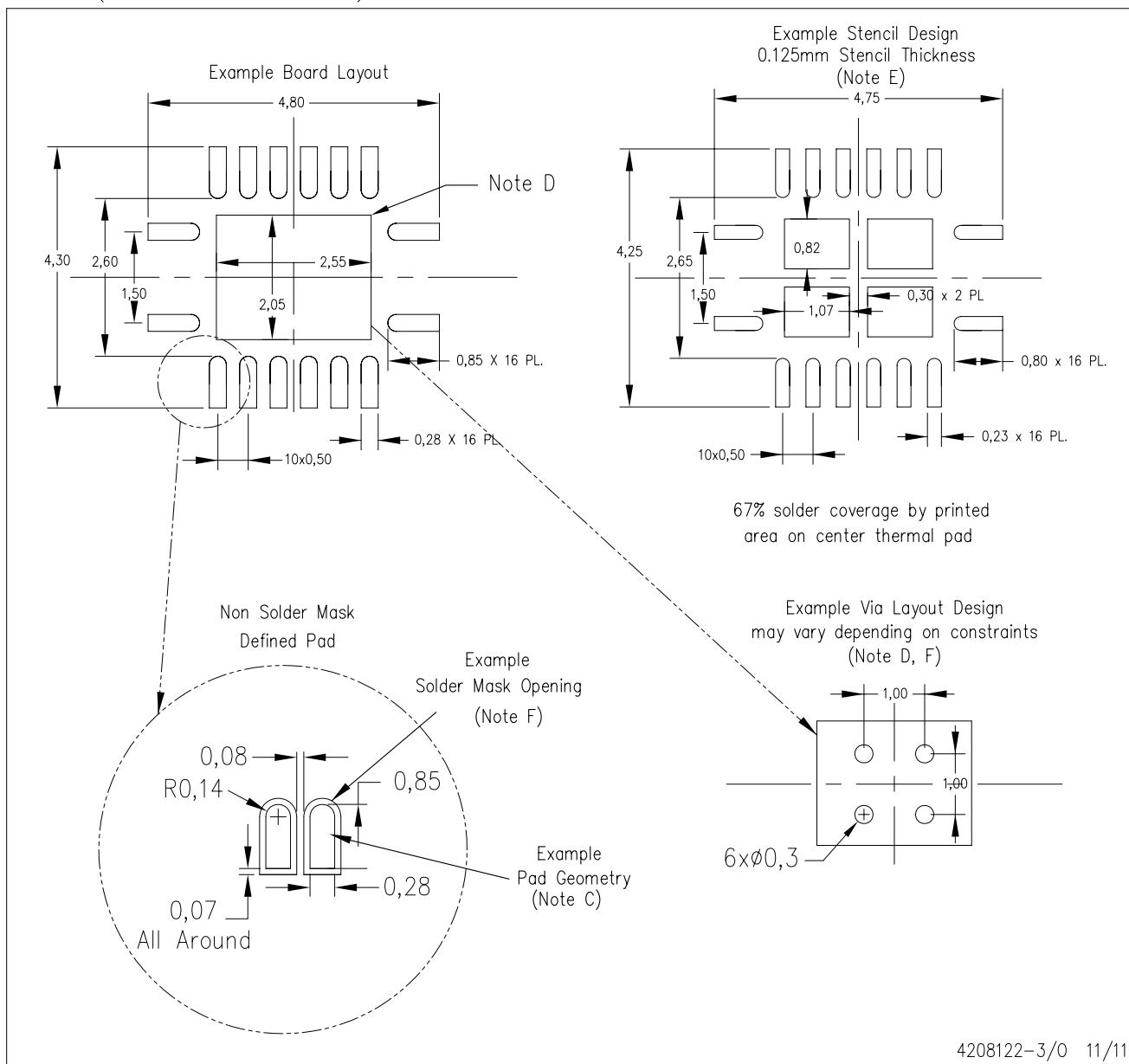
NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC-7351 is recommended for alternate designs.
         D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack
             QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
             for specific thermal information, via requirements, and recommended board layout.
             These documents are available at www.ti.com <http://www.ti.com>.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
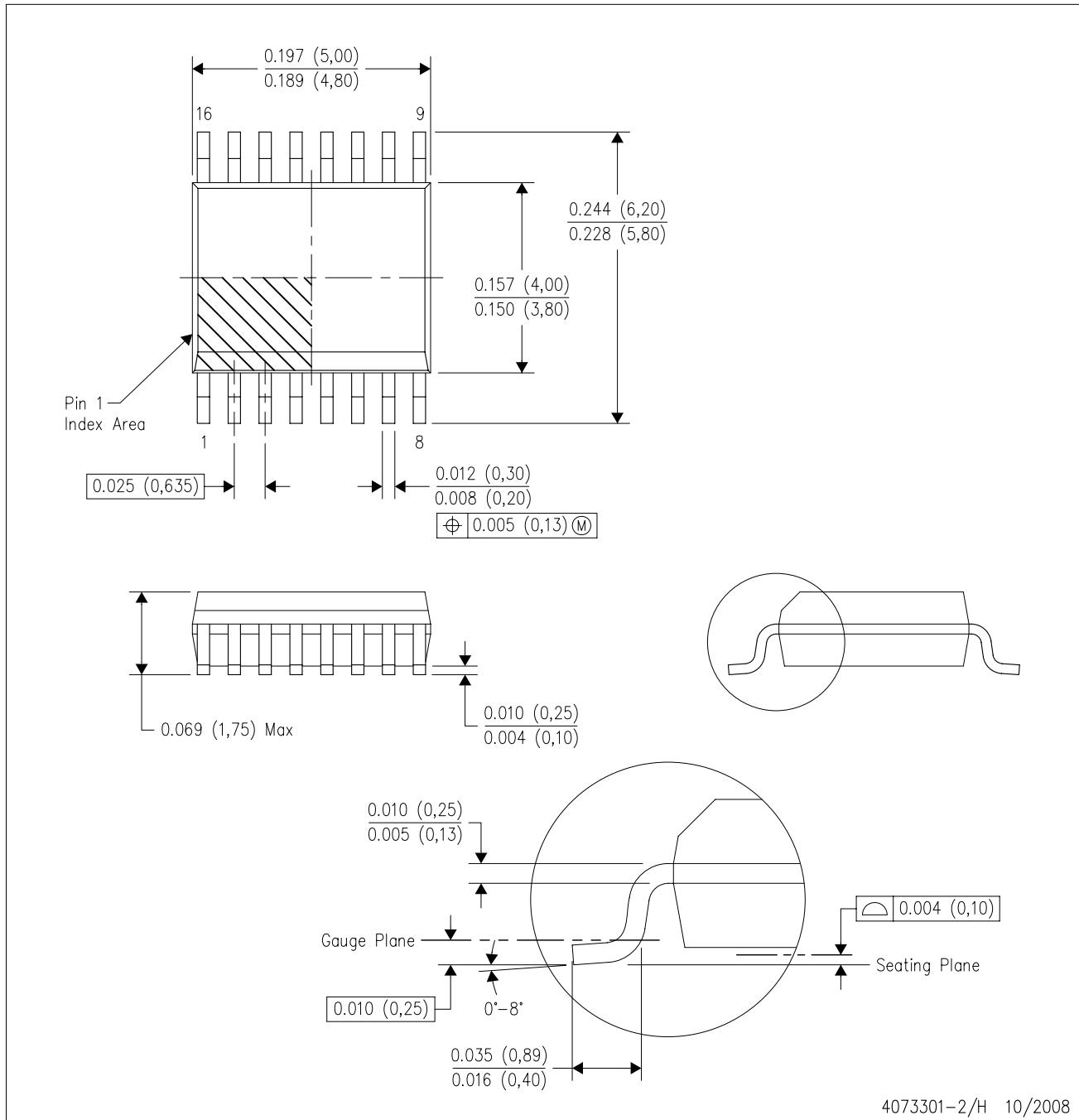
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DBQ (R−PDSO−G16)   PLASTIC SMALL−OUTLINE PACKAGE

0.197 (5,00)
0.189 (4,80)

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

Pin 1
Index Area

1   8

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.035 (0,89)
0.016 (0,40)

4073301−2/H   10/2008

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
        D. Falls within JEDEC MO−137 variation AB.

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DBQ (R−PDSO−G16)   PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

16x0,35 →| |← →| |←−14x0,635

5,2

16x0,3 →| |← →| |←−14x0,635

16x1,75

5,2

0,35

Solder Mask Opening

1,90   1,8

Pad Geometry

0,05

0,40
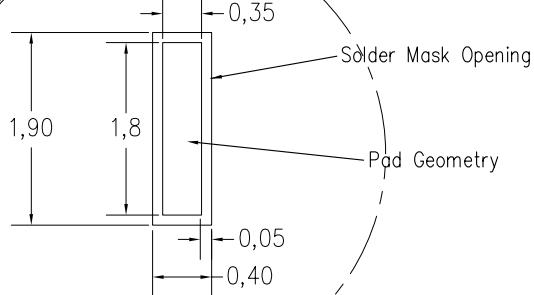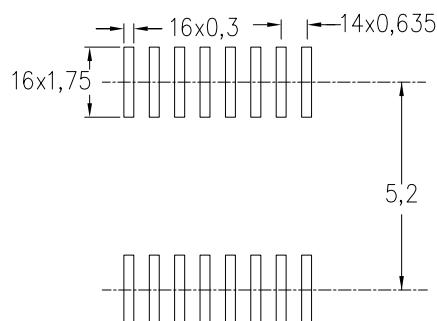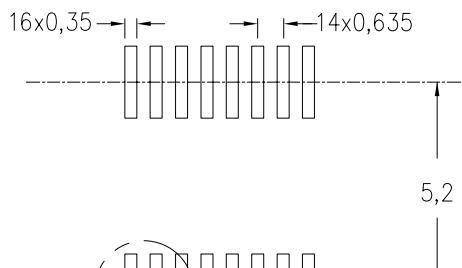
4210335−2/C 07/11

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
          D. Publication IPC−7351 is recommended for alternate designs.
          E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
              metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

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