

QUARTZ CRYSTAL OSCILLATOR

■ GENERAL DESCRIPTION

The NJU6323 series is a C-MOS quartz crystal oscillator which consists of an oscillation amplifier, 3-stage divider, output frequency selector and 3-state output buffer.

The oscillation frequency is as wide as up to 50MHz and the symmetry of 45-55% is realized over full oscillation frequency range.

The oscillation amplifier incorporates feed-back resistance and oscillation capacitors(Cg, Cd), therefore, it requires no external component except quartz crystal.

The 3-stage divider outputs f_0 , $f_0/2$, $f_0/4$ and $f_0/8$ to the output frequency selector and it determined one output frequency according to the combination of two input-signal.

The 3-state output buffer is C-MOS compatible and capable of 10 LSTTL driving.

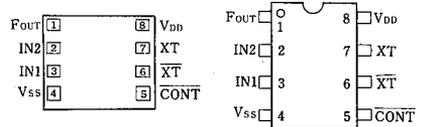
■ PACKAGE OUTLINE


NJU6323XC



NJU6323XE

4

■ PIN CONFIGURATION/PAD LOCATION

■ FEATURES

- Operating Voltage -- 3.0~6.0V
- Maximum Oscillation Frequency -- 50MHz
- Low Operating Current
- High Fan-out -- LSTTL 10
- 3-state Output Buffer
- Selected Frequency Output (mask option)
Only one frequency out of f_0 , $f_0/2$, $f_0/4$ and $f_0/8$ output
- Oscillation Capacitors Cg and Cd on-chip
- Oscillation and/or Output Stand-by Function
- Package Outline -- CHIP/EMP 8
- C-MOS Technology

■ COORDINATES

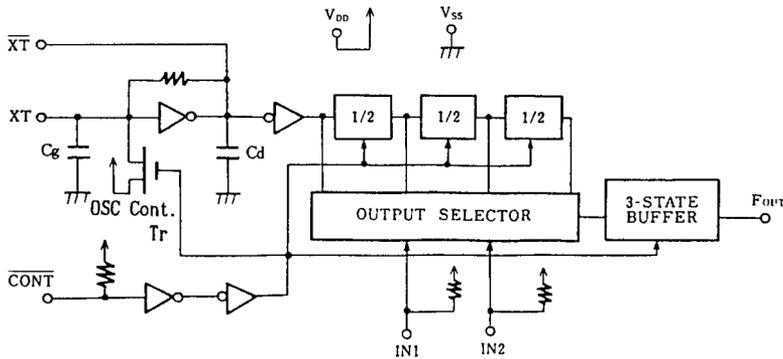
 Unit: μm

No.	PAD	X	Y
1	F _{OUT}	165	651
2	IN ₂	165	484
3	IN ₁	165	317
4	V _{SS}	165	149
5	CONT	1113	149
6	XT	1113	317
7	XT	1113	484
8	V _{DD}	1113	651

Chip Size : 1.28 X 0.8mm

 Chip Thickness : 400 μm ±30 μm
■ LINE-UP TABLE

Type No.	Cg	Cd	Osc.Stop Function
NJU6323	21pF	23pF	Yes
NJU6323J	21pF	No	Yes
NJU6323P	No	No	Yes

■ BLOCK DIAGRAM

■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N			
5	$\overline{\text{CONT}}$	Oscillation Stop Control and Divider Reset			
		$\overline{\text{CONT}}$ F_{OUT}			
		H Output either one frequency from f_0 , $f_0/2$, $f_0/4$, and $f_0/8$			
		L Oscillation Stop, Output High Impedance and Divider Reset			
6	$\overline{\text{XT}}$	Quartz Crystal Connecting Terminals			
7	XT				
8	V_{DD}	+ 5V			
3	IN1	3-Stage Divider Outputs Selected by IN1 and IN2			
2	IN2		IN1	IN2	F_{OUT}
			H	H	f_0
			L	H	$f_0/2$
			H	L	$f_0/4$
L	L	$f_0/8$			
1	F_{OUT}	Output either one frequency from f_0 , $f_0/2$, $f_0/4$, and $f_0/8$			
4	V_{SS}	GND			

■ ABSOLUTE MAXIMUM RATINGS

 ($T_a=25^\circ\text{C}$)

P A R A M E T E R	S Y M B O L	R A T I N G S	U N I T
Supply Voltage	V_{DD}	-0.5 ~ +7.0	V
Input Voltage	V_{IN}	-0.5 ~ $V_{\text{DD}}+0.5$	V
Output Voltage	V_o	-0.5 ~ $V_{\text{DD}}+0.5$	V
Input Current	I_{IN}	± 10	mA
Output Current	I_o	± 25	mA
Power Dissipation (EMP)	P_D	200	mW
Operating Temperature Range	T_{opr}	-40 ~ + 85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 ~ +150	$^\circ\text{C}$

(Note) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the circuit.

■ ELECTRICAL CHARACTERISTICS

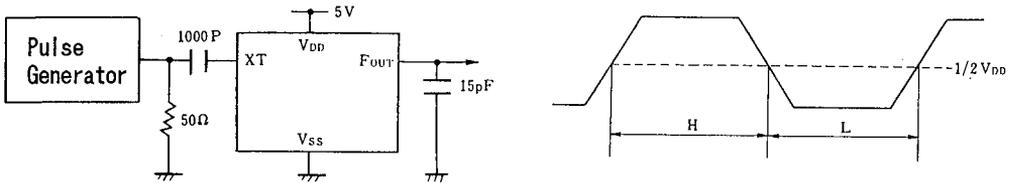
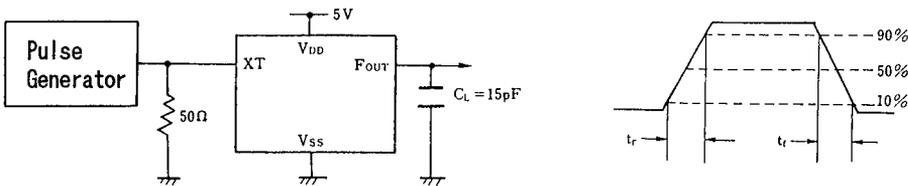
 ($T_a=25^{\circ}\text{C}$, $V_{DD}=5\text{V}$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}		3		6	V
Operating Current	I_{DD}	fosc=16MHz, No load			10	mA
Stand-by Current	I_{st}	CONT, XT= V_{SS} , No load (Note)			1	μA
Input Voltage	V_{IH}		3.5		5.0	V
	V_{IL}		0		1.5	
Output Current	I_{OH}	$V_{DD}=5\text{V}$, $V_{OH}=4.5\text{V}$	4			mA
	I_{OL}	$V_{DD}=5\text{V}$, $V_{OL}=0.5\text{V}$	4			
Input Current	I_{IN}	CONT, IN1, IN2 Terminals CONT, IN1, IN2= V_{SS}			400	μA
Internal Capacitor	C_g	Refer to Line-Up Table.				pF
	C_d					
Max. Oscillation Freq.	f_{MAX}	$V_{DD}=5\text{V}$, $C_L=15\text{pF}$	50			MHz
Output Signal Symmetry	SYM	$V_{DD}=5\text{V}$, $C_L=15\text{pF}$ at $1/2V_{DD}$	45	50	55	%
Output Signal Rise Time	t_r	$V_{DD}=5\text{V}$, $C_L=15\text{pF}$, 10% - 90%			8	ns
Output Signal Fall Time	t_f	$V_{DD}=5\text{V}$, $C_L=15\text{pF}$, 90% - 10%			8	ns

Note) Excluding input current on CONT terminal.

4

■ MEASUREMENT CIRCUITS

 (1) Output Signal Symmetry ($C_L=15\text{pF}$)

 (2) Output Signal Rise/Fall Time ($C_L=15\text{pF}$)


NJU6323 Series

MEMO

[CAUTION]

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