OptiMOS®2 Power-Transistor

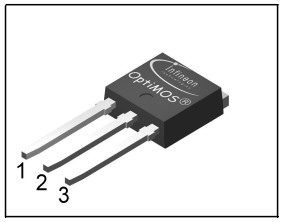
Feature

- Ideal for high-frequency dc/dc converters
- n-Channel
- Logic Level
- Excellent Gate Charge x $R_{DS(on)}$ product (FOM)
- Low On-Resistance $R_{DS(on)}$
- Superior thermal resistance
- 175°C operating temperature
- d*v*/d*t* rated

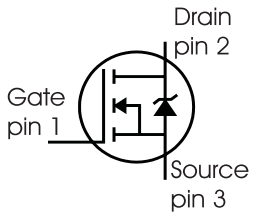
Product Summary

V_{DS}	25	V
$R_{DS(on)}$	12.8	mΩ
I_D	30	A

P- TO251 -3-1



Type	Package	Ordering Code	Marking
IPU13N03LA	P- TO251 -3-1	Q67042-S4160	13N03LA



Maximum Ratings, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current	I_D		A
T_C=25°C[1)]		30	
T_C=100°C		30	
Pulsed drain current	$I_{D\ puls}$	210	
T_C=25°C[2)]			
Avalanche energy, single pulse	E_{AS}	60	mJ
I_D=30A, V_{DD}=25V, R_{GS}=25Ω			
Reverse diode d*v*/d*t*	d*v*/d*t*	6	kV/µs
I_S=30A, V_{DS}=20V, d*i*/d*t*=200A/µs, T_{jmax}=175°C			
Gate source voltage[3)]	V_{GS}	±20	V
Power dissipation	P_{tot}	47	W
T_C=25°C			
Operating and storage temperature	T_j , T_{stg}	-55... +175	°C
IEC climatic category; DIN IEC 68-1		55/175/56	

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Thermal Characteristics					
Thermal resistance, junction - case	R_{thJC}	-	-	3.2	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	100	
SMD version, device on PCB:	R_{thJA}				
@ min. footprint		-	-	75	
@ 6 cm^2 cooling area [4)]		-	-	50	
Electrical Characteristics, at T_j = 25 °C, unless otherwise specified					
Static Characteristics					
Drain-source breakdown voltage V_{GS}=0V, I_D=1mA	$V_{(BR)DSS}$	25	-	-	V
Gate threshold voltage, V_{GS} = V_{DS} I_D = 20 µA	$V_{GS(th)}$	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}				
V_{DS}=25V, V_{GS}=0V, T_j=25°C		-	0.1	1	µA
V_{DS}=25V, V_{GS}=0V, T_j=150°C		-	10	100	-
Gate-source leakage current V_{GS}=20V, V_{DS}=0V	I_{GSS}	-	10	100	nA
Drain-source on-state resistance V_{GS}=4.5V, I_D=20A	$R_{DS(on)}$	-	17.5	21.9	mΩ
Drain-source on-state resistance V_{GS}=10V, I_D=30A	$R_{DS(on)}$	-	10.7	12.8	
Gate resistance	R_G	-	0.9	-	Ω

[1]Current limited by bondwire; with a R_{thJC} = 3.2K/W the chip is able to carry I_D= 47A.

[2]See figure 3.

[3]T_{jmax}=150°C for V_{GS}<-5V

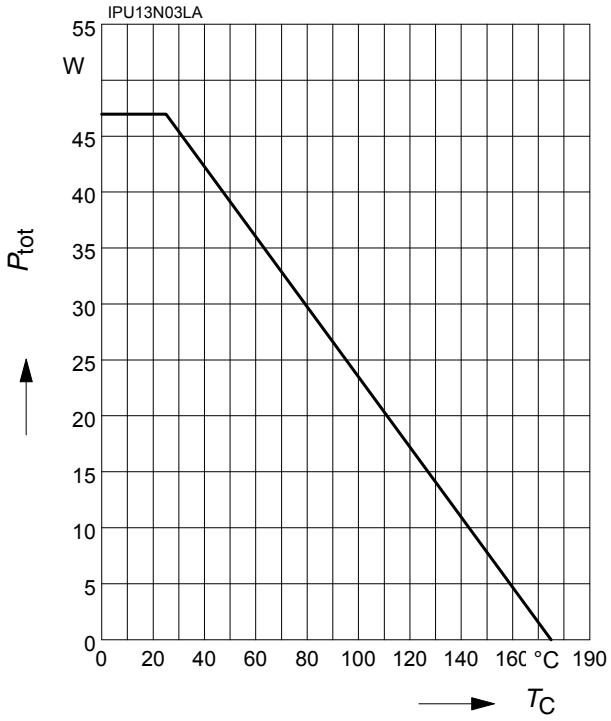
[4]Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical without blown air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Characteristics						
Transconductance	g_{fs}	$V_{DS}\geq 2*I_D*R_{DS(on)max}$, I_D=30A	19	38	-	S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=15V, f=1MHz	-	857	1139	pF
Output capacitance	C_{oss}		-	387	514	
Reverse transfer capacitance	C_{rss}		-	69	104	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15V, V_{GS}=10V, I_D=15A, R_G=2.7Ω	-	6.6	9.9	ns
Rise time	t_r		-	14.5	22	
Turn-off delay time	$t_{d(off)}$		-	18.4	27.6	
Fall time	t_f		-	3.4	5.1	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=15V, I_D=15A	-	2.4	3.2	nC
Gate charge at threshold	$Q_{G(th)}$		-	1.3	2	
Gate to drain charge	Q_{gd}		-	2.6	3.9	
Switching Charge [1)]	Q_{sw}		-	3.7	5.6	
Gate charge total	Q_g	V_{DD}=15V, I_D=15A, V_{GS}=0 to 5V	-	8.2	10.6	
Output charge	Q_{oss}	V_{DS}=15V, I_D=15A, V_{GS}=0V	-	8.2	10.6	
Gate Charge total, Sync. FET	$Q_{g(sync)}$	V_{GS}=0 to 5V, V_{DS}=0.1V	-	6.7	8.9	
Gate plateau voltage	$V_{(plateau}$	V_{DD}=15V, I_D=15A	-	3	-	V
Reverse Diode						
Inverse diode continuous forward current	I_S	T_C=25°C	-	-	30	A
Inv. diode direct current, pulsed	I_{SM}		-	-	210	
Inverse diode forward voltage	V_{SD}	V_{GS}=0V, I_F=30A	-	1	1.3	V
Reverse recovery charge	Q_{rr}	V_R=-V, I_F=I_S, di_F/dt=400A/µs	-	-	<10	nC

[1] See figure 16

1 Power dissipation

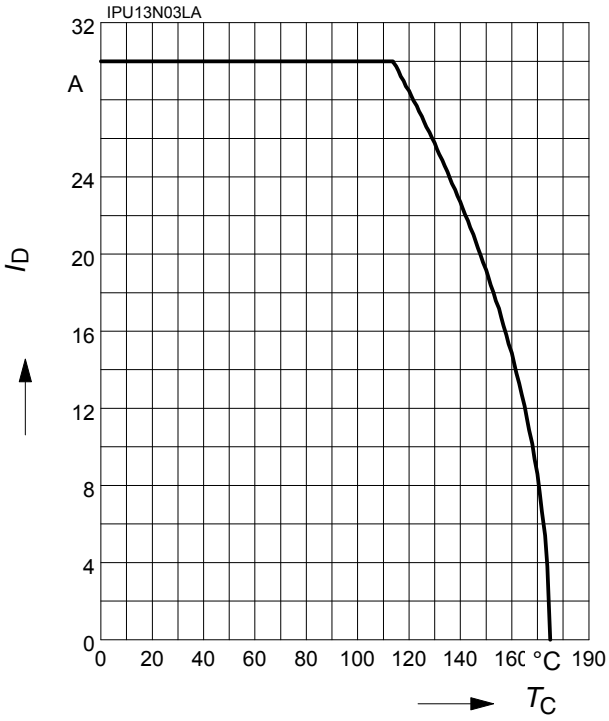
$P_{tot} = f(T_C)$



2 Drain current

$I_D = f(T_C)$

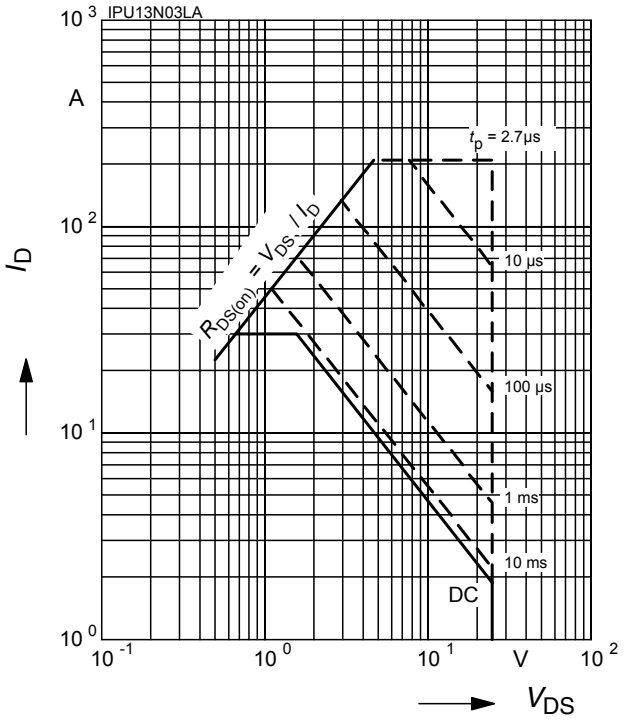
parameter: $V_{GS} \geq 10$ V



3 Safe operating area

$I_D = f(V_{DS})$

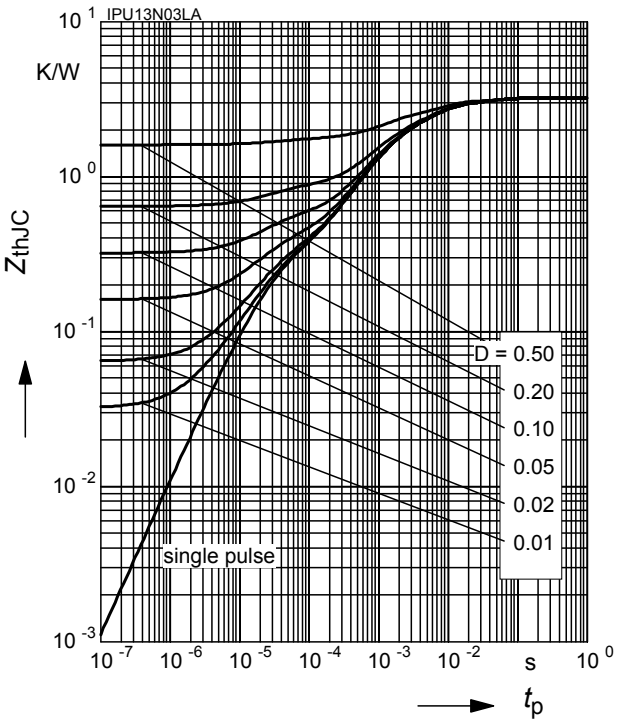
parameter : $D = 0$, $T_C = 25$ °C



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

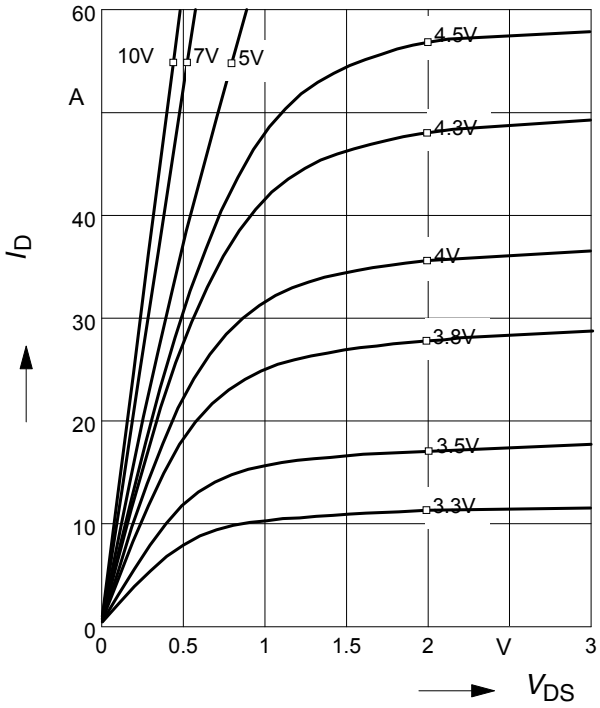
parameter : $D = t_p/T$



5 Typ. output characteristic

$I_D = f(V_{DS})$; T_j=25°C

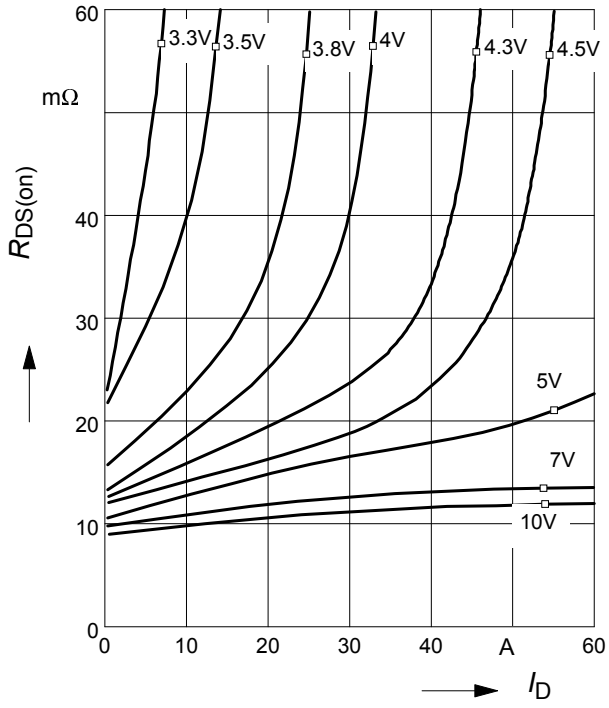
parameter: t_p = 80 µs



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D)$

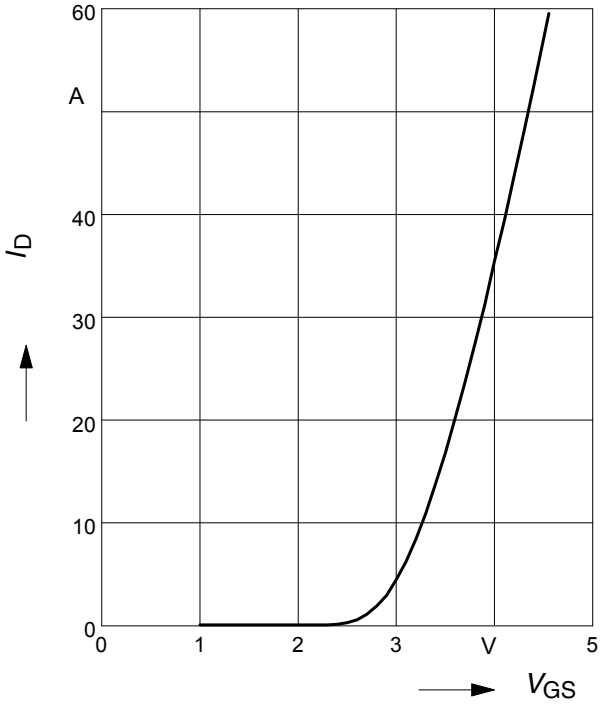
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$

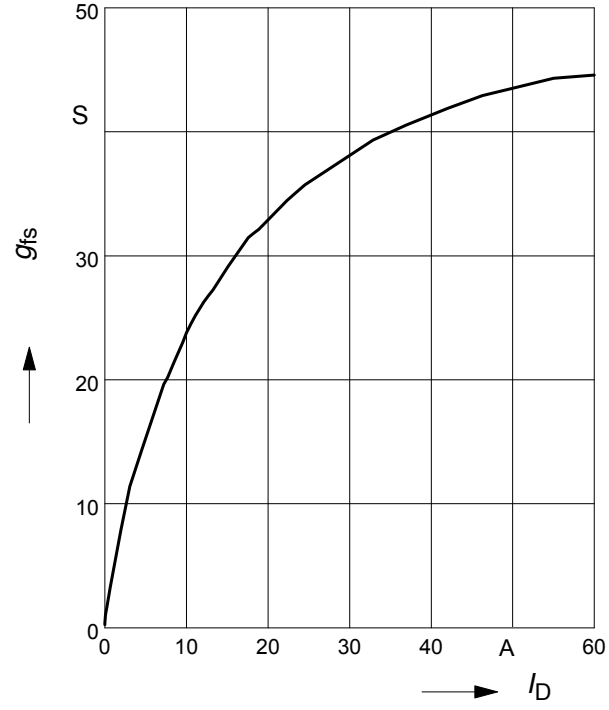
parameter: t_p = 80 µs



8 Typ. forward transconductance

g_{fs} = f(I_D); T_j=25°C

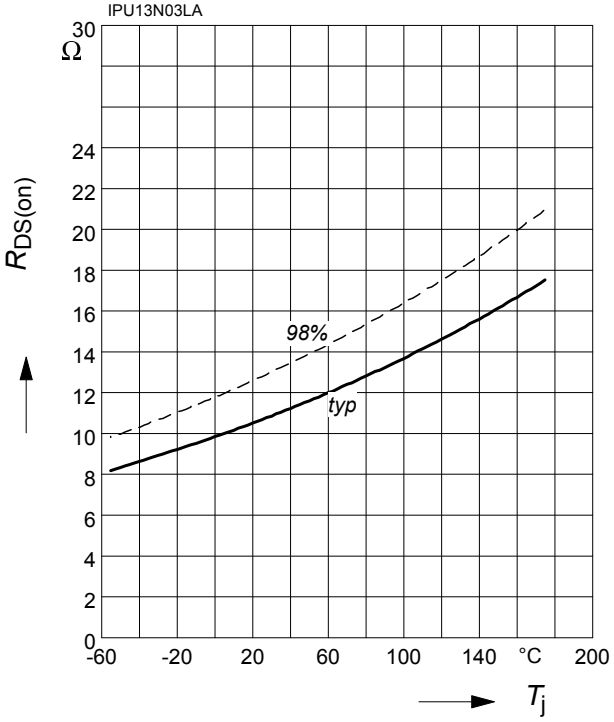
parameter: g_{fs}



9 Drain-source on-state resistance

$R_{DS(on)} = f(T_j)$

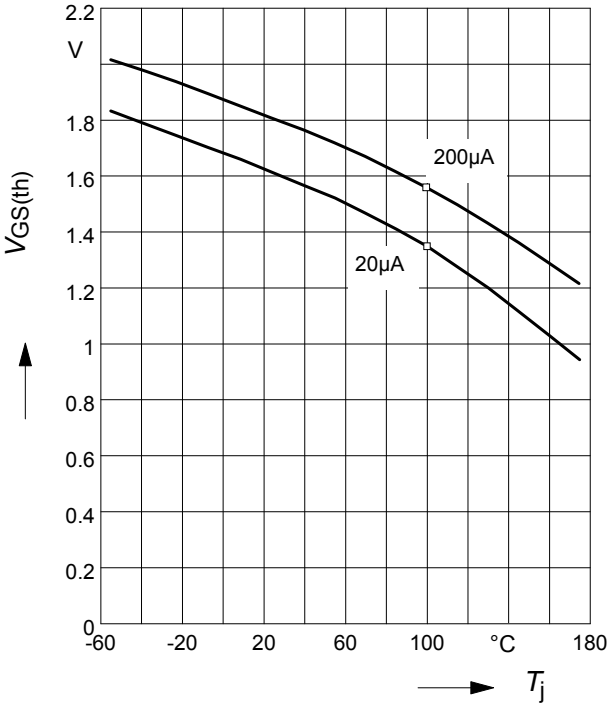
parameter : I_D = 30 A, V_{GS} = 10 V



10 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$

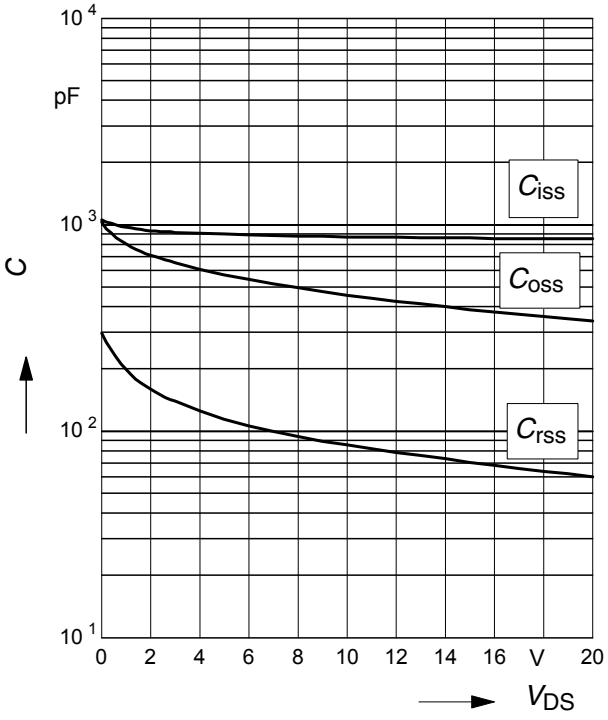
parameter: $V_{GS} = V_{DS}$



11 Typ. capacitances

$C = f(V_{DS})$

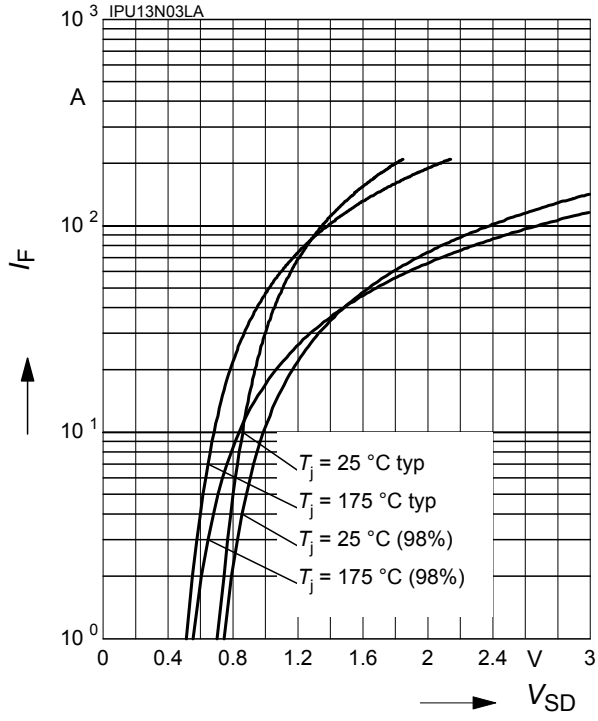
parameter: V_{GS}=0V, f=1 MHz



12 Forward character. of reverse diode

$I_F = f(V_{SD})$

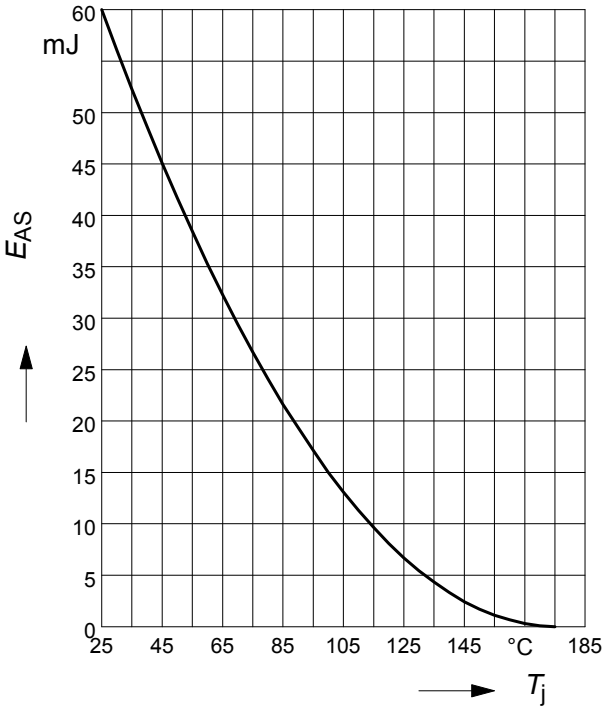
parameter: T_j , tp = 80 µs



13 Typ. avalanche energy

$E_{AS} = f(T_j)$

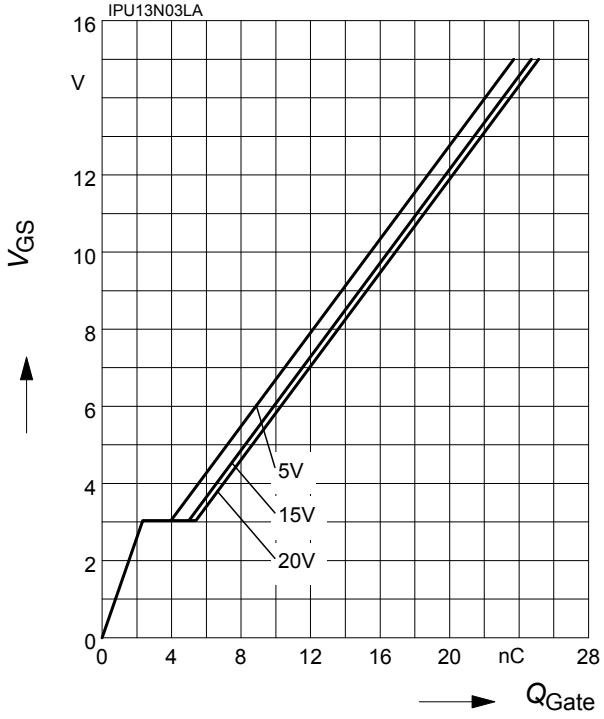
par.: I_D = 30 A, V_{DD} = 25 V, R_{GS} = 25 Ω



14 Typ. gate charge

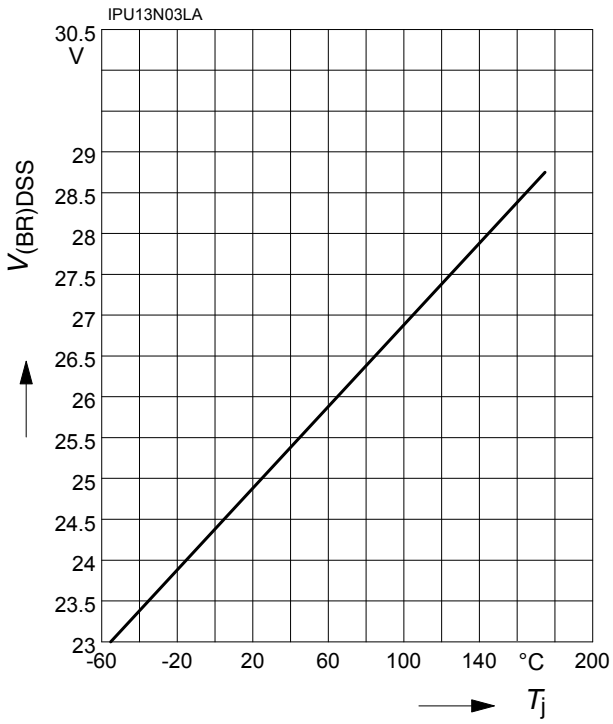
$V_{GS} = f(Q_{Gate})$

parameter: I_D = 15 A pulsed



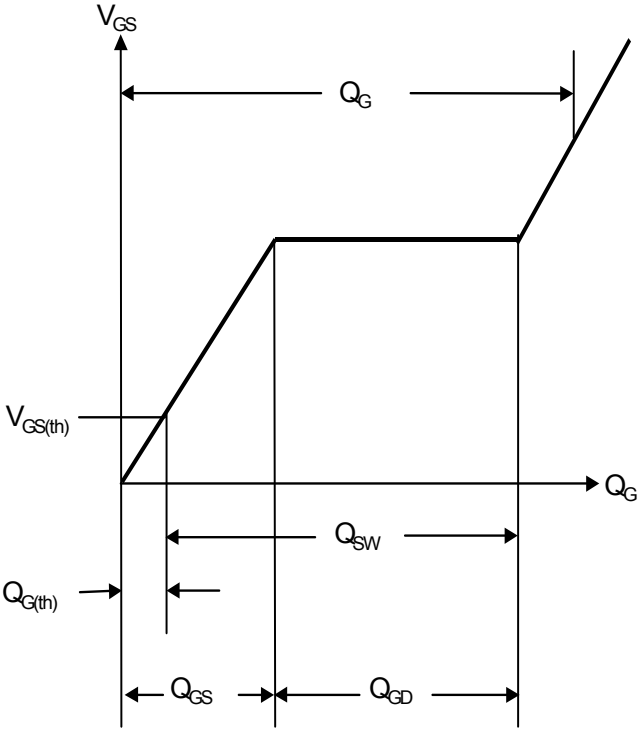
15 Drain-source breakdown voltage

$V_{(BR)DSS} = f(T_j)$



16 Gate Charge Waveforms

V_{GS}=5V, V_{DS}=15V



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