

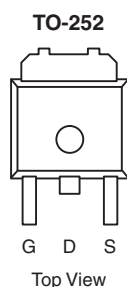
N-Channel 250-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
250	0.165 at $V_{GS} = 10$ V	17

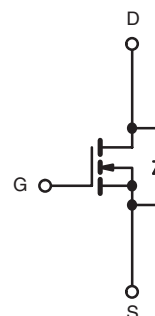
FEATURES

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature


RoHS
COMPLIANT


Drain Connected to Tab

Ordering Information: SUD17N25-165-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	250	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C) ^b	I_D	$T_C = 25$ °C	A
		$T_C = 125$ °C	
Pulsed Drain Current	I_{DM}	20	
Continuous Source Current (Diode Conduction)	I_S	17	
Single Pulse Avalanche Current	I_{AS}	5	
Single Pulse Avalanche Energy	E_{AS}	1.25	mJ
Maximum Power Dissipation	P_D	$T_C = 25$ °C	W
		$T_A = 25$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient ^a	R_{thJA}	15	18	°C/W
		40	50	
Junction-to-Case (Drain)	R_{thJC}	0.85	1.1	

Notes:

a. Surface Mounted on 1" x 1" FR4 Board.

b. See SOA curve for voltage derating.



SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ ^a	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	250			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.5		4.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 250\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 250\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$			50	
		$V_{DS} = 250\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 175\text{ }^{\circ}\text{C}$			250	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 15\text{ V}$, $V_{GS} = 10\text{ V}$	17			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 14\text{ A}$		0.131	0.165	Ω
		$V_{GS} = 10\text{ V}$, $I_D = 14\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$			0.347	
		$V_{GS} = 10\text{ V}$, $I_D = 14\text{ A}$, $T_J = 175\text{ }^{\circ}\text{C}$			0.462	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 17\text{ A}$		36		S
Dynamic ^a						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$		1950		pF
Output Capacitance	C_{oss}			160		
Reverse Transfer Capacitance	C_{rss}			70		
Total Gate Charge ^c	Q_g	$V_{DS} = 125\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 17\text{ A}$		30	42	nC
Gate-Source Charge ^c	Q_{gs}			10		
Gate-Drain Charge ^c	Q_{gd}			10		
Gate Resistance	R_g			1.6		Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 125\text{ V}$, $R_L = 7.35\text{ }\Omega$ $I_D \equiv 17\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 2.5\text{ }\Omega$		15	25	ns
Rise Time ^c	t_r			130	195	
Turn-Off Delay Time ^c	$t_{d(off)}$			30	45	
Fall Time ^c	t_f			100	150	
Source-Drain Diode Ratings and Characteristics ($T_C = 25\text{ }^{\circ}\text{C}$)						
Pulsed Current	I_{SM}				20	A
Diode Forward Voltage ^b	V_{SD}	$I_F = 17\text{ A}$, $V_{GS} = 0\text{ V}$		0.9	1.5	V
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		115	175	ns

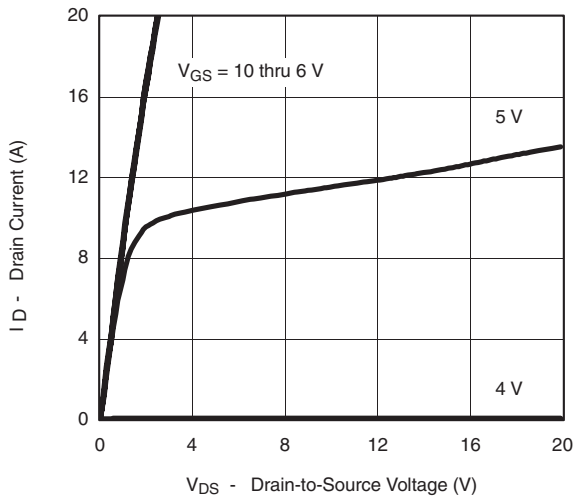
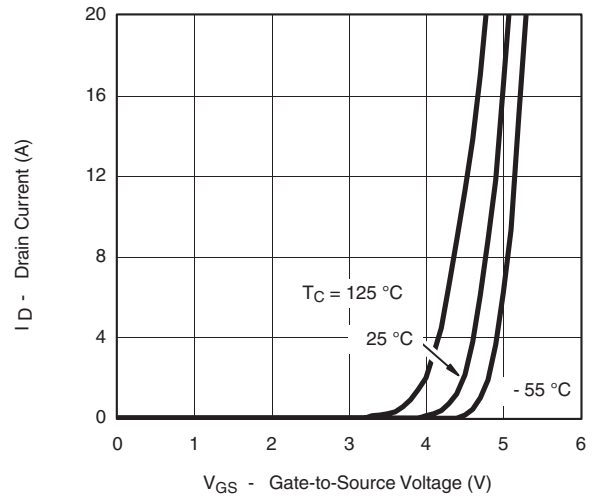
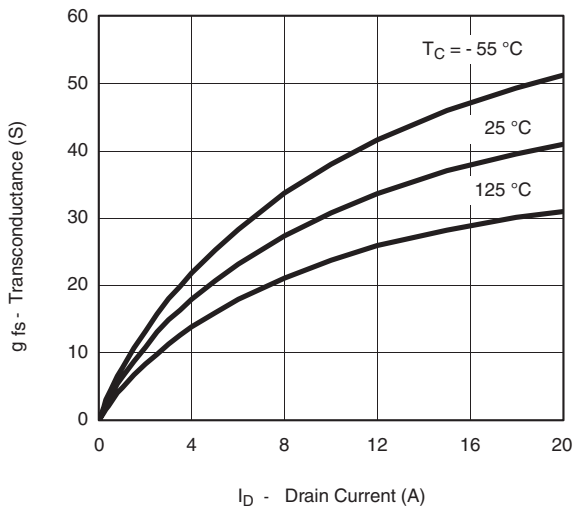
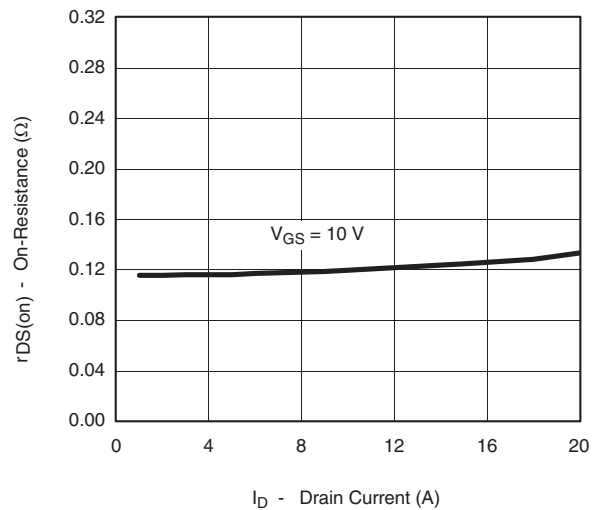
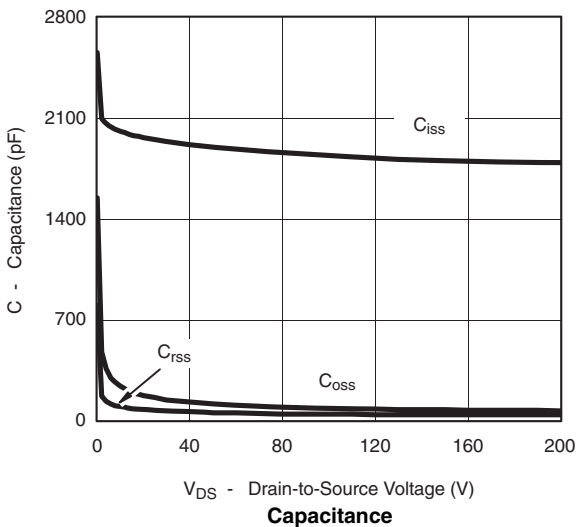
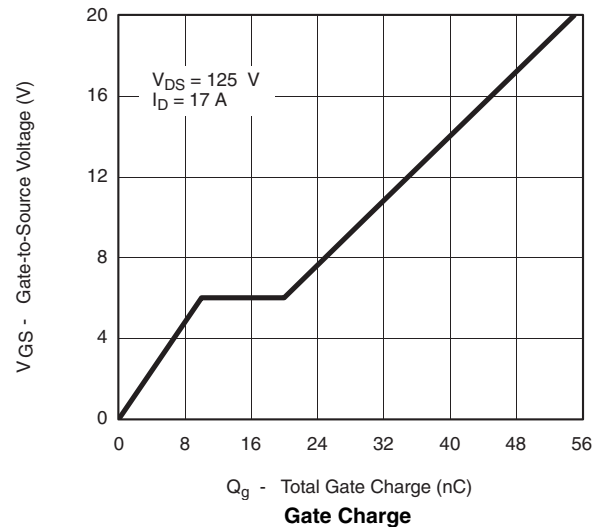
Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

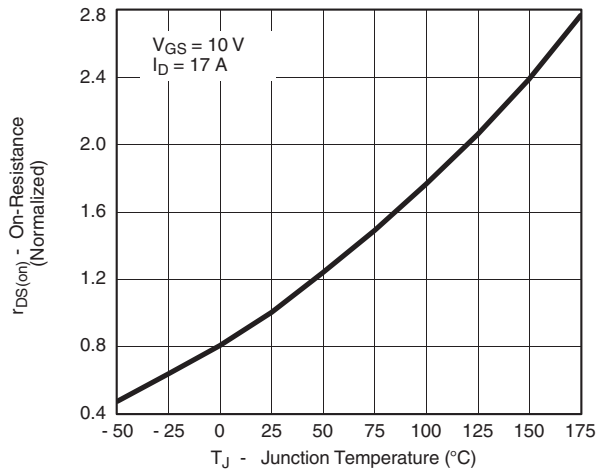
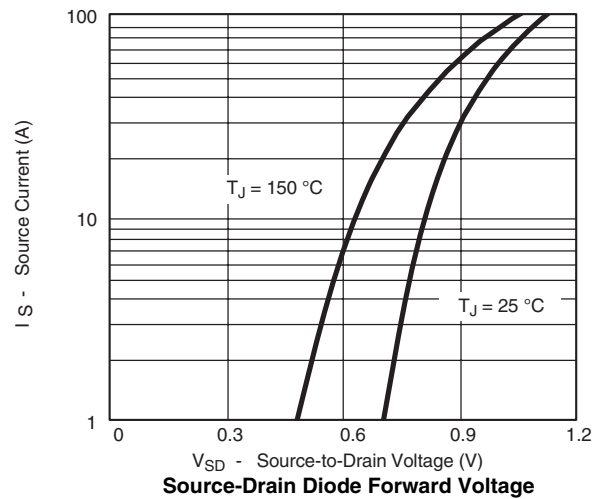
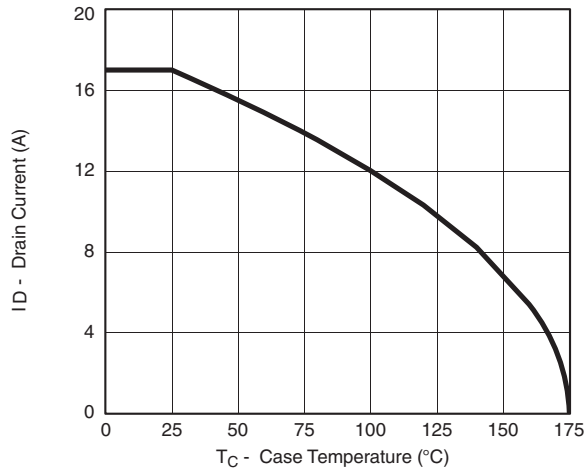
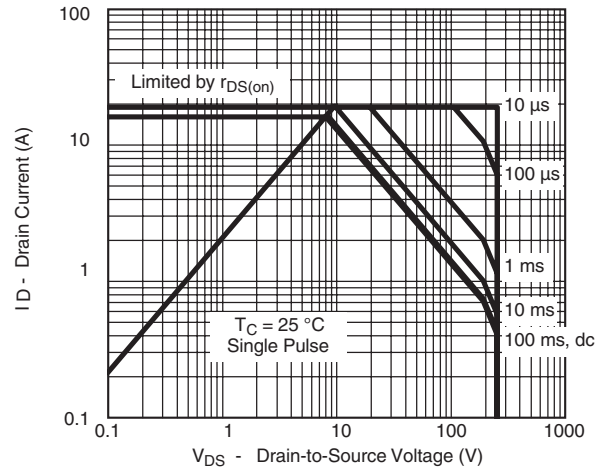
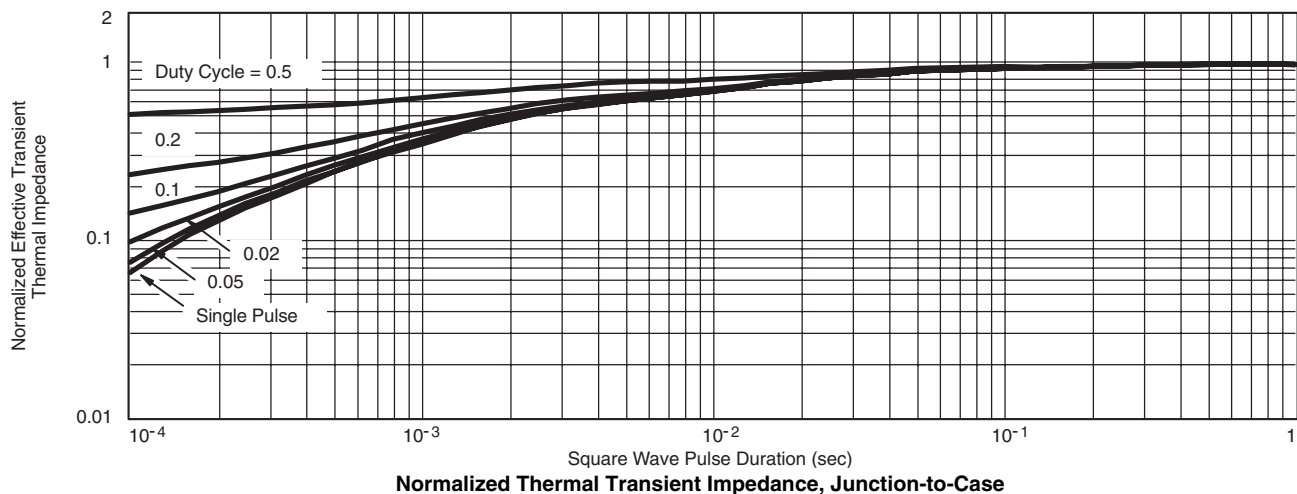
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C unless noted**Output Characteristics****Transfer Characteristics****Transconductance****On-Resistance vs. Drain Current****Capacitance****Gate Charge**

SUD17N25-165

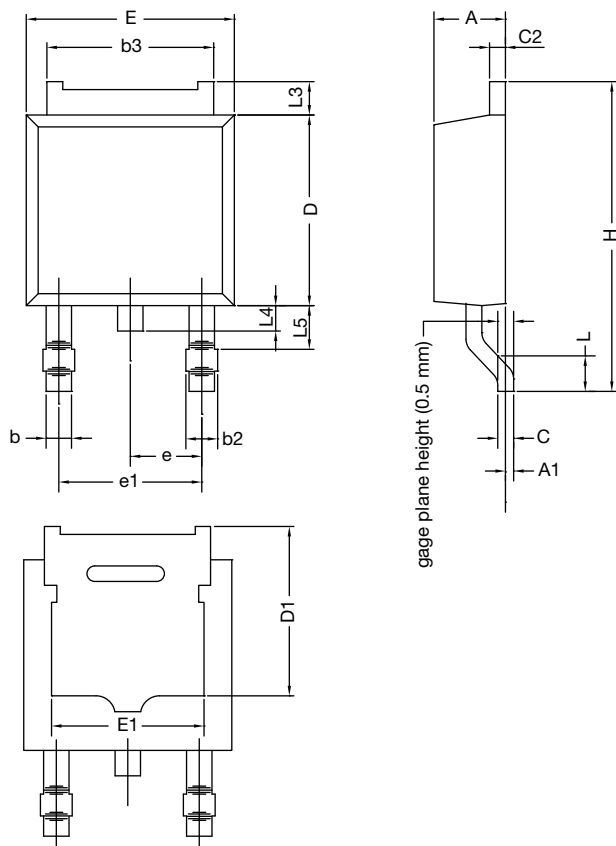
Vishay Siliconix

**TYPICAL CHARACTERISTICS** 25 °C unless noted**On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****THERMAL RATINGS****Maximum Avalanche Drain Current vs. Case Temperature****Safe Operating Area****Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72851>.



TO-252AA Case Outline

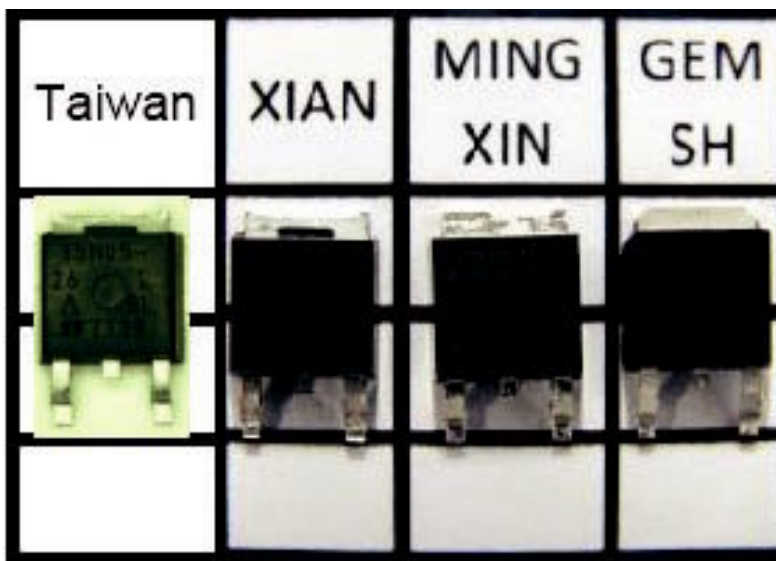


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

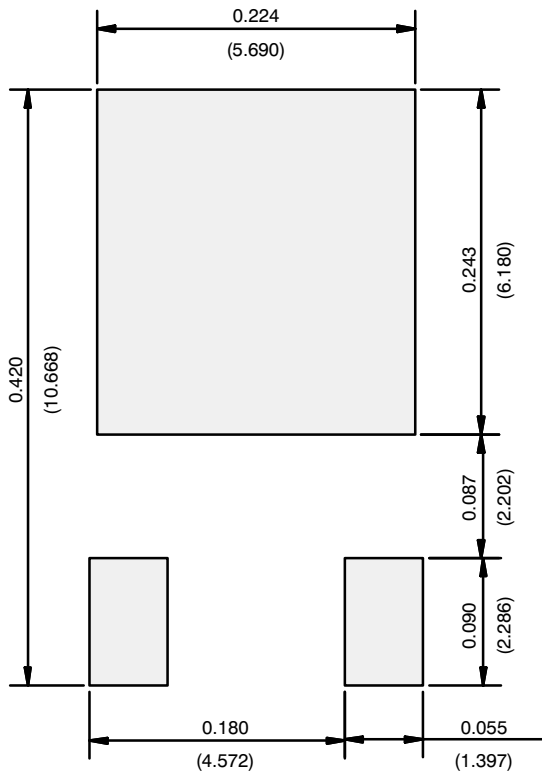
ECN: T13-0359-Rev. O, 03-Jun-13
DWG: 5347

Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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