NEC

MOS INTEGRATED CIRCUIT

μPD75P3036

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD75P3036 replaces the μPD753036's internal mask ROM with a one-time PROM or EPROM.
Because the μPD75P3036 supports programming by users, it is suitable for use in prototype testing for system development using the μPD753036 and for use in small-scale production.

* **Caution The μPD75P3036KK-T is not designed to guarantee the reliability required for use in mass-production. Please use it only for performance evaluation during testing and test production runs.**

Detailed descriptions of functions are provided in the following document. Be sure to read the document before designing.

μPD753036 User's Manual : U10201E

FEATURES

- Compatible with μPD753036
- Internal PROM: 16384 × 8 bits
  - μPD75P3036KK-T : Reprogrammable (ideally suited for system evaluation)
  - μPD75P3036GC, 75P3036GK : One-time programmable (ideally suited for small-scale production)
- Internal RAM: 768 × 4 bits
- Can operate in the same power supply voltage as the mask version μPD753036
  - V_{DD} = 1.8 to 5.5 V
- LCD controller/driver
- A/D converter

Caution Mask-option pull-up resistors are not provided in this device.

ORDERING INFORMATION

Part Number	Package	Internal PROM	Quality Grade
μPD75P3036GC-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)	One-time PROM	Standard
μPD75P3036GK-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm, 0.5-mm pitch)	One-time PROM	Standard
* μPD75P3036KK-T	80-pin ceramic WQFN	EPROM	Not applicable

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

In this document, the term PROM is used in parts common to one-time PROM versions and EPROM versions.

The information in this document is subject to change without notice.

Document No. U11575EJ1V0DS00 (1st edition)
(Previous No. IP-3657)
Date Published November 1996 P
Printed in Japan

The mark * shows major revised points.

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Functional Outline

Parameter			Function
Instruction execution time			• 0.95, 1.91, 3.81, 15.3 μs (main system clock: during 4.19-MHz operation) • 0.67, 1.33, 2.67, 10.7 μs (main system clock: during 6.0-MHz operation) • 122 μs (subsystem clock: during 32.768-kHz operation)
Internal memory	PROM		16384 × 8 bits
	RAM		768 × 4 bits
General purpose register			• 4-bit operation: 8 × 4 banks • 8-bit operation: 4 × 4 banks
Input/ output port	CMOS input	8	On-chip pull-up resistors can be specified by using software: 27
	CMOS input/output	20	
	Bit port output	8	Also used for segment pins
*	N-ch open-drain input/output pins	8	13 V withstand voltage
	Total	44	
LCD controller/driver			• Segment selection: 12/16/20 segments (can be changed to bit port output in unit of 4; max. 8) • Display mode selection: Static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty (1/3 bias)
Timer			5 channels • 8-bit timer/event counter: 3 channels (16-bit timer/event counter, carrier generator, timer with gate) • Basic interval/watchdog timer: 1 channel • Watch timer: 1 channel
Serial interface			• 3-wire serial I/O mode ... MSB or LSB can be selected for transferring first bit • 2-wire serial I/O mode • SBI mode
A/D converter			8-bit resolution: 8 channels
Bit sequential buffer (BSB)			16 bits
Clock output (PCL)			• Φ, 524, 262, 65.5 kHz (main system clock: during 4.19-MHz operation) • Φ, 750, 375, 93.8 kHz (main system clock: during 6.0-MHz operation)
Buzzer output (BUZ)			• 2, 4, 32 kHz (main system clock: during 4.19-MHz operation or subsystem clock: during 32.768-kHz operation) • 2.86, 5.72, 45.8 kHz (main system clock: during 6.0-MHz operation)
Vectored interrupt			External: 3, Internal: 5
Test input			External: 1, Internal: 1
System clock oscillator			• Ceramic or crystal oscillator for main system clock oscillation • Crystal oscillator for subsystem clock oscillation
Standby function			STOP/HALT mode
Power supply voltage			V_{DD} = 1.8 to 5.5 V
Package			• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm) * • 80-pin ceramic WQFN

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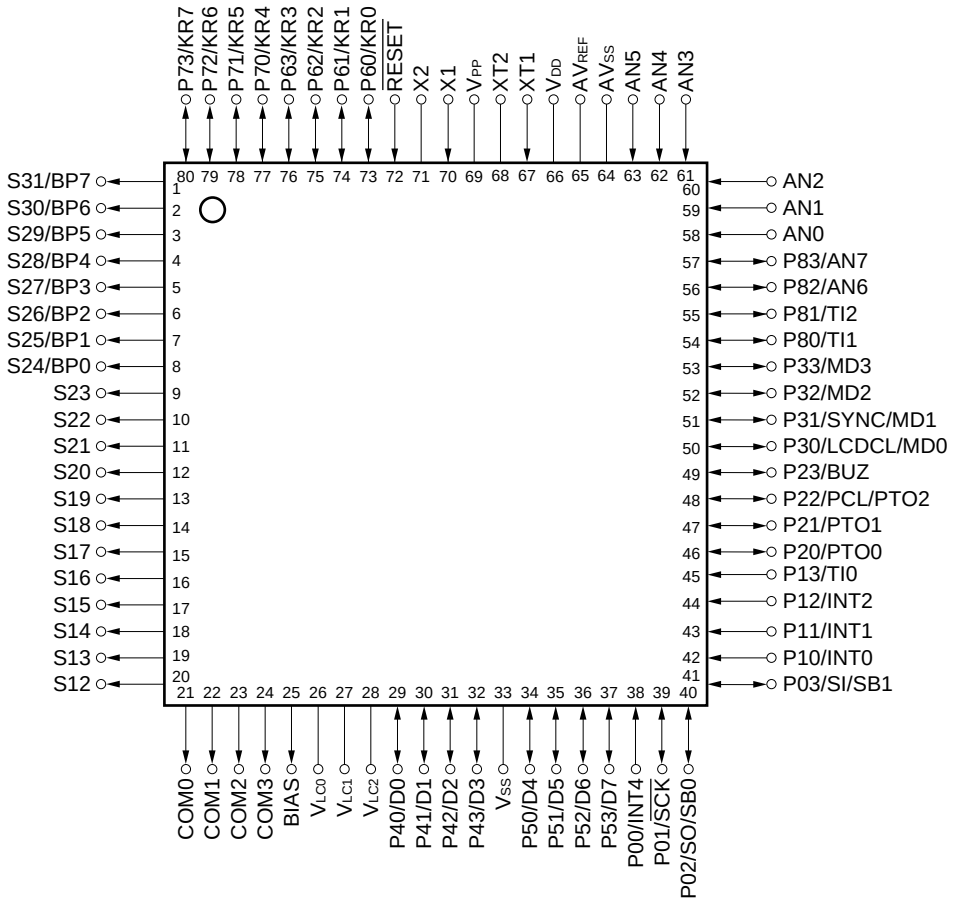
1. PIN CONFIGURATION (Top View)

- **80-pin plastic QFP (14 × 14 mm)**
  μPD75P3036GC-3B9
- **80-pin plastic TQFP (fine pitch) (12 × 12 mm)**
  μPD75P3036GK-BE9
- **80-pin ceramic WQFN**
  μPD75P3036KK-T

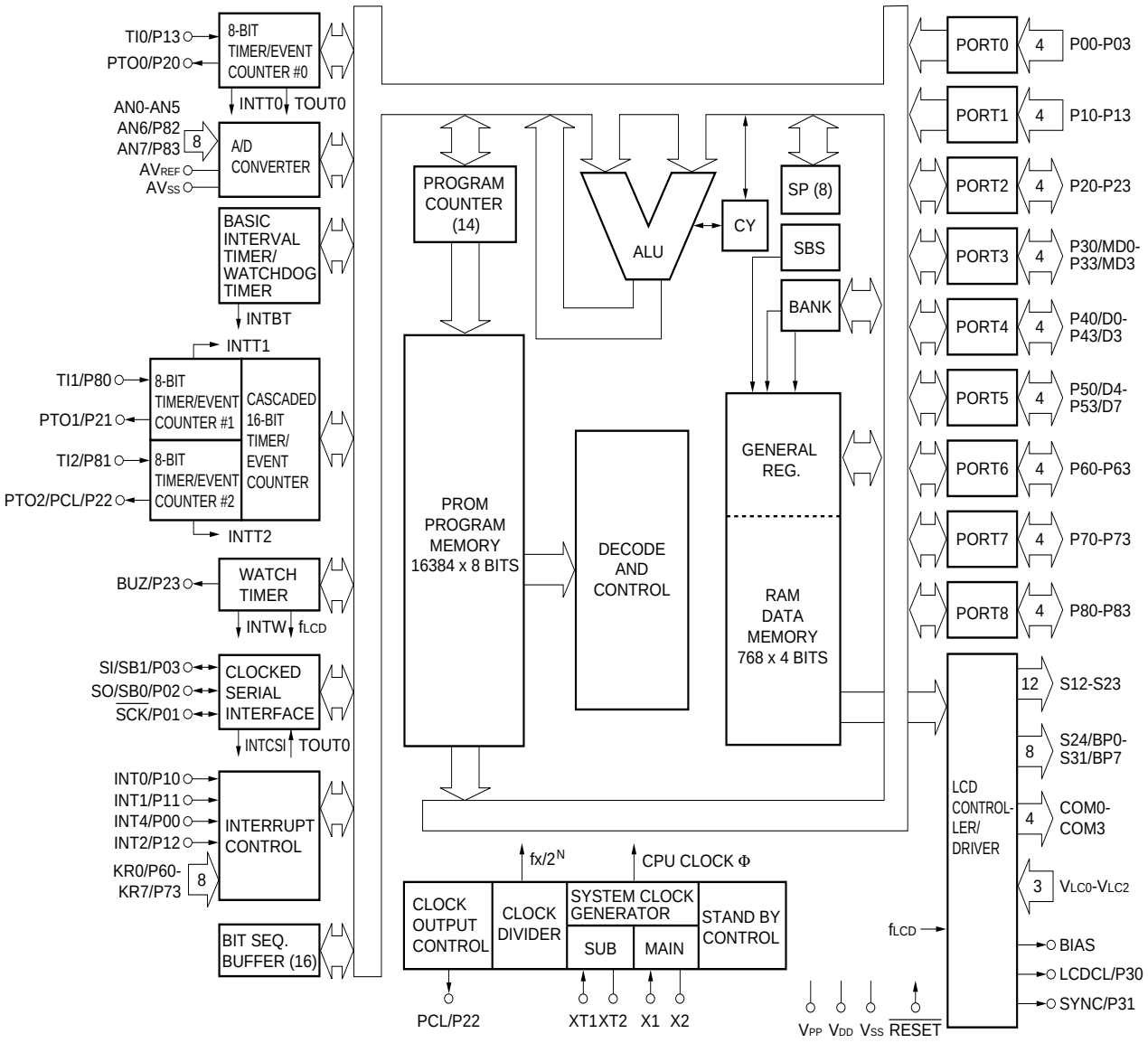


Caution Connect the V_{PP} pin directly to V_{DD}.

PIN IDENTIFICATIONS

P00 to P03	: Port0
P10 to P13	: Port1
P20 to P23	: Port2
P30 to P33	: Port3
P40 to P43	: Port4
P50 to P53	: Port5
P60 to P63	: Port6
P70 to P73	: Port7
P80 to P83	: Port8
BP0 to BP7	: Bit Port0-7
KR0 to KR7	: Key Return 0-7
$\overline{\text{SCK}}$	: Serial Clock
SI	: Serial Input
SO	: Serial Output
SB0, SB1	: Serial Bus 0,1
AV_{REF}	: Analog Reference
AV_{SS}	: Analog Ground
AN0-AN7	: Analog Input 0-7
MD0 to MD3	: Mode Selection 0-3
D0 to D7	: Data Bus 0-7
S12 to S31	: Segment Output 12-31
COM0 to COM3	: Common Output 0-3
V_{LC0} to V_{LC2}	: LCD Power Supply 0-2
BIAS	: LCD Power Supply Bias Control
LCDCL	: LCD Clock
SYNC	: LCD Synchronization
TI0 to TI2	: Timer Input 0-2
PTO0 to PTO2	: Programmable Timer Output 0-2
BUZ	: Buzzer Clock
PCL	: Programmable Clock
INT0, INT1, INT4	: External Vectored Interrupt 0, 1, 4
INT2	: External Test Input 2
X1, X2	: Main System Clock Oscillation 1, 2
XT1, XT2	: Subsystem Clock Oscillation 1, 2
$\overline{\text{RESET}}$	: Reset
V_{PP}	: Programming Power Supply
V_{DD}	: Positive Power Supply
V_{SS}	: Ground

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin name	I/O	Alternate function	Function	8-bit I/O	Status after reset	I/O circuit type[Note 1]
P00	Input	INT4	This is a 4-bit input port (PORT0). Connection of an on-chip pull-up resistor can be specified in 3-bit units by software for P01 to P03.	No	Input	<B>
P01	I/O	$\overline{\text{SCK}}$				<F>-A
P02	I/O	SO/SB0				<F>-B
P03	I/O	SI/SB1				<M>-C
P10	Input	INT0	This is a 4-bit input port (PORT1). Connection of an on-chip pull-up resistor can be specified in 4-bit units by software. P10/INT0 can select noise elimination circuit.	No	Input	<B>-C
P11		INT1				
P12		INT2				
P13		TI0				
P20	I/O	PTO0	This is a 4-bit I/O port (PORT2). Connection of an on-chip pull-up resistor can be specified in 4-bit units by software.	No	Input	E-B
P21		PTO1				
P22		PCL/PTO2				
P23		BUZ				
P30	I/O	LCDCL/MD0	This is a programmable 4-bit I/O port (PORT3). Input and output can be specified in bit units. Connection of an on-chip pull-up resistor can be specified in 4-bit units by software.	No	Input	E-B
P31		SYNC/MD1				
P32		MD2				
P33		MD3				
* P40[Note 2]	I/O	D0	This is an N-ch open-drain 4-bit I/O port (PORT4). When set to open-drain, voltage is 13 V. Also functions as data I/O pin (lower 4 bits) for program memory (PROM) write/verify.	Yes	High impedance	M-E
P41[Note 2]		D1				
P42[Note 2]		D2				
P43[Note 2]		D3				
* P50[Note 2]	I/O	D4	This is an N-ch open-drain 4-bit I/O port (PORT5). When set to open-drain, voltage is 13 V. Also functions as data I/O pin (upper 4 bits) for program memory (PROM) write/verify.		High impedance	M-E
P51[Note 2]		D5				
P52[Note 2]		D6				
P53[Note 2]		D7				

Notes 1. Circuit types enclosed in brackets indicate Schmitt trigger input.

2. Low level input leakage current increases when input instructions or bit manipulate instructions are executed.

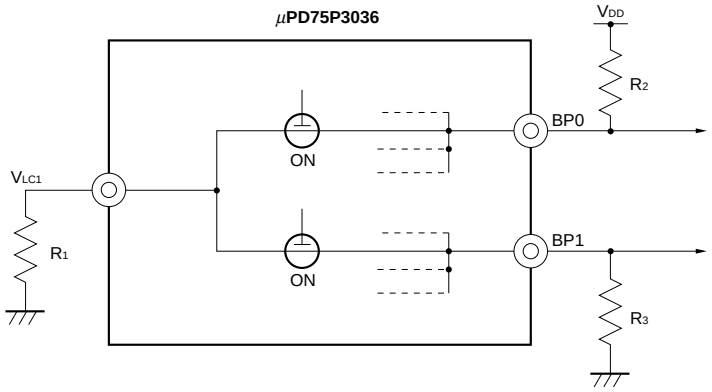
3.1 Port Pins (2/2)

Pin name	I/O	Alternate function	Function	8-bit I/O	Status after reset	I/O circuit type[Note 1]
P60	I/O	KR0	This is a programmable 4-bit I/O port (PORT6). Input and output can be specified in bit units. Connection of an on-chip pull-up resistor can be specified in 4-bit units by software.	Yes	Input	<F>-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	I/O	KR4	This is a 4-bit I/O port (PORT7). Connection of an on-chip pull-up resistor can be specified in 4-bit units by software.		Input	<F>-A
P71		KR5				
P72		KR6				
P73		KR7				
P80	I/O	TI1	This is a 4-bit I/O port (PORT8). Connection of an on-chip pull-up resistor can be specified in 4-bit units by software.	No	Input	<E>-E
P81		TI2				
P82		AN6				Y-B
P83		AN7				
BP0	Output	S24	These pins are also used as 1-bit I/O port (BIT PORT) segment output pin.	No	**Note 2**	H-A
BP1		S25				
BP2		S26				
BP3		S27				
BP4	Output	S28				
BP5		S29				
BP6		S30				
BP7		S31				

Notes 1. Circuit types enclosed in brackets indicate Schmitt trigger input.

* **2.** BP0 through BP7 select V_{LC1} as an input source.
However, the output levels change depending on the external circuit of BP0 through BP7 and V_{LC1}.

* **Example** Because BP0 through BP7 are mutually connected inside the μPD75P3036, the output levels of BP0 through BP7 are determined by R_1, R_2, and R_3.



3.2 Non-port Pins (1/2)

Pin name	I/O	Alternate function	Function		Status after reset	I/O circuit type[Note]
TI0	Input	P13	External event pulse input to timer/event counter		Input	<B>-C
TI1		P80				<E>-E
TI2		P81				
PTO0	Output	P20	Timer/event counter output		Input	E-B
PTO1		P21				
PTO2		P22/PCL				
PCL	Output	P22/PTO2	Clock output		Input	E-B
BUZ	Output	P23	Frequency output (for buzzer or system clock trimming)		Input	E-B
$\overline{\text{SCK}}$	I/O	P01	Serial clock I/O		Input	<F>-A
SO/SB0	I/O	P02	Serial data output Serial data bus I/O		Input	<F>-B
SI/SB1	I/O	P03	Serial data input Serial data bus I/O		Input	<M>-C
INT4	Input	P00	Edge detection vectored interrupt input (valid for detecting both rising and falling edges)		Input	<B>
INT0	Input	P10	Edge detection vectored interrupt input (detected edge is selectable) INT0/P10 can select noise elimination circuit.	Noise elimination circuit /asynchronous is selectable	Input	<B>-C
INT1		P11		Asynchronous		
INT2	Input	P12	Rising edge detection test input	Asynchonous	Input	<B>-C
KR0 to KR3	Input	P60 to P63	Parallel falling edge detection test input		Input	<F>-A
KR4 to KR7	Input	P70 to P73	Parallel falling edge detection test input		Input	<F>-A
X1	Input	—	Ceramic/crystal oscillation circuit connection for main system clock. If using an external clock, input to X1 and input inverted phase to X2.		—	—
X2	—	—				
XT1	Input	—	Crystal oscillation circuit connection for subsystem clock. If using an external clock, input to XT1 and input inverted phase to XT2. XT1 can be used as a 1-bit (test) input.		—	—
XT2	—	—				
$\overline{\text{RESET}}$	Input	—	System reset input (low level active)		—	<B>
MD0	I/O	P30/LCDCL	Mode selection for program memory (PROM) write/verify		Input	E-B
MD1		P31/SYNC				
MD2, MD3		P32, P33				
D0 to D3	I/O	P40 to P43	Data bus for program memory (PROM) write/verify		Input	M-E
D4 to D7		P50 to P53				
V_{PP}	—	—	Programmable power supply voltage for program memory (PROM) write/verify. For normal operation, connect to V_{DD}. Apply +12.5 V for PROM write/verify.		—	—
V_{DD}	—	—	Positive power supply		—	—
V_{SS}	—	—	Ground		—	—

Note Circuit types enclosed in brackets indicate Schmitt trigger input.

3.2 Non-port Pins (2/2)

Pin name	I/O	Alternate function	Function	Status after reset	I/O circuit type
S12 to S23	Output	—	Segment signal output	**Note 1**	G-A
S24 to S31	Output	BP0 to BP7	Segment signal output	**Note 1**	H-A
COM0 to COM3	Output	—	Common signal output	**Note 1**	G-B
V_{LC0} to V_{LC2}	—	—	Power source for LCD driver	—	—
BIAS	Output	—	Output for external split resistor cut	High impedance	—
LCDCL[Note 2]	Output	P30/MD0	Clock output for driving external expansion driver	Input	E-B
SYNC[Note 2]	Output	P31/MD1	Clock output for synchronization of external expansion driver	Input	E-B
AN0 to AN5	Input	—	Analog signal input for A/D converter	Input	Y
AN6		P82			Y-B
AN7		P83			
AV_{REF}	—	—	A/D converter reference voltage	—	Z-N
AV_{SS}	—	—	A/D converter reference GND potential	—	Z-N

Notes 1. The V_{LCX} (X = 0, 1, 2) shown below are selected as the input source for the display outputs.
S12 to S31: V_{LC1}, COM0 to COM2: V_{LC2}, COM3: V_{LC0}

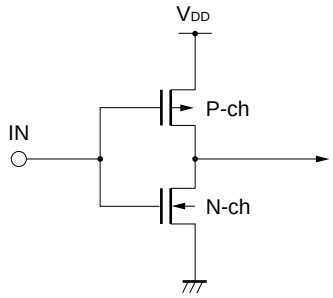
2. These pins are provided for future system expansion. Currently, only P30 and P31 are used.

3.3 Pin Input/Output Circuits

The input/output circuits for the μPD75P3036's pins are shown in schematic form below.

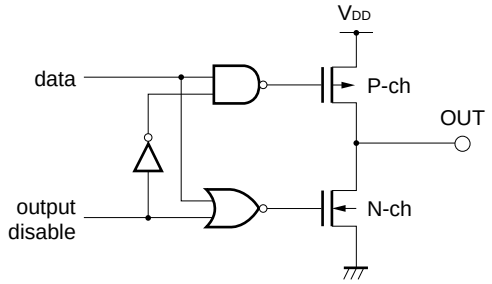
(1/3)

TYPE A



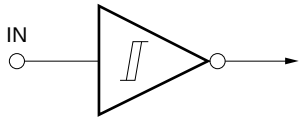
CMOS standard input buffer

TYPE D



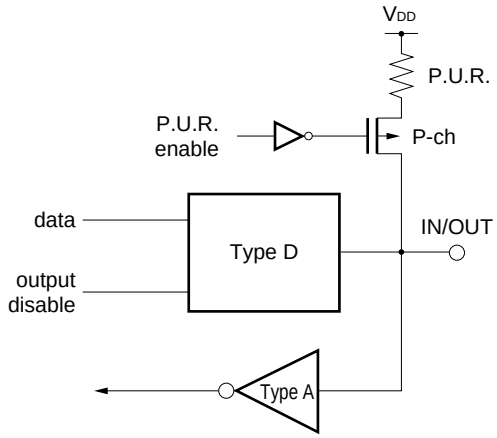
Push-pull output that can be set to output high-impedance (with both P-ch and N-ch OFF).

TYPE B



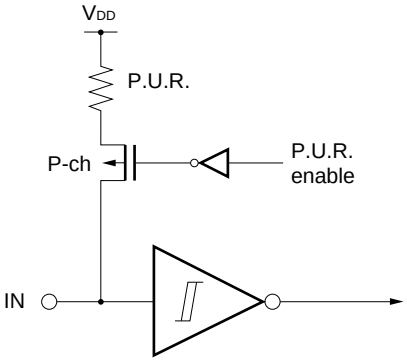
Schmitt trigger input with hysteresis characteristics.

TYPE E-B



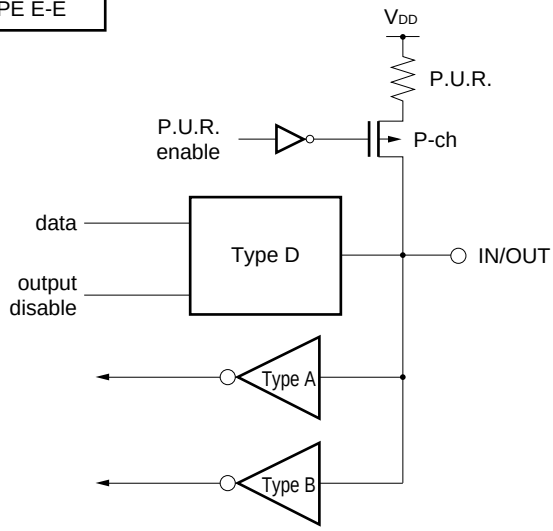
P.U.R. : Pull-Up Resistor

TYPE B-C



P.U.R. : Pull-Up Resistor

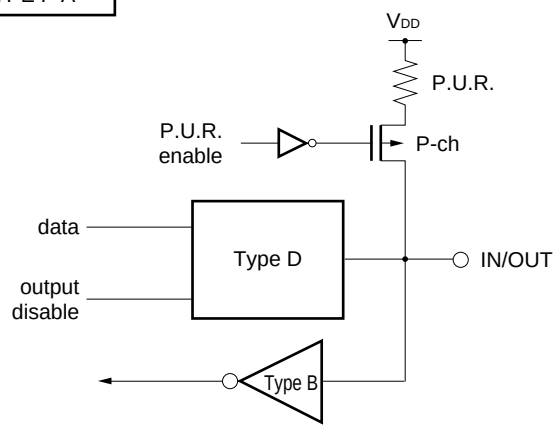
TYPE E-E



P.U.R. : Pull-Up Resistor

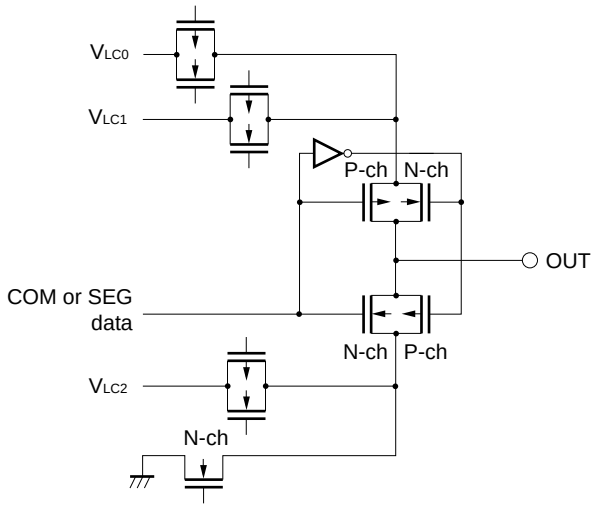
(2/3)

TYPE F-A

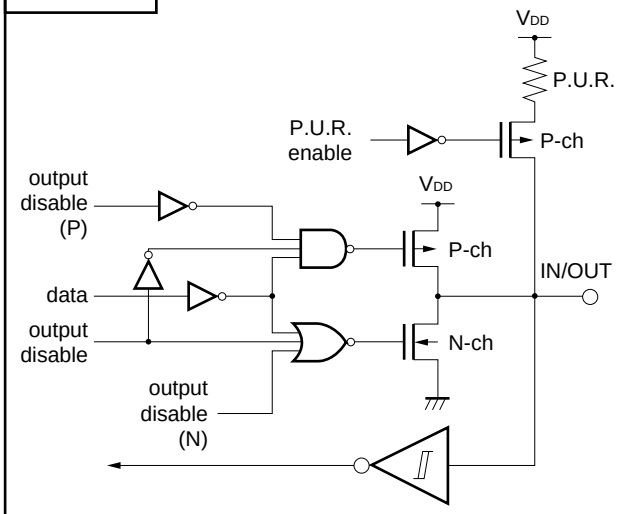


P.U.R. : Pull-Up Resistor

TYPE G-B*

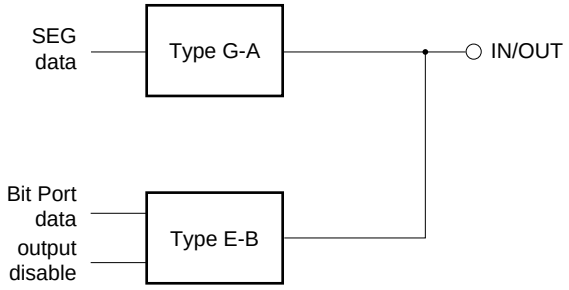


TYPE F-B

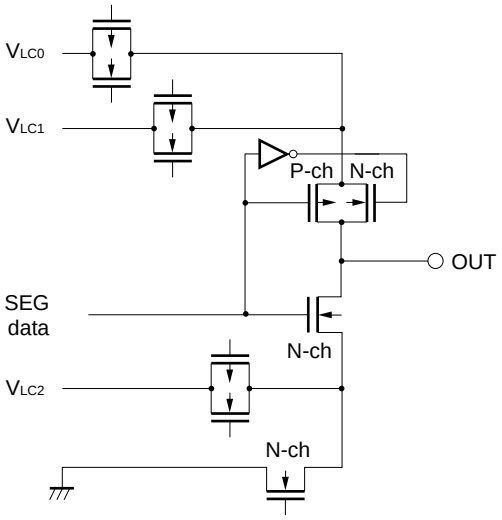


P.U.R. : Pull-Up Resistor

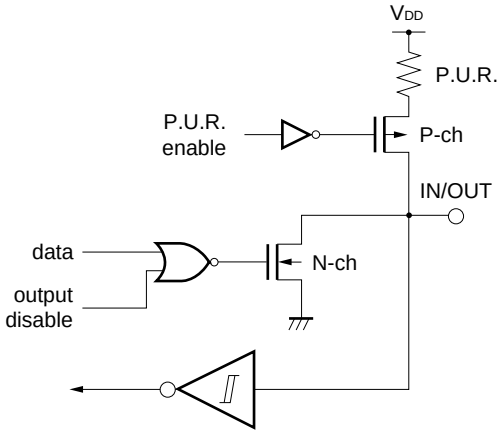
TYPE H-A*



TYPE G-A*

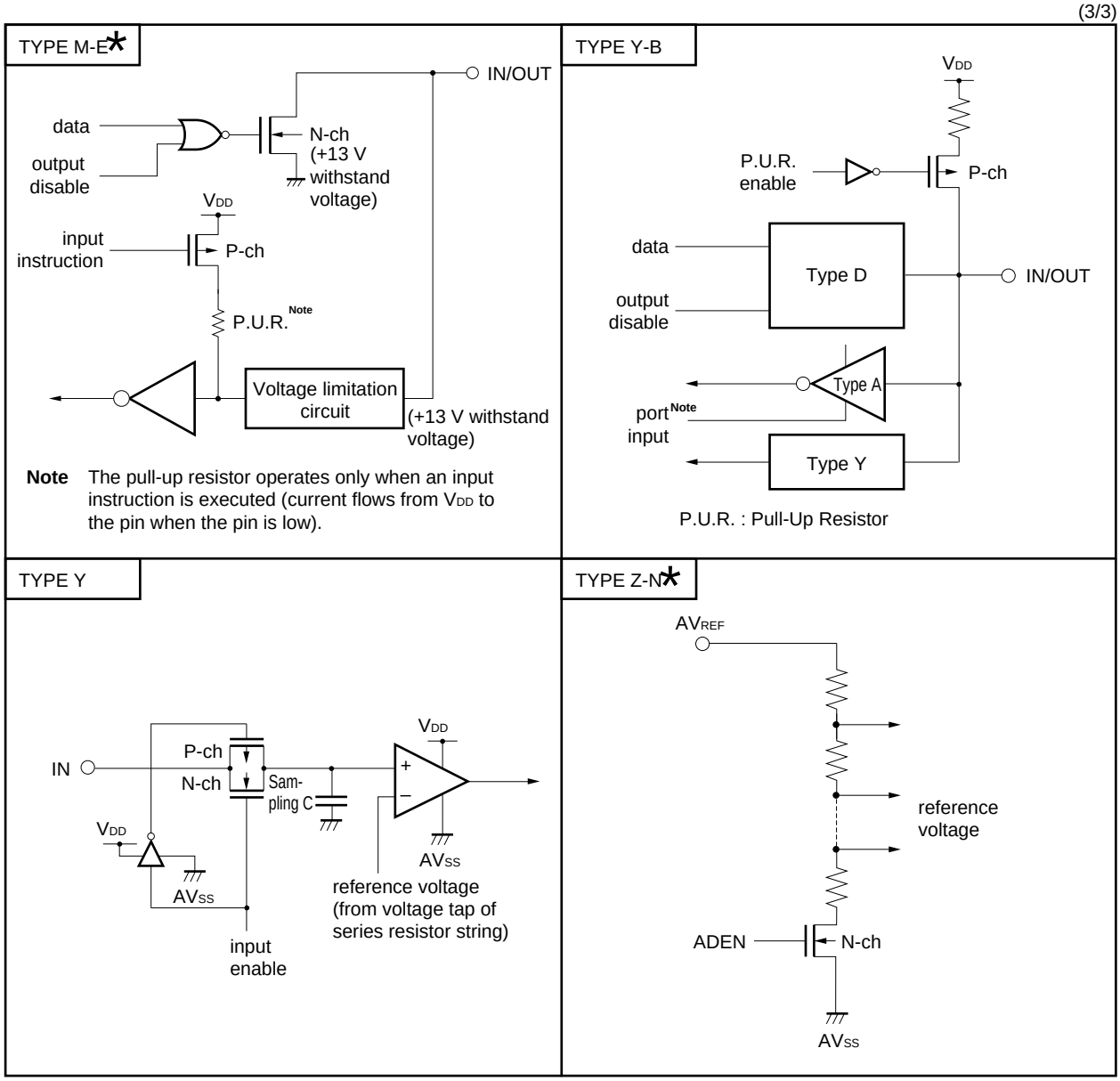


TYPE M-C



P.U.R. : Pull-Up Resistor

(3/3)



Note Becomes active when an input instruction is executed.

★ 3.4 Recommended Connection of Unused Pins

Pin	Recommended connection
P00/INT4	Connect to V_{SS} or V_{DD}
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD} via a resistor individually
P02/SO/SB0	
P03/SI/SB1	Connect to V_{SS}
P10/INT0 to P12/INT2	Connect to V_{SS} or V_{DD}
P13/TI0	
P20/PTO0	Input status : connect to V_{SS} or V_{DD} via a resistor individually. Output status: open
P21/PTO1	
P22/PTO2/PCL	
P23/BUZ	
P30/LCDCL	
P31/SYNC	
P32, P33	
P40 to P43	Connect to V_{SS}
P50 to P53	
P60/KR0 to P63/KR3	Input status : connect to V_{SS} or V_{DD} via a resistor individually. Output status: open
P70/KR4 to P73/KR7	
P80/TI1	
P81/TI2	
P82/AN6	
P83/AN7	
S12 to S23	Open
S24/BP0 to S31/BP7	
COM0 to COM3	
V_{LC0} to V_{LC2}	Connect to V_{SS}
BIAS	Connect to V_{SS} only when V_{LC0} to V_{LC2} are all not used. In other cases, leave open.
XT1[Note]	Connect to V_{SS} or V_{DD}
XT2[Note]	Open
AN0 to AN5	Connect to V_{SS} or V_{DD}
V_{PP}	Connect to V_{DD} directly

Note When the subsystem clock is not used, set SOS.0 to 1 (so as not to use the internal feedback resistor).

4. Mk I MODE AND Mk II MODE SELECTION FUNCTION

Setting a stack bank selection (SBS) register for the μPD75P3036 enables the program memory to be switched between Mk I mode and Mk II mode. This function is applicable when using the μPD75P3036 to evaluate the μPD753036.

When the SBS bit 3 is set to 1 : sets Mk I mode (supports Mk I mode for μPD753036)
When the SBS bit 3 is set to 0 : sets Mk II mode (supports Mk II mode for μPD753036)

4.1 Difference between Mk I Mode and Mk II Mode

Table 4-1 lists points of difference between the Mk I mode and the Mk II mode for the μPD75P3036.

Table 4-1. Difference between Mk I Mode and Mk II Mode

Item		Mk I Mode	Mk II Mode
Program counter		PC_{13-0}	
Program memory (bytes)		16384	
Data memory (bits)		768 x 4	
Stack	Stack bank	Selectable via memory banks 0 to 2	
	No. of stack bytes	2 bytes	3 bytes
Instruction	BRA !addr1 instruction CALLA !addr1 instruction	Not available	Available
Instruction execution time	CALL !addr instruction	3 machine cycles	4 machine cycles
	CALLF !faddr instruction	2 machine cycles	3 machine cycles
Supported mask ROM versions		When set to Mk I mode for μPD753036	When set to Mk II mode for μPD753036

* **Caution The Mk II mode supports a program area exceeding 16 Kbytes for the 75X and 75XL series. Therefore, this mode is effective for enhancing software compatibility with products exceeding 16 Kbytes.**
When the Mk II mode is selected, the number of stack bytes used during execution of subroutine call instructions increases by one byte per stack compared to the Mk I mode. When the CALL !addr and CALLF !faddr instructions are used, the machine cycle becomes longer by one machine cycle. Therefore, use the Mk I mode if the RAM efficiency and processing performance are more important than software compatibility.

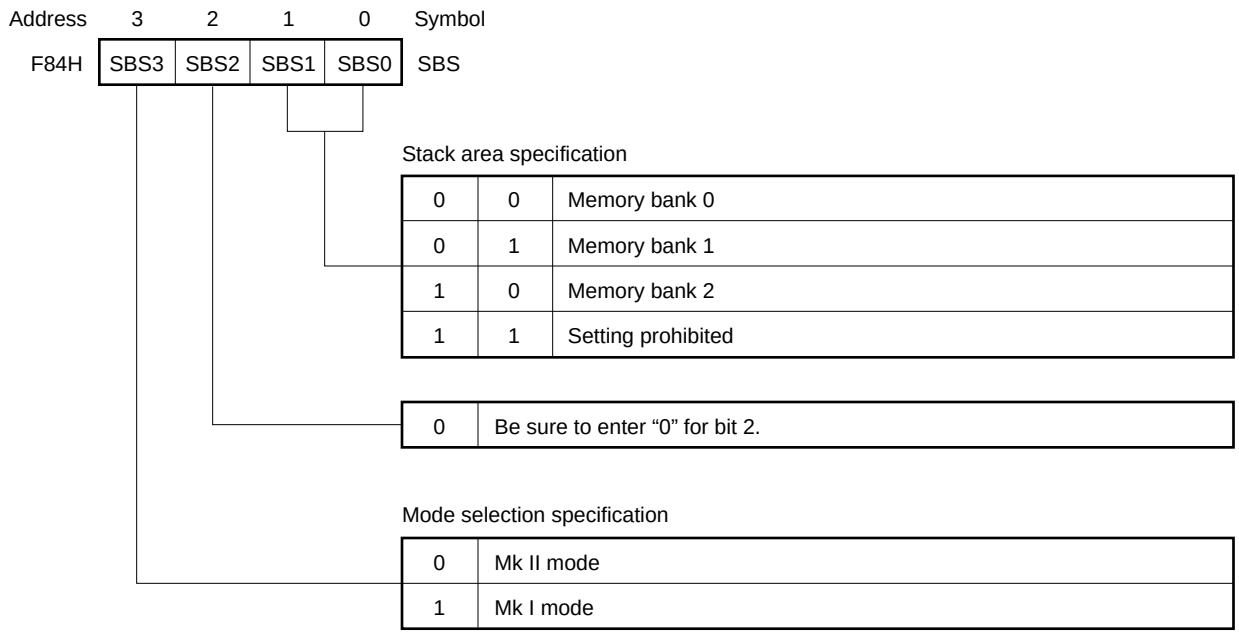
4.2 Setting of Stack Bank Selection Register (SBS)

Use the stack bank selection register to switch between Mk I mode and Mk II mode. Figure 4-1 shows the format for doing this.

The stack bank selection register is set using a 4-bit memory manipulation instruction. When using the Mk I mode, be sure to initialize the stack bank selection register to 10xxB[Note] at the beginning of the program. When using the Mk II mode, be sure to initialize it to 00xxB[Note].

Note Set the desired value for xx.

Figure 4-1. Format of Stack Bank Selection Register



Cautions 1. SBS3 is set to “1” after $\overline{\text{RESET}}$ input, and consequently the CPU operates in Mk I mode. When using instructions for Mk II mode, set SBS3 to “0” and set Mk II mode before using the instructions.

2. When using Mk II mode, execute a subroutine call instruction and an interrupt instruction after $\overline{\text{RESET}}$ input and after setting the stack bank selection register.

5. DIFFERENCES BETWEEN μPD75P3036 AND μPD753036

The μPD75P3036 replaces the internal mask ROM in the program memory of the μPD753036 with a one-time PROM or EPROM. The μPD75P3036's Mk I mode supports the Mk I mode in the μPD753036 and the μPD75P3036's Mk II mode supports the Mk II mode in the μPD753036.

Table 5-1 lists differences among the μPD75P3036 and the μPD753036. Be sure to check the differences among these products before using them with PROMs for debugging or prototype testing of application systems or, later, when using them with a mask ROM for full-scale production.

As to CPU function and on-chip hardware, see the **User's Manual**.

Table 5-1. Differences between μPD75P3036 and μPD753036

Item		μPD753036	**μPD75P3036**
Program counter		14 bits	
Program memory (bytes)		16384 Mask ROM	16384 One-time PROM, EPROM
Data memory (x 4 bits)		768	
Mask option	Pull-up resistor of ports 4, 5	Yes (can specify whether to incorporate on-chip or not)	No (don't incorporate on-chip)
	Split resistor for LCD driving power supply		
	Selection of oscillation stabilization wait time	Yes (can select either $2^{17}/f_X$ or $2^{15}/f_X$)**Note**	No (fixed to $2^{15}/f_X$)**Note**
	Selection of subsystem clock feedback resistor	Yes (can select either use enabled or use disabled)	No (use enabled)
Pin configuration	Pin No. 29 to 32	P40 to P43	P40/D0 to P43/D3
	Pin No. 34 to 37	P50 to P53	P50/D4 to P53/D7
	Pin No. 50	P30/LCDCL	P30/LCDCL/MD0
	Pin No. 51	P31/SYNC	P31/SYNC/MD1
	Pin No. 52	P32	P32/MD2
	Pin No. 53	P33	P33/MD3
	Pin No. 69	IC	V_{PP}
Other		Noise resistance and noise radiation may differ due to the different circuit sizes and mask layouts.	

Note $2^{17}/f_X$ is 21.8 ms during 6.0-MHz operation, and 31.3 ms during 4.19-MHz operation.
$2^{15}/f_X$ is 5.46 ms during 6.0-MHz operation, and 7.81 ms during 4.19-MHz operation.

Caution Noise resistance and noise radiation are different in PROM and mask ROM versions. In transferring to mask ROM versions from the PROM version in a process between prototype development and full production, be sure to fully evaluate the mask ROM version's CS (not ES).

6. PROGRAM COUNTER (PC) AND MEMORY MAP

6.1 Program Counter (PC) ... 14 bits

This is a 14-bit binary counter that stores program memory address data.

Figure 6-1. Configuration of Program Counter

PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PC

6.2 Program Memory (PROM) ... 16384 x 8 bits

The program memory consists of 16384 x 8-bit one-time PROM or EPROM.

- Addresses 0000H and 0001H
  Vector table wherein the program start address and the values set for the RBE and MBE at the time a $\overline{\text{RESET}}$ signal is generated are written. Reset start is possible from any address.

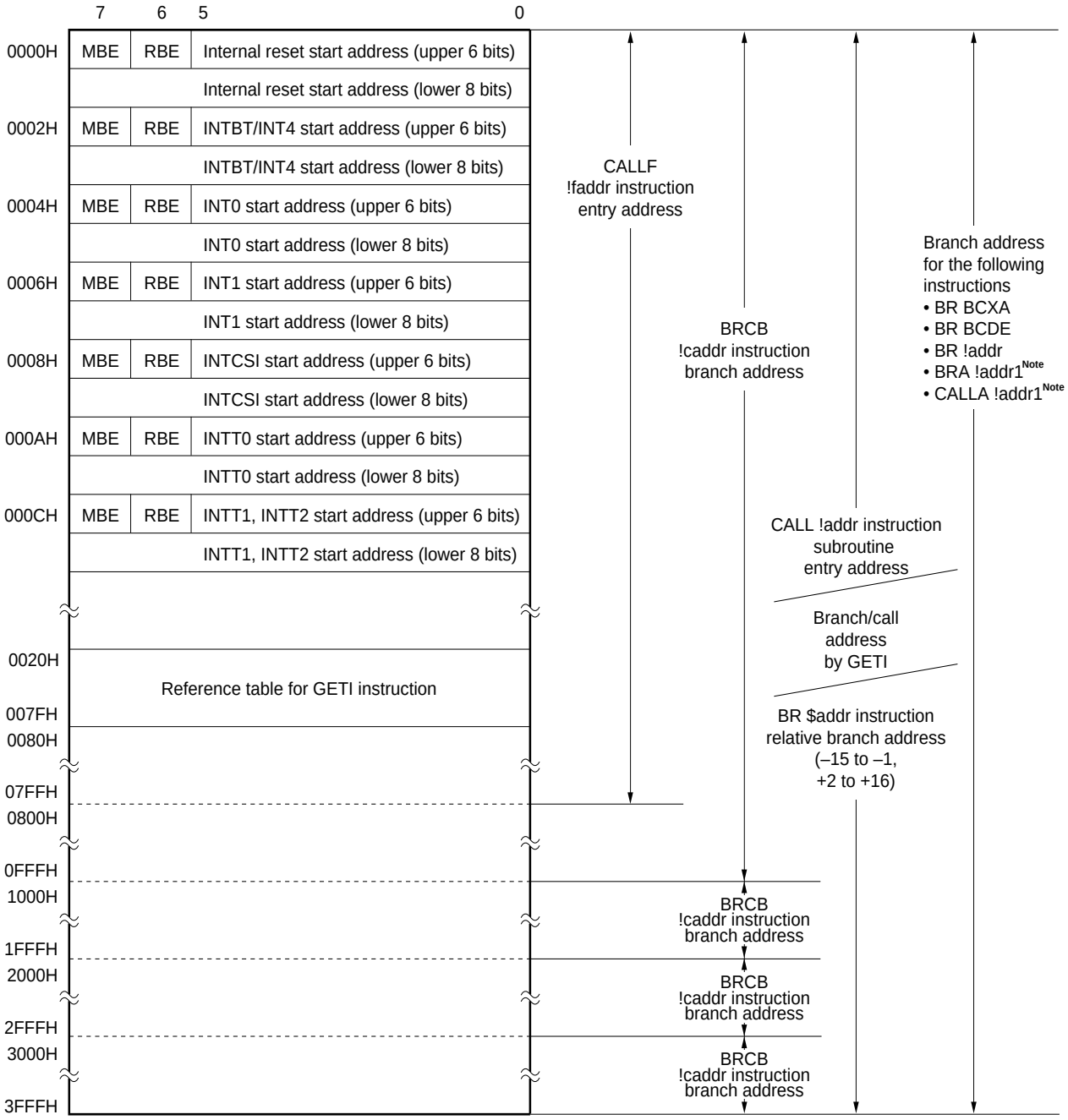
- Addresses 0002H to 000DH
  Vector table wherein the program start address and the values set for the RBE and MBE by each vectored interrupt are written. Interrupt processing can start from any address.

- Addresses 0020H to 007FH
  Table area referenced by the GETI instruction[Note].

Note The GETI instruction realizes a 1-byte instruction on behalf of any 2-byte/3-byte instruction, or two 1-byte instructions. It is used to decrease the number of program steps.

Figure 6-2 shows the addressing ranges for the program memory, branch instruction and the subroutine call instruction.

Figure 6-2. Program Memory Map



* **Note** Can be used only in the Mk II mode.

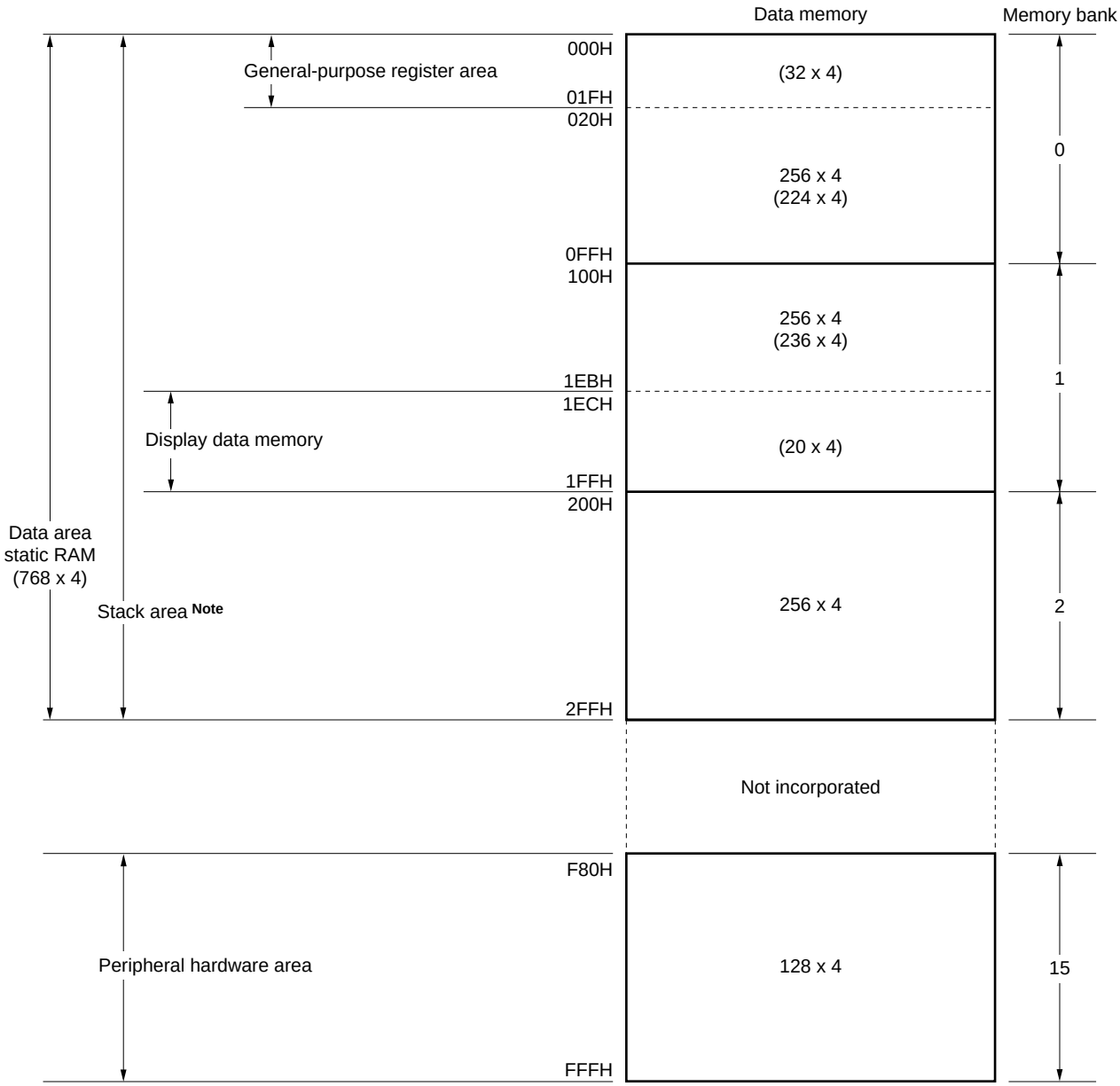
Remark For instructions other than those noted above, the BR PCDE and BR PCXA instructions can be used to branch to addresses with changes in the PC's lower 8 bits only.

6.3 Data Memory (RAM) ... 768 x 4 bits

Figure 6-3 shows the data memory configuration.

Data memory consists of a data area and a peripheral hardware area. The data area consists of 768 x 4-bit static RAM.

Figure 6-3. Data Memory Map



Note Memory bank 0, 1, or 2 can be selected as the stack area.

7. INSTRUCTION SET

(1) Representation and coding formats for operands

In the instruction's operand area, use the following coding format to describe operands corresponding to the instruction's operand representations (for further description, see the **RA75X Assembler Package User's Manual—Language (EEU-1363)**). When there are several codes, select and use just one. Codes that consist of uppercase letters and + or – symbols are key words that should be entered as they are.

For immediate data, enter an appropriate numerical value or label.

Enter register flag symbols as label descriptors instead of mem, fmem, pmem, bit, etc. (for further description, see the **User's Manual**). The number of labels that can be entered for fmem and pmem are restricted.

Representation	Coding format
reg	X, A, B, C, D, E, H, L
reg1	X, B, C, D, E, H, L
rp	XA, BC, DE, HL
rp1	BC, DE, HL
rp2	BC, DE
rp'	XA, BC, DE, HL, XA', BC', DE', HL'
rp'1	BC, DE, HL, XA', BC', DE', HL'
rpa	HL, HL+, HL–, DE, DL
rpa1	DE, DL
n4	4-bit immediate data or label
n8	8-bit immediate data or label
mem	8-bit immediate data or label[Note]
bit	2-bit immediate data or label
fmem	FB0H-FBFH, FF0H-FFFH immediate data or label
pmem	FC0H-FFFH immediate data or label
addr	0000H-3FFFH immediate data or label
addr1	0000H-3FFFH immediate data or label
caddr	12-bit immediate data or label
faddr	11-bit immediate data or label
taddr	20H-7FH immediate data (however, bit0 = 0) or label
PORTn	PORT0-PORT8
IEXXX	IEBT, IECSI, IET0-IET2, IE0-IE2, IE4, IEW
RBn	RB0-RB3
MBn	MB0-MB2, MB15

Note When processing 8-bit data, only even-numbered addresses can be entered.

(2) Operation legend

A	: A register; 4-bit accumulator
B	: B register
C	: C register
D	: D register
E	: E register
H	: H register
L	: L register
X	: X register
XA	: Register pair (XA); 8-bit accumulator
BC	: Register pair (BC)
DE	: Register pair (DE)
HL	: Register pair (HL)
XA’	: Expansion register pair (XA’)
BC’	: Expansion register pair (BC’)
DE’	: Expansion register pair (DE’)
HL’	: Expansion register pair (HL’)
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag; bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
RBE	: Register bank enable flag
PORTn	: Port n (n = 0 to 8)
IME	: Interrupt master enable flag
IPS	: Interrupt priority selection register
IEXXX	: Interrupt enable flag
RBS	: Register bank selection register
MBS	: Memory bank selection register
PCC	: Processor clock control register
.	: Delimiter for address and bit
(XX)	: The contents addressed by XX
XXH	: Hexadecimal data

(3) Description of symbols used in addressing area

*1	MB = MBE • MBS MBS = 0-2, 15	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (000H-07FH) MB = 15 (F80H-FFFH) MBE = 1 : MB = MBS MBS = 0-2, 15	
*4	MB = 15, fmem = FB0H-FBFH, FF0H-FFFH	
*5	MB = 15, pmem = FC0H-FFFH	
*6	addr = 0000H-3FFFH	Program memory addressing
*7	addr, addr1 = (Current PC) –15 to (Current PC) –1 (Current PC) +2 to (Current PC) +16	
*8	caddr = 0000H-0FFFH ($PC_{13, 12}$ = 00B: Mk I or Mk II mode) or 1000H-1FFFH ($PC_{13, 12}$ = 01B: Mk I or Mk II mode) or 2000H-2FFFH ($PC_{13, 12}$ = 10B: Mk I or Mk II mode) or 3000H-3FFFH ($PC_{13, 12}$ = 11B: Mk I or Mk II mode)	
*9	faddr = 0000H-07FFH	
*10	taddr = 0020H-007FH	
*11	addr1 = 0000H-3FFFH	

Remarks 1. MB indicates access-enabled memory banks.
2. In area *2, MB = 0 for both MBE and MBS.
3. In areas *4 and *5, MB = 15 for both MBE and MBS.
4. Areas *6 to *11 indicate corresponding address-enabled areas.

(4) Description of machine cycles

S indicates the number of machine cycles required for skipping of skip-specified instructions. The value of S varies as shown below.

- No skip ..... S = 0
- Skipped instruction is 1-byte or 2-byte instruction .... S = 1
- Skipped instruction is 3-byte instruction[Note] ..... S = 2

Note 3-byte instructions: BR !addr, BRA !addr1, CALL !addr, CALLA !addr1

Caution The GETI instruction is skipped for one machine cycle.

One machine cycle equals one cycle (= t_{CY}) of the CPU clock Φ. Use the PCC setting to select among four cycle times.

Instruction group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Transfer	MOV	A, #n4	1	1	A<-n4		String-effect A
		reg1, #n4	2	2	reg1<-n4		
		XA, #n8	2	2	XA<-n8		String-effect A
		HL, #n8	2	2	HL<-n8		String-effect B
		rp2, #n8	2	2	rp2<-n8		
		A, @HL	1	1	A<-(HL)	*1	
		A, @HL+	1	2+S	A<-(HL), then L<-L+1	*1	L=0
		A, @HL–	1	2+S	A<-(HL), then L<-L–1	*1	L=FH
		A, @rpa1	1	1	A<-(rpa1)	*2	
		XA, @HL	2	2	XA<-(HL)	*1	
		@HL, A	1	1	(HL)<-A	*1	
		@HL, XA	2	2	(HL)<-XA	*1	
		A, mem	2	2	A<-(mem)	*3	
		XA, mem	2	2	XA<-(mem)	*3	
		mem, A	2	2	(mem)<-A	*3	
		mem, XA	2	2	(mem)<-XA	*3	
		A, reg1	2	2	A<-reg1		
		XA, rp’	2	2	XA<-rp’		
		reg1, A	2	2	reg1<-A		
		rp’1, XA	2	2	rp’1<-XA		
	XCH	A, @HL	1	1	A<->(HL)	*1	
		A, @HL+	1	2+S	A<->(HL), then L<-L+1	*1	L=0
		A, @HL–	1	2+S	A<->(HL), then L<-L–1	*1	L=FH
		A, @rpa1	1	1	A<->(rpa1)	*2	
		XA, @HL	2	2	XA<->(HL)	*1	
		A, mem	2	2	A<->(mem)	*3	
		XA, mem	2	2	XA<->(mem)	*3	
		A, reg1	1	1	A<->reg1		
		XA, rp’	2	2	XA<->rp’		
Table reference	MOVT	XA, @PCDE	1	3	XA<-$(PC_{13\text{-}8}+DE)_{ROM}$		
		XA, @PCXA	1	3	XA<-$(PC_{13\text{-}8}+XA)_{ROM}$		
		XA, @BCDE	1	3	XA<-$(BCDE)_{ROM}$ Note	*6	
		XA, @BCXA	1	3	XA<-$(BCXA)_{ROM}$ Note	*6	

Note Only the lower 2 bits in the B register are valid.

Instruction group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY<-(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY<-(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY<-(H+mem$_{3-0}$.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit)<-CY	*4	
		pmem.@L, CY	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))<-CY	*5	
		@H+mem.bit, CY	2	2	(H+mem$_{3-0}$.bit)<-CY	*1	
Arithmetic/ logical operation	ADDS	A, #n4	1	1+S	A<-A+n4		carry
		XA, #n8	2	2+S	XA<-XA+n8		carry
		A, @HL	1	1+S	A<-A+(HL)	*1	carry
		XA, rp’	2	2+S	XA<-XA+rp’		carry
		rp’1, XA	2	2+S	rp’1<-rp’1+XA		carry
	ADDC	A, @HL	1	1	A, CY<-A+(HL)+CY	*1	
		XA, rp’	2	2	XA, CY<-XA+rp’+CY		
		rp’1, XA	2	2	rp’1, CY<-rp’1+XA+CY		
	SUBS	A, @HL	1	1+S	A<-A–(HL)	*1	borrow
		XA, rp’	2	2+S	XA<-XA–rp’		borrow
		rp’1, XA	2	2+S	rp’1<-rp’1–XA		borrow
	SUBC	A, @HL	1	1	A, CY<-A–(HL)–CY	*1	
		XA, rp’	2	2	XA, CY<-XA–rp’–CY		
		rp’1, XA	2	2	rp’1, CY<-rp’1–XA–CY		
	AND	A, #n4	2	2	A<-A∧n4		
		A, @HL	1	1	A<-A∧(HL)	*1	
		XA, rp’	2	2	XA<-XA∧rp’		
		rp’1, XA	2	2	rp’1<-rp’1∧XA		
	OR	A, #n4	2	2	A<-A∨n4		
		A, @HL	1	1	A<-A∨(HL)	*1	
		XA, rp’	2	2	XA<-XA∨rp’		
		rp’1, XA	2	2	rp’1<-rp’1∨XA		
	XOR	A, #n4	2	2	A<-A∨̄n4		
		A, @HL	1	1	A<-A∨̄(HL)	*1	
		XA, rp’	2	2	XA<-XA∨̄rp’		
		rp’1, XA	2	2	rp’1<-rp’1∨̄XA		
Accumulator manipulation	RORC	A	1	1	CY<-A$_0$, A$_3$<-CY, A$_{n-1}$<-A$_n$		
	NOT	A	2	2	A<-$\overline{A}$		
Increment/ decrement	INCS	reg	1	1+S	reg<-reg+1		reg=0
		rp1	1	1+S	rp1<-rp1+1		rp1=00H
		@HL	2	2+S	(HL)<-(HL)+1	*1	(HL)=0
		mem	2	2+S	(mem)<-(mem)+1	*3	(mem)=0
	DECS	reg	1	1+S	reg<-reg–1		reg=FH
		rp’	2	2+S	rp’<-rp’–1		rp’=FFH

Instruction group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Comparison	SKE	reg, #n4	2	2+S	Skip if reg=n4		reg=n4
		@HL, #n4	2	2+S	Skip if(HL)=n4	*1	(HL)=n4
		A, @HL	1	1+S	Skip if A=(HL)	*1	A=(HL)
		XA, @HL	2	2+S	Skip if XA=(HL)	*1	XA=(HL)
		A, reg	2	2+S	Skip if A=reg		A=reg
		XA, rp'	2	2+S	Skip if XA=rp'		XA=rp'
Carry flag manipulation	SET1	CY	1	1	CY<-1		
	CLR1	CY	1	1	CY<-0		
	SKT	CY	1	1+S	Skip if CY=1		CY=1
	NOT1	CY	1	1	CY<-$\overline{CY}$		
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit)<-1	*3	
		fmem.bit	2	2	(fmem.bit)<-1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))<-1	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit)<-1	*1	
	CLR1	mem.bit	2	2	(mem.bit)<-0	*3	
		fmem.bit	2	2	(fmem.bit)<-0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))<-0	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit)<-0	*1	
	SKT	mem.bit	2	2+S	Skip if(mem.bit)=1	*3	(mem.bit)=1
		fmem.bit	2	2+S	Skip if(fmem.bit)=1	*4	(fmem.bit)=1
		pmem.@L	2	2+S	Skip if(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=1	*5	(pmem.@L)=1
		@H+mem.bit	2	2+S	Skip if(H+mem$_{3-0}$.bit)=1	*1	(@H+mem.bit)=1
	SKF	mem.bit	2	2+S	Skip if(mem.bit)=0	*3	(mem.bit)=0
		fmem.bit	2	2+S	Skip if(fmem.bit)=0	*4	(fmem.bit)=0
		pmem.@L	2	2+S	Skip if(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=0	*5	(pmem.@L)=0
		@H+mem.bit	2	2+S	Skip if(H+mem$_{3-0}$.bit)=0	*1	(@H+mem.bit)=0
	SKTCLR	fmem.bit	2	2+S	Skip if(fmem.bit)=1 and clear	*4	(fmem.bit)=1
		pmem.@L	2	2+S	Skip if(pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$))=1 and clear	*5	(pmem.@L)=1
		@H+mem.bit	2	2+S	Skip if(H+mem$_{3-0}$.bit)=1 and clear	*1	(@H+mem.bit)=1
	AND1	CY, fmem.bit	2	2	CY<-CY∧(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY<-CY∧(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY<-CY∧(H+mem$_{3-0}$.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY<-CY∨(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY<-CY∨(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY<-CY∨(H+mem$_{3-0}$.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY<-CY∀ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY<- CY∀(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY<-CY∀(H+mem$_{3-0}$.bit)	*1	

Instruction group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Branch	BR[Note 1]	addr	—	—	PC_{13-0}<-addr (Use the assembler to select the most appropriate instruction among the following. • BR !addr • BRCB !caddr • BR $addr)	*6	
		addr1	—	—	PC_{13-0}<-addr1 (Use the assembler to select the most appropriate instruction among the following. • BRA !addr1 • BR !addr • BRCB !caddr • BR $addr1)	*11	
		!addr	3	3	PC_{13-0}<-addr	*6	
		$addr	1	2	PC_{13-0}<-addr	*7	
		$addr1	1	2	PC_{13-0}<-addr1		
		PCDE	2	3	PC_{13-0}<-PC_{13-8}+DE		
		PCXA	2	3	PC_{13-0}<-PC_{13-8}+XA		
		BCDE	2	3	PC_{13-0}<-BCDE[Note 2]	*6	
		BCXA	2	3	PC_{13-0}<-BCXA[Note 2]	*6	
	BRA[Note 1]	!addr1	3	3	PC_{13-0}<-addr1	*11	
	BRCB	!caddr	2	2	PC_{13-0}<-$PC_{13, 12}$+$caddr_{11-0}$	*8	

Notes 1. The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

2. Only the lower 2 bits in the B register are valid.

Instruction group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Subroutine stack control	CALLA[Note]	!addr1	3	3	(SP–6)(SP–3)(SP–4)<-PC_{11-0} (SP–5)<-0, 0, $PC_{13, 12}$ (SP–2)<-X, X, MBE, RBE PC_{13-0}<-addr1, SP<-SP–6	*11	
	CALL[Note]	!addr	3	3	(SP–4)(SP–1)(SP–2)<-PC_{11-0} (SP–3)<-MBE, RBE, $PC_{13, 12}$ PC_{13-0}<-addr, SP<-SP–4	*6	
				4	(SP–6)(SP–3)(SP–4)<-PC_{11-0} (SP–5)<-0, 0, $PC_{13, 12}$ (SP–2)<-X, X, MBE, RBE PC_{13-0}<-addr, SP<-SP–6		
	CALLF[Note]	!faddr	2	2	(SP–4)(SP–1)(SP–2)<-PC_{11-0} (SP–3)<-MBE, RBE, $PC_{13, 12}$ PC_{13-0}<-000+faddr, SP<-SP–4	*9	
				3	(SP–6)(SP–3)(SP–4)<-PC_{11-0} (SP–5)<-0, 0, $PC_{13, 12}$ (SP–2)<-X, X, MBE, RBE PC_{13-0}<-000+faddr, SP<-SP–6		
	RET[Note]		1	3	MBE, RBE, $PC_{13, 12}$<-(SP+1) PC_{11-0}<-(SP)(SP+3)(SP+2) SP<-SP+4		
					X, X, MBE, RBE<-(SP+4) PC_{11-0}<-(SP)(SP+3)(SP+2) 0, 0, $PC_{13, 12}$<-(SP+1) SP<-SP+6		
	RETS[Note]		1	3+S	MBE, RBE, $PC_{13, 12}$<-(SP+1) PC_{11-0}<-(SP)(SP+3)(SP+2) SP<-SP+4 then skip unconditionally		Unconditional
					X, X, MBE, RBE<-(SP+4) PC_{11-0}<-(SP)(SP+3)(SP+2) 0, 0, $PC_{13, 12}$<-(SP+1) SP<-SP+6 then skip unconditionally		
	RETI[Note]		1	3	MBE, RBE, $PC_{13, 12}$<-(SP+1) PC_{11-0}<-(SP)(SP+3)(SP+2) PSW<-(SP+4)(SP+5), SP<-SP+6		
					0, 0, $PC_{13, 12}$<-(SP+1) PC_{11-0}<-(SP)(SP+3)(SP+2) PSW<-(SP+4)(SP+5), SP<-SP+6		

Note The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

Instruction group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Subroutine stack control	PUSH	rp	1	1	(SP–1)(SP–2)<-rp, SP<-SP–2		
		BS	2	2	(SP–1)<-MBS, (SP–2)<-RBS, SP<-SP–2		
	POP	rp	1	1	rp<-(SP+1)(SP), SP<-SP+2		
		BS	2	2	MBS<-(SP+1), RBS<-(SP), SP<-SP+2		
Interrupt control	EI		2	2	IME(IPS.3)<-1		
		IEXXX	2	2	IEXXX<-1		
	DI		2	2	IME(IPS.3)<-0		
		IEXXX	2	2	IEXXX<-0		
I/O	IN[Note 1]	A, PORTn	2	2	A<-PORTn (n=0-8)		
		XA, PORTn	2	2	XA<-PORTn+1, PORTn (n=4, 6)		
	OUT[Note 1]	PORTn, A	2	2	PORTn<-A (n=2-8)		
		PORTn, XA	2	2	PORTn+1, PORTn<-XA (n=4, 6)		
CPU control	HALT		2	2	Set HALT Mode(PCC.2<-1)		
	STOP		2	2	Set STOP Mode(PCC.3<-1)	*10	
	NOP		1	1	No Operation		
Special	SEL	RBn	2	2	RBS<-n (n=0-3)		
		MBn	2	2	MBS<-n (n=0-2, 15)		
	GETI[Note 2, 3]	taddr	1	3	• When using TBR instruction PC13-0<-(taddr)5-0+(taddr+1)		
					• When using TCALL instruction (SP–4)(SP–1)(SP–2)<-PC11-0 (SP–3)<-MBE, RBE, PC13, 12 PC13-0<-(taddr)5-0+(taddr+1) SP<-SP–4		
					• When using instruction other than TBR or TCALL Execute (taddr)(taddr+1) instruction		Determined by referenced instruction
			1	3	• When using TBR instruction PC13-0<-(taddr)5-0+(taddr+1)	*10	
				4	• When using TCALL instruction (SP–6)(SP–3)(SP–4)<-PC11-0 (SP–5)<-MBE, RBE, PC13, 12 (SP–2)<-X, X, MBE, RBE PC13-0<-(taddr)5-0+(taddr+1) SP<-SP–6		
				3	• When using instruction other than TBR or TCALL Execute (taddr)(taddr+1) instruction		Determined by referenced instruction

Notes 1. Before executing the IN or OUT instruction, set MBE to 0 or 1 and set MBS to 15.

2. TBR and TCALL instructions are assembler pseudo-instructions for the GETI instruction's table definitions.

3. The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

8. PROM (PROGRAM MEMORY) WRITE AND VERIFY

The μPD75P3036 contains a 16384 x 8-bit PROM as a program memory. The pins listed in the table below are used for this PROM's write/verify operations. Clock input from the X1 pin is used instead of address input as a method for updating addresses.

Pin	Function
V_{PP}	Pin where program voltage is applied during program memory write/verify (usually V_{DD} potential)
X1, X2	Clock input pins for address updating during program memory write/verify. Input the X1 pin's inverted signal to the X2 pin.
MD0 to MD3	Operation mode selection pin for program memory write/verify
D0/P40 to D3/P43 (lower 4 bits) D4/P50 to D7/P53 (upper 4 bits)	8-bit data I/O pins for program memory write/verify
V_{DD}	Pin where power supply voltage is applied. Applies 1.8 to 5.5 V in normal operation mode and +6 V for program memory write/verify.

Caution Pins not used for program memory write/verify should be connected to V_{SS}.

8.1 Operation Modes for Program Memory Write/Verify

When +6 V is applied to the V_{DD} pin and +12.5 V to the V_{PP} pin, the μPD75P3036 enters the program memory write/verify mode. The following operation modes can be specified by setting pins MD0 to MD3 as shown below.

Operation mode specification						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Zero-clear program memory address
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

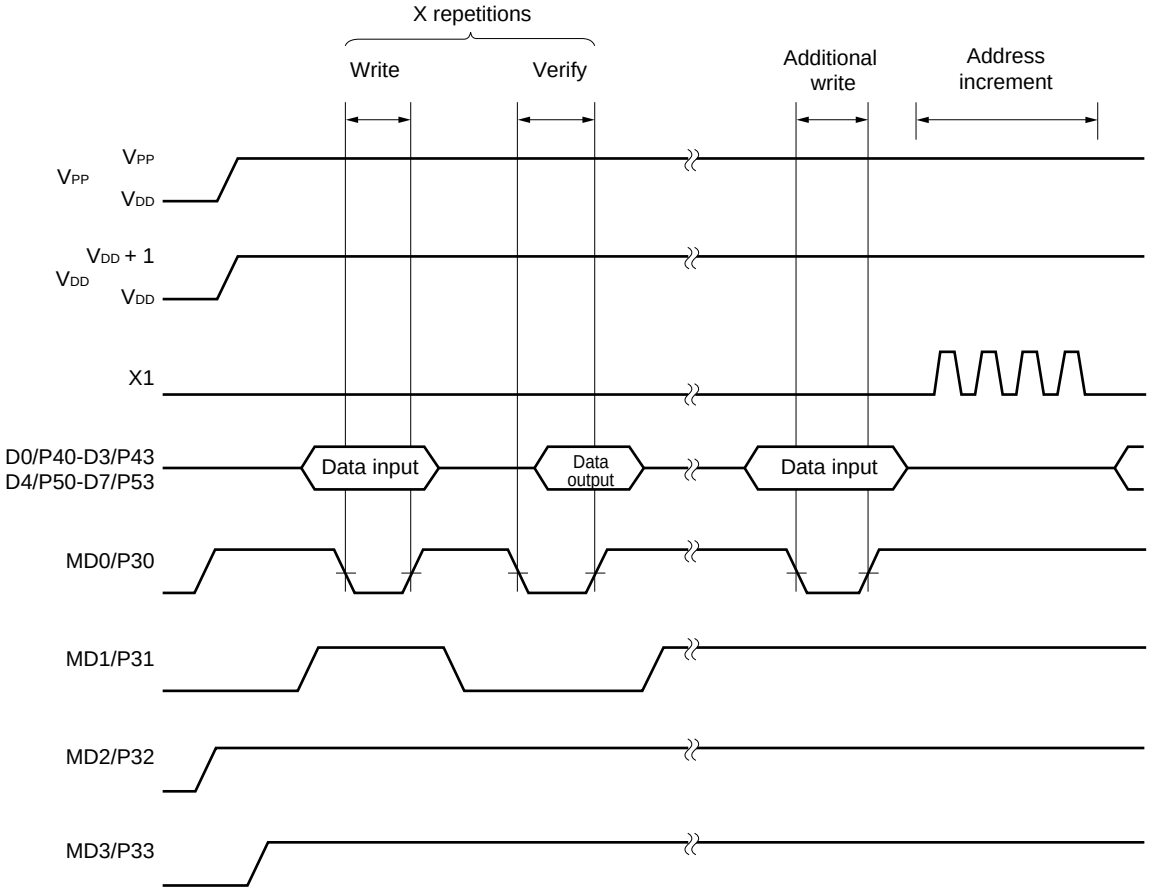
X: L or H

* **8.2 Program Memory Write Procedure**

Program memory can be written at high speed using the following procedure.

(1) Pull unused pins to V_{SS} through resistors. Set the X1 pin low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Select the zero-clear program memory address mode.
(5) Supply 6 V to the V_{DD} and 12.5 V to the V_{PP} pins.
(6) Write data in the 1 ms write mode.
(7) Select the verify mode. If the data is correct, go to step (8) and if not, repeat steps (6) and (7).
(8) (X : number of write operations from steps (6) and (7)) x 1 ms additional write.
(9) Apply four pulses to the X1 pin to increment the program memory address by one.
(10) Repeat steps (6) to (9) until the end address is reached.
(11) Select the zero-clear program memory address mode.
(12) Return the V_{DD} and V_{PP} pins back to 5 V.
(13) Turn off the power.

The following figure shows steps (2) to (9).

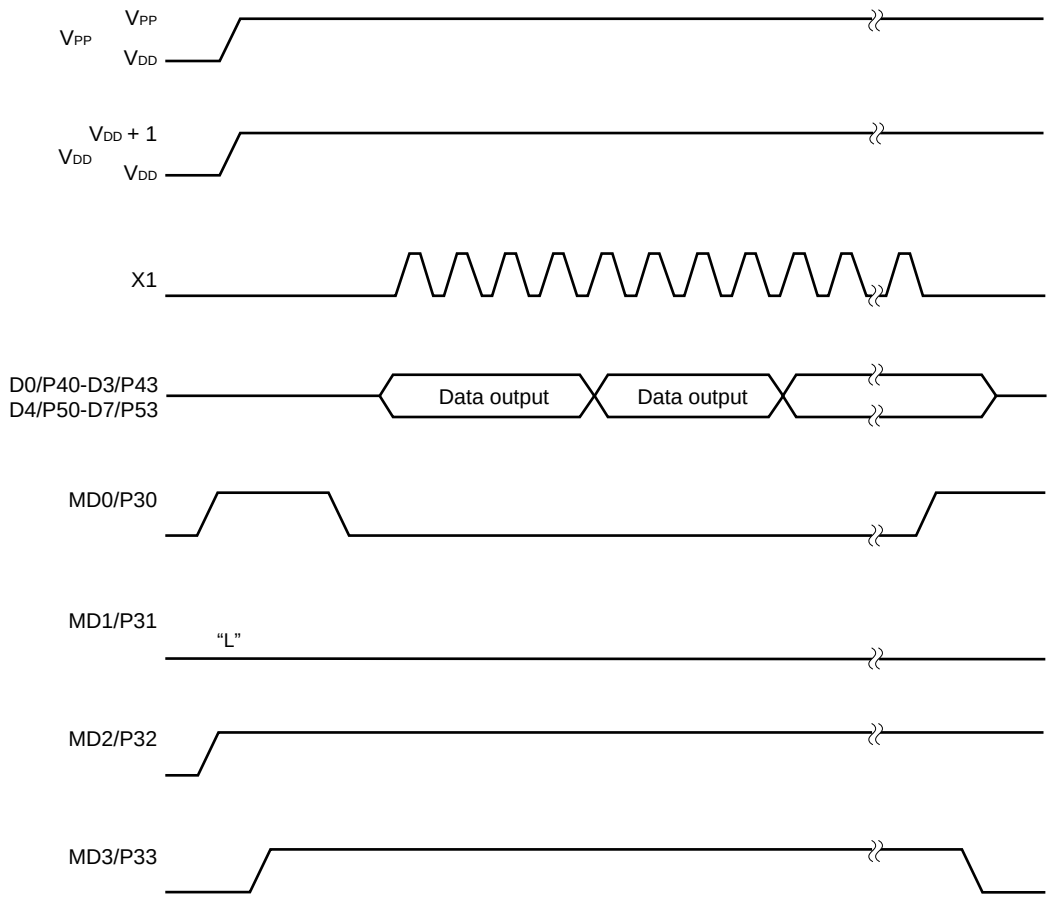


★ 8.3 Program Memory Read Procedure

The μPD75P3036 can read program memory contents using the following procedure.

(1) Pull unused pins to V_{SS} through resistors. Set the X1 pin low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Select the zero-clear program memory address mode.
(5) Supply 6 V to the V_{DD} and 12.5 V to the V_{PP} pins.
(6) Select the verify mode. Apply four clock pulses to the X1 pin. Every four clock pulses will output the data stored in one address.
(7) Select the zero-clear program memory address mode.
(8) Return the V_{DD} and V_{PP} pins back to 5 V.
(9) Turn off the power.

The following figure shows steps (2) to (7).



* 9. PROGRAM ERASURE (μPD75P3036KK-T ONLY)

The μPD75P3036KK-T is capable of erasing (FFH) the data written in a program memory and rewriting.
To erase the programmed data, expose the erasure window to light having a wavelength shorter than about 400 nm. Normally, irradiate ultraviolet rays of 254-nm wavelength. The amount of exposure required to completely erase the programmed data is as follows:

- UV intensity x erasure time : 15 W• s/cm^2 or more
- Erasure time : 15 to 20 minutes (when a UV lamp of 12000 μW/cm^2 is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, soiled erasure window, etc.)

When erasing the contents of data, set up the UV lamp within 2.5 cm from the erasure window. Further, if a filter is provided for a UV lamp, irrradiate the ultraviolet rays after removing the filter.

* 10. OPAQUE FILM ON ERASURE WINDOW (μPD75P3036KK-T ONLY)

To protect from unintentional erasure by rays other than that of the lamp for erasing EPROM contents, and to protect internal circuit other than EPROM from misoperating due to light radiation, cover the erasure window with an opaque film when EPROM contents erasure is not performed.

11. ONE-TIME PROM SCREENING

Due to its structure, the one-time PROM versions (μPD75P3036GC-3B9, μPD75P3036GK-BE9) cannot be fully tested before shipment by NEC. Therefore, NEC recommends that after the required data is written and the PROM is stored under the temperature and time conditions shown below, the PROM should be verified via a screening.

Storage temperature	Storage time
125 ˚C	24 hours

∗ 12. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
PROM supply voltage	V_{PP}			–0.3 to +13.5	V
Input voltage	V_{I1}	Other than ports 4, 5		–0.3 to V_{DD} +0.3	V
	V_{I2}	Ports 4, 5	N-ch open drain	–0.3 to +14	V
Output voltage	V_O			–0.3 to V_{DD} +0.3	V
High-level output current	I_{OH}	Per pin		–10	mA
		Total of all pins		–30	mA
Low-level output current	I_{OL}	Per pin		30	mA
		Total of all pins		200	mA
Operating ambient temperature	T_A			–40 to +85[Note]	˚C
Storage temperature	T_{stg}			–65 to +150	˚C

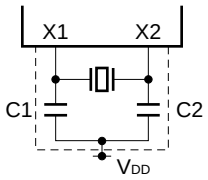
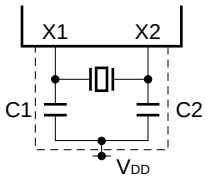
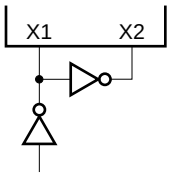
Note To drive LCD at 1.8 V ≤ V_{DD} < 2.7 V, T_A = –10 to +85 °C

Caution If the absolute maximum ratings of even one of the parameters is exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings are therefore values which, when exceeded, can cause the product to be damaged. Be sure that these values are never exceeded when using the product.

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C_{IO}				15	pF

Main System Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Constants	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1		1.0		6.0Note 2	MHz
		Oscillation stabilization timeNote 3	After V_{DD} has reached MIN. value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1.0		6.0Note 2	MHz
		Oscillation stabilization timeNote 3	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X)Note 1		1.0		6.0Note 2	MHz
		X1 input high-, low-level widths (t_{XH}, t_{XL})		83.3		500	ns

Notes 1. The oscillation frequency and X1 input frequency shown above indicate characteristics of the oscillation circuit only. For the instruction execution time, refer to AC Characteristics.

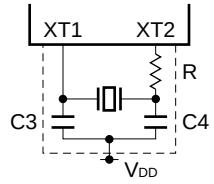
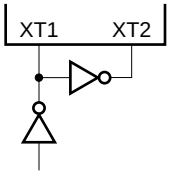
2. If the oscillation frequency is 4.19 MHz < f_X ≤ 6.0 MHz at 1.8 V ≤ V_{DD} < 2.7 V, do not select the processor clock control register (PCC) = 0011. If PCC = 0011, one machine cycle time is less than 0.95 μs, falling short of the rated value of 0.95 μs.

3. The oscillation stabilization time is the time required for oscillation to be stabilized after V_{DD} has been applied or STOP mode has been released.

Caution When using the main system clock oscillation circuit, wire the portion enclosed in the dotted line in the above figure as follows to prevent adverse influence due to wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{DD}.**
- **Do not ground to a power supply pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

Subsystem Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Constants	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V		1.0	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		100	kHz
		XT1 input high-, low-level widths (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. The oscillation frequency shown above indicate characteristics of the oscillation circuit only. For the instruction execution time, refer to AC Characteristics.

2. The oscillation stabilization time is the time required for oscillation to be stabilized after V_{DD} has been applied.

Caution When using the subsystem clock oscillation circuit, wire the portion enclosed in the dotted line in the above figure as follows to prevent adverse influence due to wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{DD}.**
- **Do not ground to a power supply pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

The subsystem clock oscillation circuit has a low amplification factor to reduce current dissipation and is more susceptible to noise than the main system clock oscillation circuit. Therefore, exercise utmost care in wiring the subsystem clock oscillation circuit.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Low-level output current	I_{OL}	Per pin					15	mA
		Total of all pins					120	mA
High-level input voltage	V_{IH1}	Ports 2, 3, P82, P83		2.7 V ≤ V_{DD} ≤ 5.5 V	0.7 V_{DD}		V_{DD}	V
				1.8 V ≤ V_{DD} < 2.7 V	0.9 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, P80, P81, $\overline{RESET}$		2.7 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
				1.8 V ≤ V_{DD} < 2.7 V	0.9 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4, 5	N-ch open drain	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7 V_{DD}		13	V
				1.8 V ≤ V_{DD} < 2.7 V	0.9 V_{DD}		13	V
	V_{IH4}	X1, XT1			V_{DD}–0.1		V_{DD}	V
Low-level input voltage	V_{IL1}	Ports 2, 3, 4, 5, P82, P83		2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
				1.8 V ≤ V_{DD} < 2.7 V	0		0.1 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, P80, P81, $\overline{RESET}$		2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
				1.8 V ≤ V_{DD} < 2.7 V	0		0.1 V_{DD}	V
	V_{IL3}	X1, XT1			0		0.1	V
High-level output voltage	V_{OH}	$\overline{SCK}$, SO, ports 2, 3, 6, 7, 8, BP0 to BP7 I_{OH} = –1 mA			V_{DD}–0.5			V
Low-level output voltage	V_{OL1}	$\overline{SCK}$, SO, ports 2 to 8, BP0 to BP7		I_{OL} = 15 mA V_{DD} = 4.5 to 5.5 V		0.2	2.0	V
				I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1	N-ch open drain Pull-up resistor ≥ 1 kΩ				0.2 V_{DD}	V
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	Pins other than X1, XT1				3	μA
	I_{LIH2}		X1, XT1				20	μA
	I_{LIH3}	V_{IN} = 13 V	Ports 4, 5 (N-ch open drain)				20	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	Pins other than ports 4, 5, X1, XT1				–3	μA
	I_{LIL2}		X1, XT1				–20	μA
			Ports 4, 5 (N-ch open drain) When input instruction is not executed				–3	μA
	I_{LIL3}		Ports 4, 5 (N-ch open drain) When input instruction is executed				–30	μA
				V_{DD} = 5 V		–10	–27	μA
				V_{DD} = 3 V		–3	–8	μA
High-level output leakage current	I_{LOH1}	V_{OUT} = V_{DD}	$\overline{SCK}$, SO/SB0, SB1, ports 2, 3, 6, 7, 8, BP0 to BP7				3	μA
	I_{LOH2}	V_{OUT} = 13 V	Ports 4, 5 (N-ch open drain)				20	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V					–3	μA
Internal pull-up resistor	R_{L1}	V_{IN} = 0 V	Ports 0 to 3, 6 to 8 (except pin P00)		50	100	200	kΩ

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	VAC0 = 0	–40 to + 85 °C			2.7		V_{DD}	V
			–10 to + 85 °C			2.2		V_{DD}	V
		VAC0 = 1				1.8		V_{DD}	V
VAC current[Note 1]	I_{VAC}	VAC0 = 1, V_{DD} = 2.0 V ±10 %					1	4	μA
LCD output voltage deviation[Note 2] (common)	V_{ODC}	I_O = ±1.0 μA	$V_{LCD0} = V_{LCD}$ $V_{LCD1} = V_{LCD} \times 2/3$ $V_{LCD2} = V_{LCD} \times 1/3$ 1.8 V ≤ V_{LCD} ≤ V_{DD}[Note 1]			0		±0.2	V
LCD output voltage deviation[Note 2] (segment)	V_{ODS}	I_O = ±0.5 μA				0		±0.2	V
Supply current[Notes 1, 3]	I_{DD1}	6.00 MHz[Note 4] crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5.0 V ±10 %[Note 5]				3.5	10.5	mA
			V_{DD} = 3.0 V ±10 %[Note 6]				0.86	2.5	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ±10 %			0.9	2.7	mA
				V_{DD} = 3.0 V ±10 %			0.5	1.0	mA
	I_{DD1}	4.19 MHz[Note 4] crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5.0 V ±10 %[Note 5]				2.7	8.1	mA
			V_{DD} = 3.0 V ±10 %[Note 6]				0.33	1.0	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ±10 %			0.7	2.0	mA
				V_{DD} = 3.0 V ±10 %			0.3	0.9	mA
	I_{DD3}	32.768 kHz[Note 7] crystal oscillation	Low-voltage mode[Note 8]	V_{DD} = 3.0 V ±10 %			45	135	μA
				V_{DD} = 2.0 V ±10 %			22	66	μA
				V_{DD} = 3.0 V, T_A = 25 °C			45	90	μA
			Low current dissipation mode[Note 9]	V_{DD} = 3.0 V ±10 %			43	129	μA
				V_{DD} = 3.0 V, T_A = 25 °C			43	86	μA
	I_{DD4}		HALT mode	Low-voltage mode[Note 8]	V_{DD} = 3.0 V ±10 %		8.5	25	μA
					V_{DD} = 2.0 V ±10 %		3.0	9.0	μA
					V_{DD} = 3.0 V, T_A = 25 °C		8.5	17	μA
				Low current dissipation mode[Note 9]	V_{DD} = 3.0 V ±10 %		4.6	13.8	μA
					V_{DD} = 3.0 V, T_A = 25 °C		4.6	9.2	μA
	I_{DD5}	XT1 = 0 V[Note 10] STOP mode	V_{DD} = 5.0 V ±10 %				0.05	10	μA
			V_{DD} = 3.0 V ±10 %				0.02	5.0	μA
				T_A = 25 °C			0.02	3.0	μA

Notes 1. Clear VAC0 to 0 in the low current dissipation mode and STOP mode. When VAC0 is set to 1, the current increases by about 1 μA.

2. Voltage deviation is the difference between the ideal values (V_{LCDn}; n = 0, 1, 2) of the segment and common outputs and the output voltage.

3. The current flowing through the internal pull-up resistor is not included.

4. Including the case when the subsystem clock oscillates.

5. When the device operates in high-speed mode with the processor clock control register (PCC) set to 0011.

6. When the device operates in low-speed mode with PCC set to 0000.

7. When the device operates on the subsystem clock, with the system clock control register (SCC) set to 1001 and oscillation of the main system clock stopped.

8. When the sub-oscillation circuit control register (SOS) is set to 0000.

9. When SOS is set to 0010.

10. When SOS is set to 00×1, and the feedback resistor of the sub-oscillation circuit is not used (× : don't care).

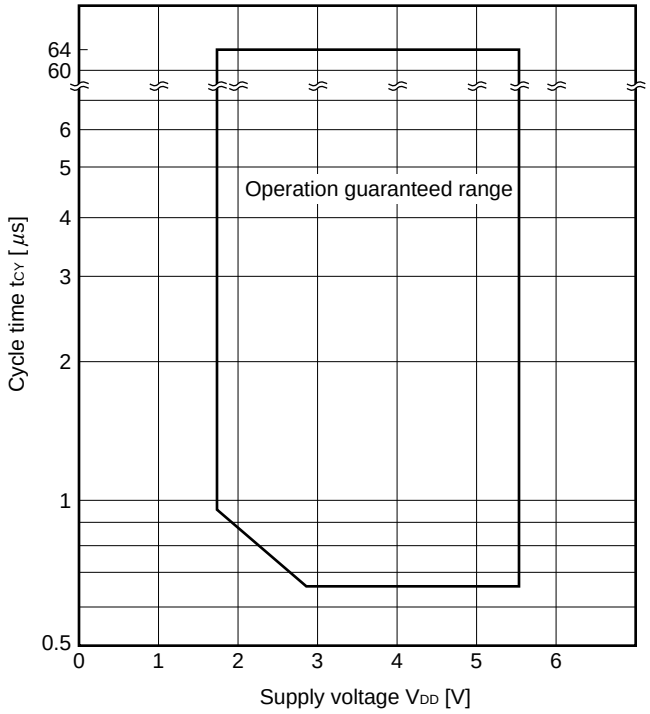
AC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time[Note 1] (minimum instruction execution time = 1 machine cycle)	t_{CY}	Operates with main system clock	V_{DD} = 2.7 to 5.5 V	0.67		64	μs
				0.95		64	μs
		Operates with subsystem clock		114	122	125	μs
TI0, TI1, TI2 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		1.0	MHz
				0		275	kHz
TI0, TI1, TI2 high-, low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.48			μs
				1.8			μs
Interrupt input high-, low-level widths	t_{INTH}, t_{INTL}	INT0	IM02 = 0	**Note 2**			μs
			IM02 = 1	10			μs
		INT1, 2, 4		10			μs
		KR0 to KR7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes 1. The cycle time of the CPU clock (Φ) is determined by the oscillation frequency of the connected resonator (and external clock), the system clock control register (SCC), and processor clock control register (PCC).
The figure on the right shows the supply voltage V_{DD} vs. cycle time t_{CY} characteristics when the device operates with the main system clock.

2. $2t_{CY}$ or $128/f_X$ depending on the setting of the interrupt mode register (IM0).

t_{CY} vs V_{DD}
(with main system clock)



Serial transfer operation

2-wire and 3-wire serial I/O modes ($\overline{SCK}$ ··· internal clock output): (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high-, low-level widths	t_{KL1},	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
	t_{KH1}			t_{KCY1}/2–150			ns
SI[Note 1] setup time (to $\overline{SCK}$ ↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI[Note 1] hold time	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
(from $\overline{SCK}$ ↑)				600			ns
$\overline{SCK}$ ↓ → SO[Note 1] output	t_{KSO1}	R_L = 1 kΩ, [Note 2]	V_{DD} = 2.7 to 5.5 V	0		250	ns
delay time		C_L = 100 pF		0		1000	ns

Notes 1. Read as SB0 or SB1 when using the 2-wire serial I/O mode.

2. R_L and C_L respectively indicate the load resistance and load capacitance of the SO output line.

2-wire and 3-wire serial I/O modes ($\overline{SCK}$ ··· external clock input): (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high-, low-level widths	t_{KL2},	V_{DD} = 2.7 to 5.5 V		400			ns
	t_{KH2}			1600			ns
SI[Note 1] setup time (to $\overline{SCK}$ ↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI[Note 1] hold time	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
(from $\overline{SCK}$ ↑)				600			ns
$\overline{SCK}$ ↓ → SO[Note 1] output	t_{KSO2}	R_L = 1 kΩ, [Note 2]	V_{DD} = 2.7 to 5.5 V	0		300	ns
delay time		C_L = 100 pF		0		1000	ns

Notes 1. Read as SB0 or SB1 when using the 2-wire serial I/O mode.

2. R_L and C_L respectively indicate the load resistance and load capacitance of the SO output line.

SBI mode ($\overline{SCK}$ ··· internal clock output (master)): (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high-, low-level widths	t_{KL3},	V_{DD} = 2.7 to 5.5 V		t_{KCY3}/2–50			ns
	t_{KH3}			t_{KCY3}/2–150			ns
SB0, 1 setup time	t_{SIK3}	V_{DD} = 2.7 to 5.5 V		150			ns
(to $\overline{SCK}$ ↑)				500			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
$\overline{SCK}$ ↓ → SB0, 1 output	t_{KSO3}	R_L = 1 kΩ, Note	V_{DD} = 2.7 to 5.5 V	0		250	ns
delay time		C_L = 100 pF		0		1000	ns
$\overline{SCK}$ ↑ → SB0, 1 ↓	t_{KSB}			t_{KCY3}			ns
SB0, 1 ↓ → $\overline{SCK}$ ↓	t_{SBK}			t_{KCY3}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY3}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY3}			ns

Note R_L and C_L respectively indicate the load resistance and load capacitance of the SB0, 1 output line.

SBI mode ($\overline{SCK}$ ··· external clock input (slave)): (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high-, low-level widths	t_{KL4},	V_{DD} = 2.7 to 5.5 V		400			ns
	t_{KH4}			1600			ns
SB0, 1 setup time	t_{SIK4}	V_{DD} = 2.7 to 5.5 V		100			ns
(to $\overline{SCK}$ ↑)				150			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
$\overline{SCK}$ ↓ → SB0, 1 output	t_{KSO4}	R_L = 1 kΩ, Note	V_{DD} = 2.7 to 5.5 V	0		300	ns
delay time		C_L = 100 pF		0		1000	ns
$\overline{SCK}$ ↑ → SB0, 1 ↓	t_{KSB}			t_{KCY4}			ns
SB0, 1 ↓ → $\overline{SCK}$ ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY4}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY4}			ns

Note R_L and C_L respectively indicate the load resistance and load capacitance of the SB0, 1 output line.

A/D Converter Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Absolute accuracy[Note 1]		V_{DD} = AV_{REF}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.5	LSB
			1.8 V ≤ V_{DD} < 2.7 V			3	LSB
		V_{DD} ≠ AV_{REF}				3	LSB
Conversion time	t_{CONV}	**Note 2**				168/f_X	μs
Sampling time	t_{SAMP}	**Note 3**				44/f_X	μs
Analog input voltage	V_{IAN}			AV_{SS}		AV_{REF}	V
Analog input impedance	R_{AN}				1000		MΩ
AV_{REF} current	I_{REF}				0.25	2.0	mA

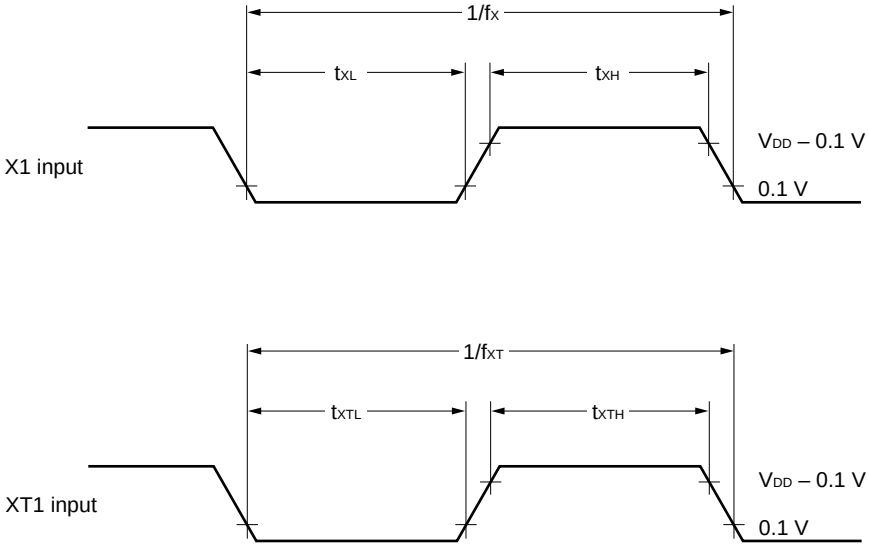
Notes 1. Absolute accuracy excluding quantization error (±1/2LSB)

2. Time until end of conversion (EOC = 1) after execution of conversion start instruction (40.1 μs: f_X = 4.19 MHz).

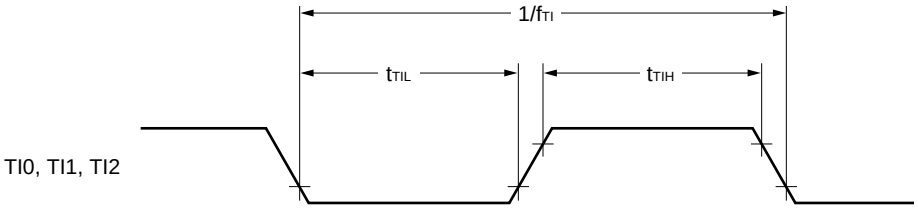
3. Time until end of sampling after execution of conversion start instruction (10.5 μs: f_X = 4.19 MHz).

AC timing test points (except X1 and XT1 inputs)

Clock timing

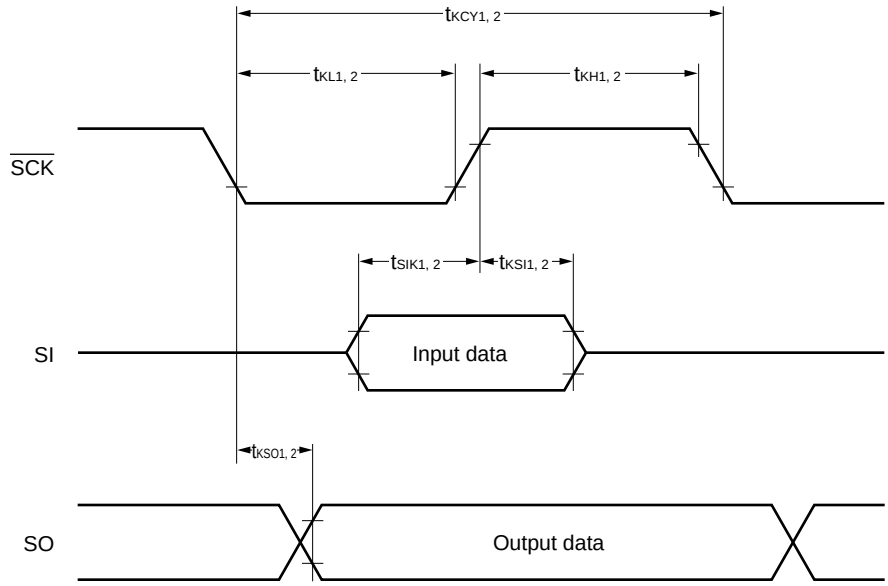


TI0, TI1, TI2 timing

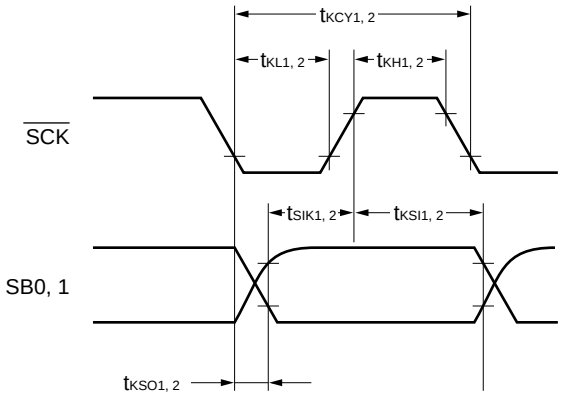


Serial transfer timing

3-wire serial I/O mode

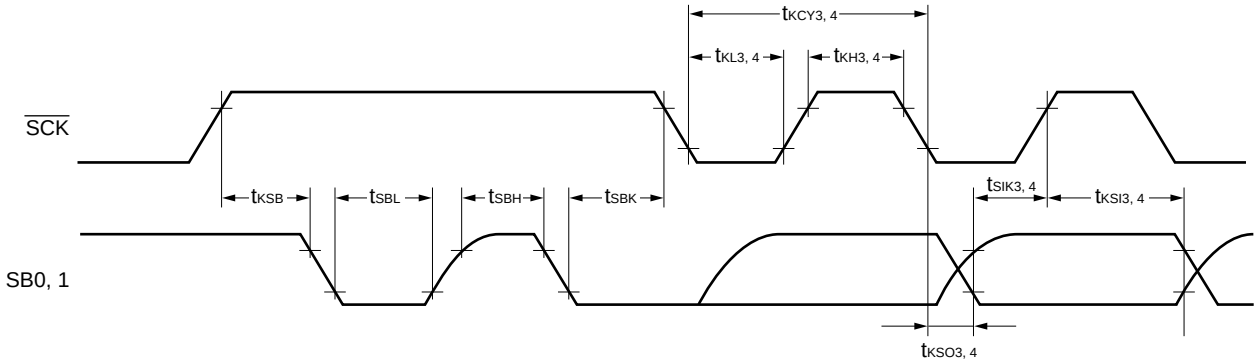


2-wire serial I/O mode

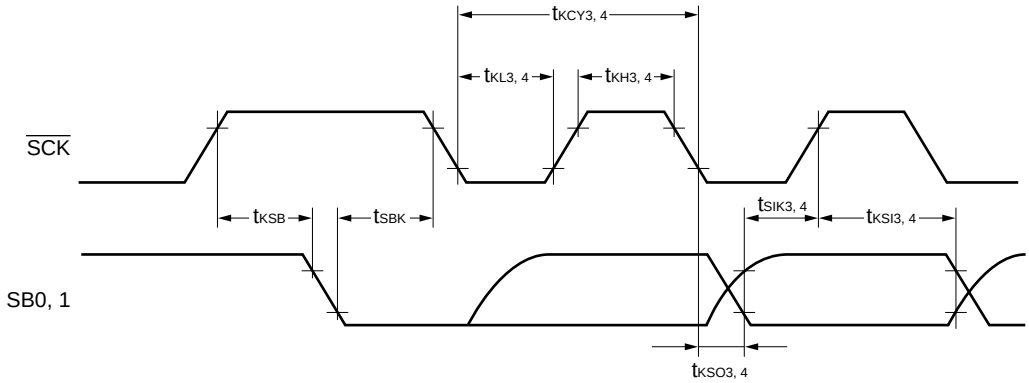


Serial transfer timing

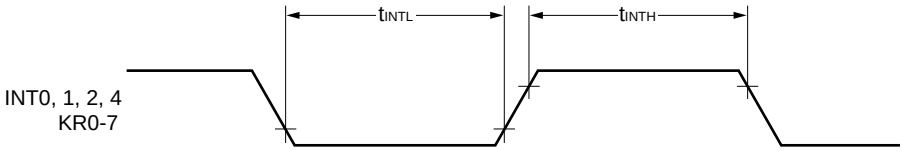
Bus release signal transfer



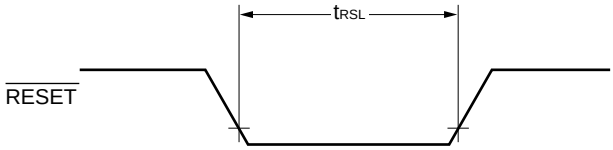
Command signal transfer



Interrupt input timing



$\overline{\text{RESET}}$ input timing



Data retention characteristics of data memory in STOP mode and at low supply voltage (T_A = –40 to +85 °C)

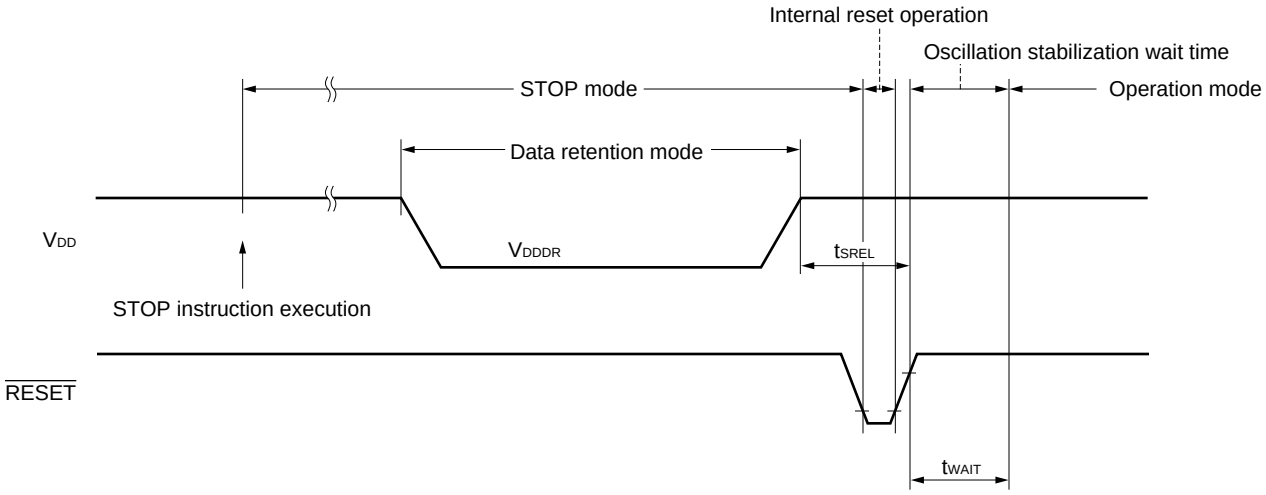
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Released by $\overline{\text{RESET}}$		$2^{15}/f_X$		ms
		Released by interrupt request		**Note 2**		ms

Notes 1. The oscillation stabilization wait time is the time during which the CPU stops operating to prevent unstable operation when oscillation is started.

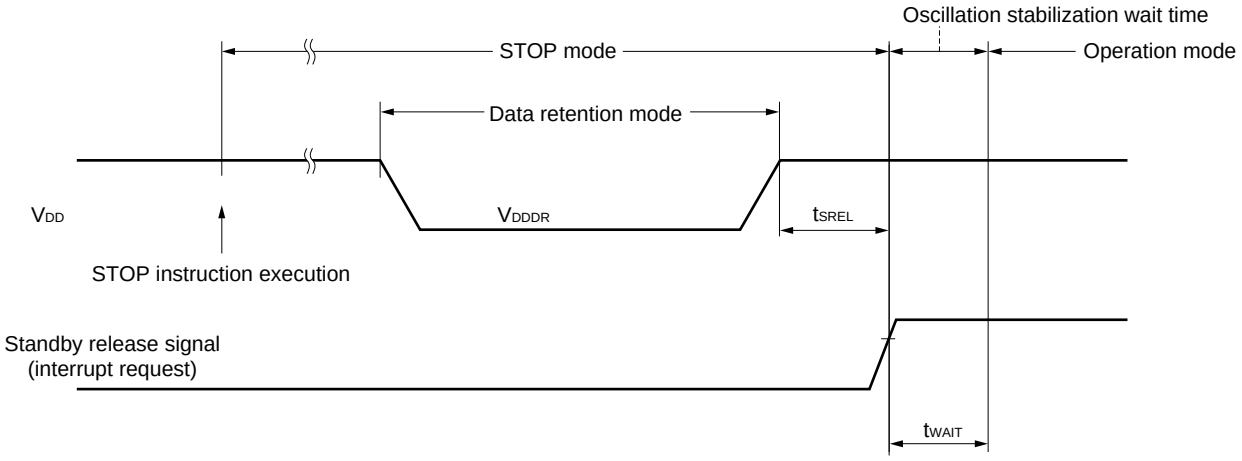
2. Set by the basic interval timer mode register (BTM). (Refer to the table below.)

BTM3	BTM2	BTM1	BTM0	Wait Time	
				f_X = 4.19 MHz	f_X = 6.0 MHz
–	0	0	0	$2^{20}/f_X$ (approx. 250 ms)	$2^{20}/f_X$ (approx. 175 ms)
–	0	1	1	$2^{17}/f_X$ (approx. 31.3 ms)	$2^{17}/f_X$ (approx. 21.8 ms)
–	1	0	1	$2^{15}/f_X$ (approx. 7.81 ms)	$2^{15}/f_X$ (approx. 5.46 ms)
–	1	1	1	$2^{13}/f_X$ (approx. 1.95 ms)	$2^{13}/f_X$ (approx. 1.37 ms)

Data retention timing (when STOP mode released by $\overline{\text{RESET}}$)



Data retention timing (standby release signal: when STOP mode released by interrupt signal)



DC Programming Characteristics (T_A = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	Except X1, X2	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD}–0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	Except X1, X2	0		0.3 V_{DD}	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
High-level output voltage	V_{OH}	I_{OH} = –1 mA	V_{DD}–1.0			V
Low-level output voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Cautions 1. Ensure that V_{PP} does not exceed +13.5 V including overshoot.

2. V_{DD} must be applied before V_{PP}, and cut after V_{PP}.

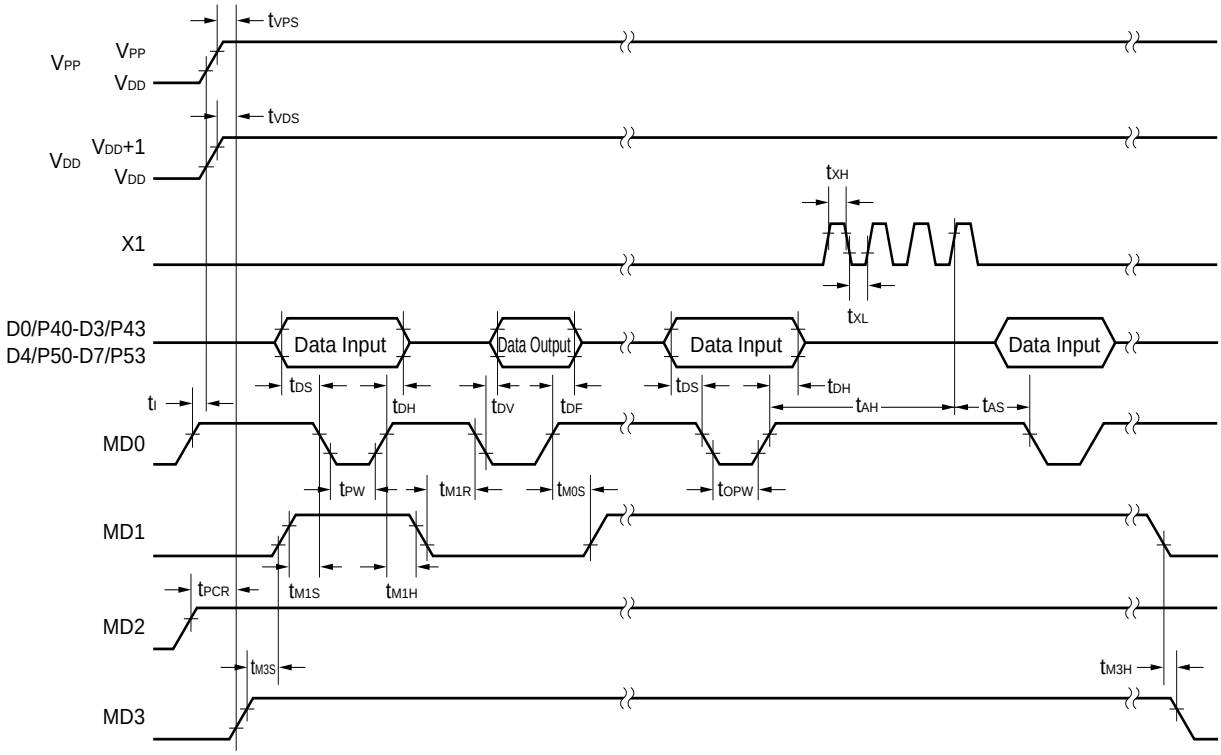
AC Programming Characteristics (T_A = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	**Note 1**	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time[Note 2] (to MD0↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (to MD0↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (to MD0↓)	t_{DS}	t_{DS}		2			μs
Address hold time[Note 2] (from MD0↑)	t_{AH}	t_{AH}		2			μs
Data hold time (from MD0↑)	t_{DH}	t_{DH}		2			μs
MD0↑→Data output float delay time	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (to MD3↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (to MD3↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1↑)	t_{M0S}	t_{CES}		2			μs
MD0↓→Data output delay time	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (from MD0↑)	t_{M1H}	t_{OEH}	t_{M1H} + t_{M1R} ≥ 50 μs	2			μs
MD1 recovery time (from MD0↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	—		10			μs
X1 input high-, low-level widths	t_{XH}, t_{XL}	—		0.125			μs
X1 input frequency	f_X	—				4.19	MHz
Initial mode setting time	t_I	—		2			μs
MD3 setup time (to MD1↑)	t_{M3S}	—		2			μs
MD3 hold time (from MD1↓)	t_{M3H}	—		2			μs
MD3 setup time (to MD0↓)	t_{M3SR}	—	Program memory read	2			μs
Data output delay time from address[Note 2]	t_{DAD}	t_{ACC}	Program memory read			2	μs
Data output hold time from address[Note 2]	t_{HAD}	t_{OH}	Program memory read	0		130	μs
MD3 hold time (from MD0↑)	t_{M3HR}	—	Program memory read	2			μs
MD3↓→Data output float delay time	t_{DFR}	—	Program memory read			2	μs

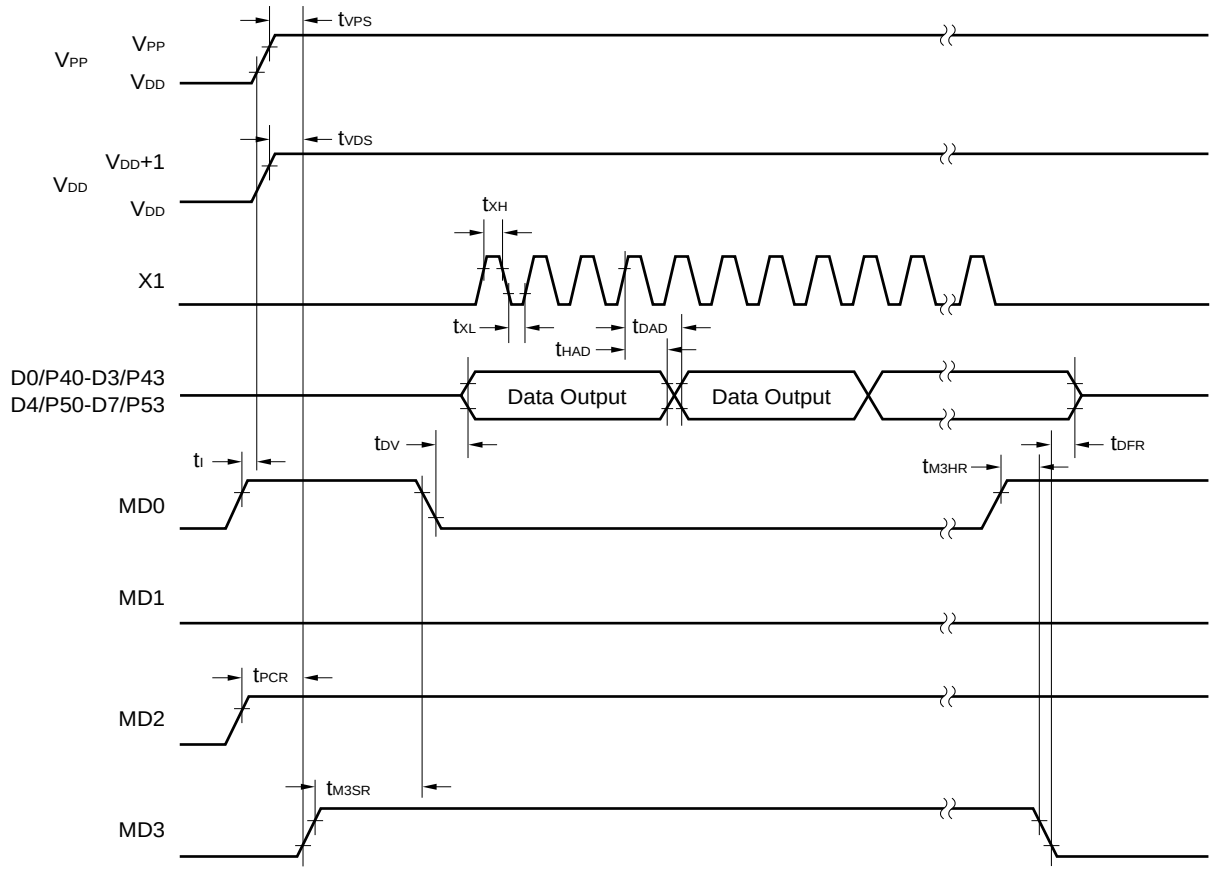
Notes 1. Symbol of corresponding μPD27C256A

2. The internal address signal is incremented by 1 on the 4th rise of the X1 input, and is not connected to a pin.

Program Memory Write Timing

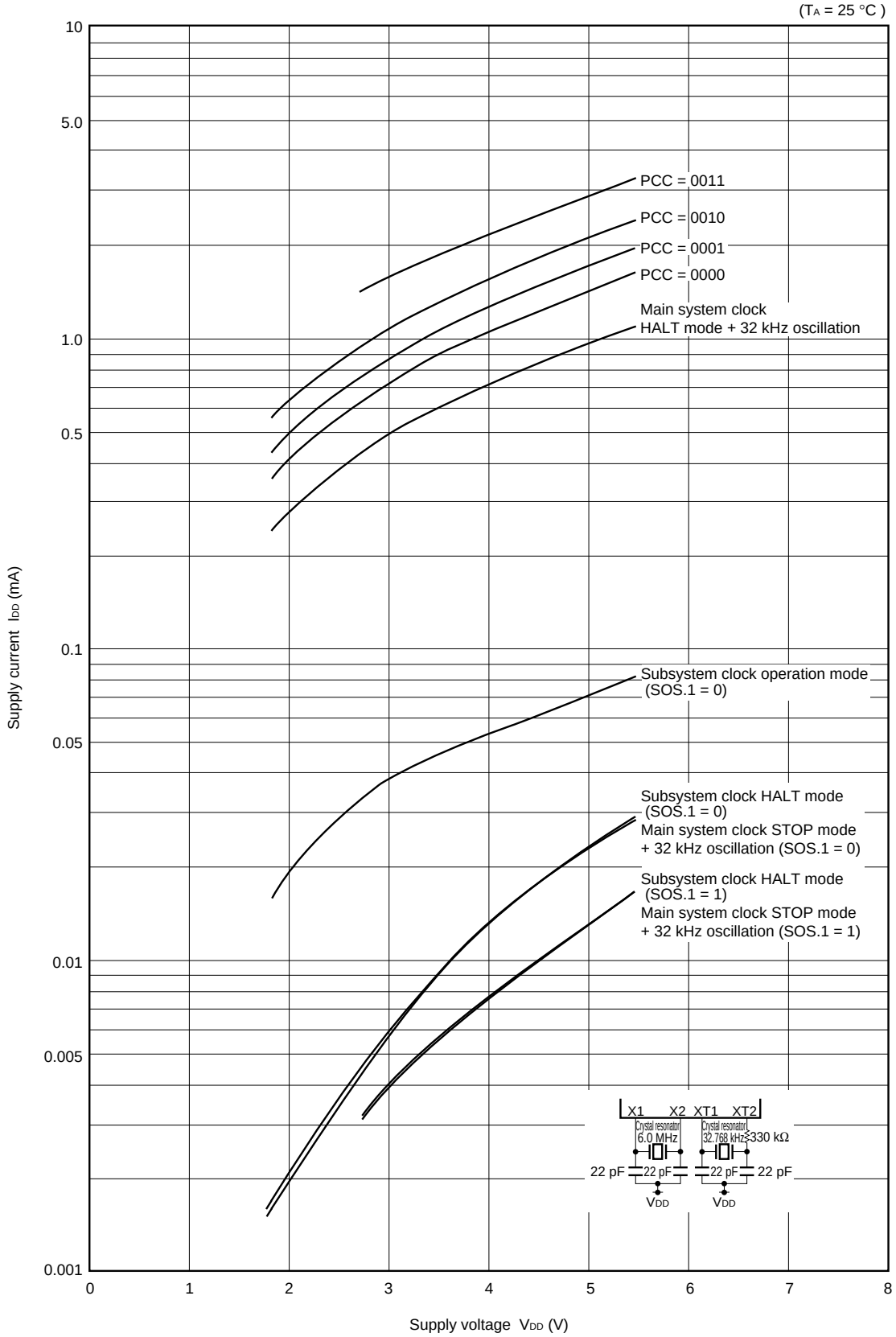


Program Memory Read Timing

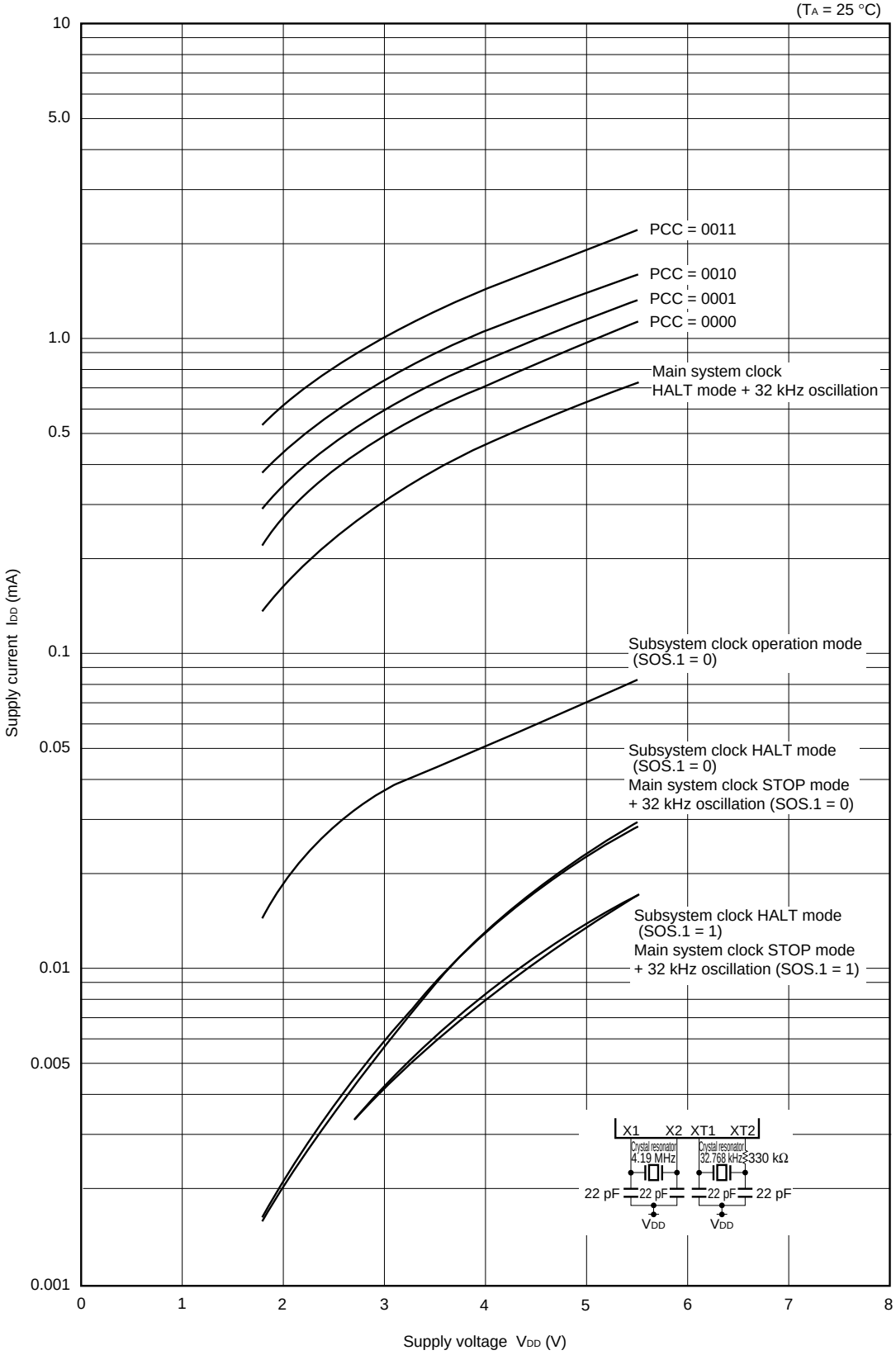


* 13. CHARACTERISTIC CURVES (FOR REFERENCE ONLY)

I_{DD} vs. V_{DD} (main system clock: 6.0-MHz crystal resonator)

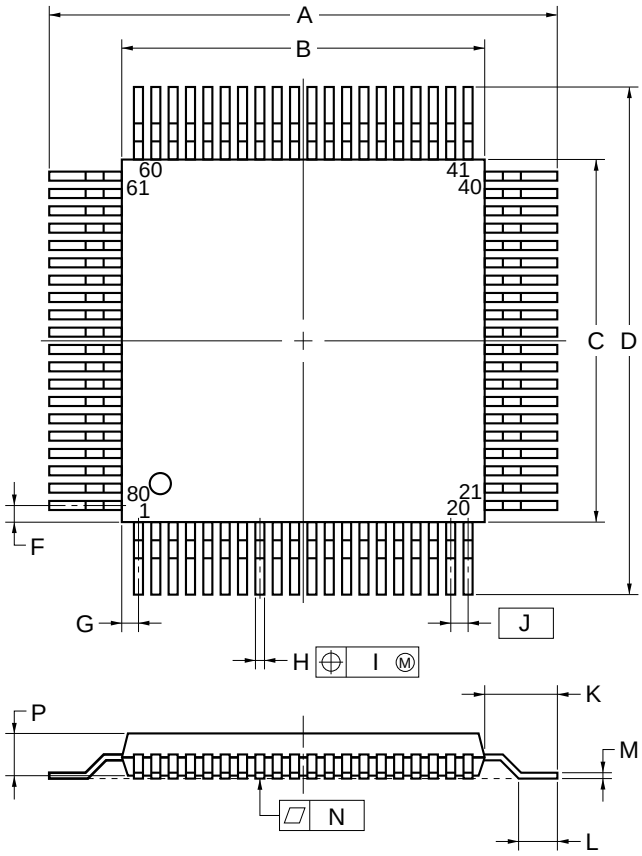


I_{DD} vs. V_{DD} (main system clock: 4.19-MHz crystal resonator)

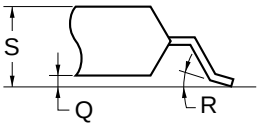


14. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×14)



detail of lead end



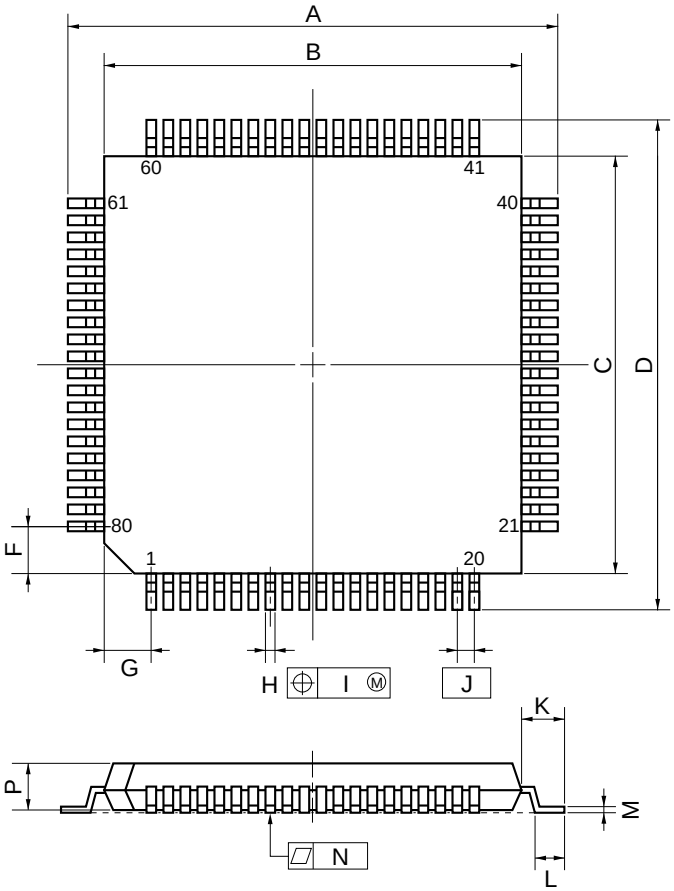
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

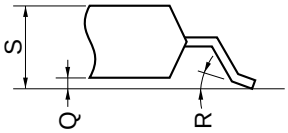
ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-4

80 PIN PLASTIC TQFP (FINE PITCH) (□12)



detail of lead end



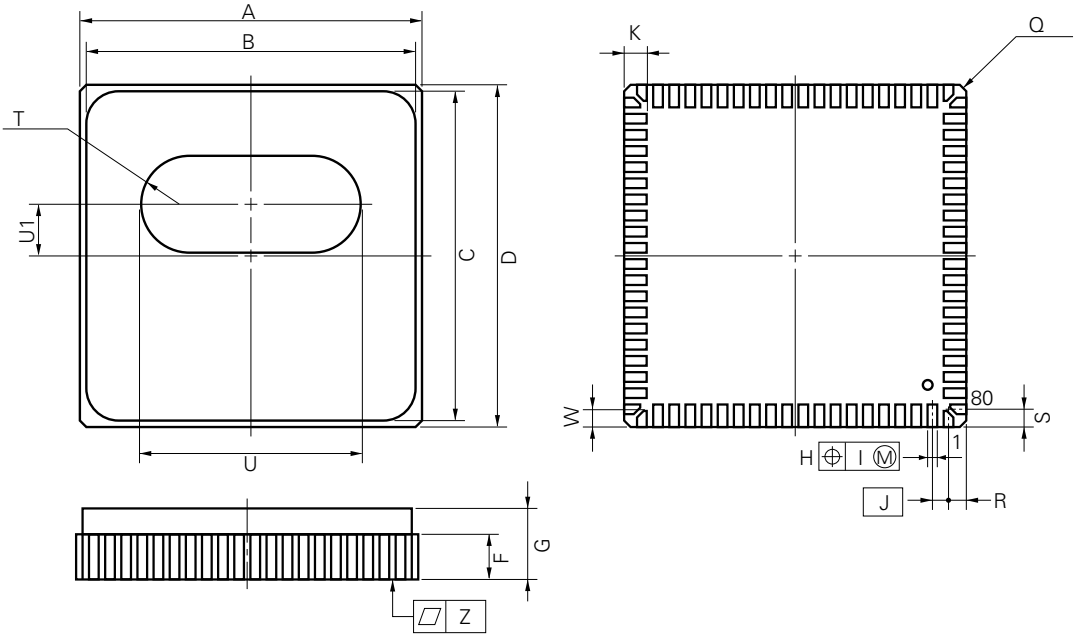
NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	$0.551^{+0.009}_{-0.008}$
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	$0.551^{+0.009}_{-0.008}$
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

* 80 PIN CERAMIC WQFN



X80KW-65A-1

NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	0.551±0.008
B	13.6	0.535
C	13.6	0.535
D	14.0±0.2	0.551±0.008
F	1.84	0.072
G	3.6 MAX.	0.142 MAX.
H	0.45±0.10	$0.018^{+0.004}_{-0.005}$
I	0.06	0.003
J	0.65 (T.P.)	0.024 (T.P.)
K	1.0±0.15	$0.039^{+0.007}_{-0.006}$
Q	C 0.3	C 0.012
R	0.825	0.032
S	0.825	0.032
T	R 2.0	R 0.079
U	9.0	0.354
U1	2.1	0.083
W	0.75±0.15	$0.030^{+0.006}_{-0.007}$
Z	0.10	0.004

★ 15. RECOMMENDED SOLDERING CONDITIONS

Solder the μPD75P3036 under the following recommended conditions.
For the details on the recommended soldering conditions, refer to Information Document **Semiconductor Device Mounting Technology Manual (C10535E)**.
For the soldering methods and conditions other than those recommended, consult NEC.

Table 15-1. Soldering Conditions of Surface Mount Type

(1) μPD75P3036GC-3B9: 80-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235 ˚C, Reflow time: 30 seconds or below (210 ˚C or higher), Number of reflow processes: 3 max.	IR35-00-3
VPS	Package peak temperature: 215 ˚C, Reflow time: 40 seconds or below (200 ˚C or higher), Number of reflow processes: 3 max.	VP15-00-3
Wave soldering	Solder temperature: 260 ˚C or below, Flow time: 10 seconds or below, Number of flow processes: 1 Preheating temperature: 120 ˚C or below (package surface temperature)	WS60-00-1
Pin partial heating	Pin temperature: 300 ˚C or below, Time: 3 seconds or below (per side of device)	—

Caution Do not use two or more soldering methods in combination (except the pin partial heating method).

(2) μPD75P3036GK-BE9: 80-pin plastic TQFP (fine pitch) (12 × 12 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235 ˚C, Reflow time: 30 seconds or below (210 ˚C or higher), Number of reflow processes: 3 max., Exposure limit: 7 days Note (After that, prebaking is necessary at 125 ˚C for 10 hours.)	IR35-107-3
VPS	Package peak temperature: 215 ˚C, Reflow time: 40 seconds or below (200 ˚C or higher), Number of reflow processes: 3 max., Exposure limit: 7 days Note (After that, prebaking is necessary at 125 ˚C for 10 hours.)	VP15-107-3
Wave soldering	Solder temperature: 260 ˚C or below, Flow time: 10 seconds or below, Number of flow processes: 1, Preheating temperature: 120 ˚C or below (package surface temperature) Exposure limit: 7 days Note (After that, prebaking is necessary at 125 ˚C for 10 hours.)	WS60-107-1
Pin partial heating	Pin temperature: 300 ˚C or below, Time: 3 seconds or below (per side of device)	—

Note The number of days for storage after the dry pack has been opened. The storage conditions are 25 ˚C, 65 % RH max.

Caution Do not use two or more soldering methods in combination (except the pin partial heating method).

APPENDIX A. FUNCTION LIST OF μPD75336, 753036, AND 75P3036

		μPD75336	μPD753036	**μPD75P3036**
ROM (bytes)		16256 Mask ROM	16384 Mask ROM	16384 One-time PROM, EPROM
RAM (x 4 bits)		768		
Mk I, Mk II mode selection function		No	Yes	
Instruction set		75X High-End	75XL	
I/O ports	Total	44		
	CMOS input	8		
	CMOS I/O	20 (4 of which can directly drive LEDs)		
	CMOS output	8 (also used as segment pins)		
	N-ch open-drain I/O	8 (can directly drive LEDs, medium-voltage port)		
Mask options		Yes		No
Timers		4 channels: • 8-bit timer/ event counter ..... 2 chs • Basic interval timer ... 1 ch • Watch timer ..... 1 ch	5 channels: • 8-bit timer/event counters ..... 3 chs (16-bit timer/event counter, carrier generator, timer with gate) • Basic interval timer/watchdog timer ..... 1 ch • Watch timer ..... 1 ch	
Vectored interrupt		• External : 3 • Internal : 4	• External : 3 • Internal : 5	
Test input		• External : 1 • Internal : 1	• External : 1 • Internal : 1	
Power supply voltage		V_{DD} = 2.7 to 6.0 V	V_{DD} = 1.8 to 5.5 V	
Instruction execution time	When main system clock is selected	0.95, 1.91, 3.81, or 15.3 μs (@ 4.19 MHz)	• 0.95, 1.91, 3.81, or 15.3 μs (@ 4.19 MHz) • 0.67, 1.33, 2.67, or 10.7 μs (@ 6.0 MHz)	
	When subsystem clock is selected	122 μs (@ 32.768 kHz)		
Package		80-pin plastic QFP (14 x 14 mm) 80-pin plastic TQFP (fine pitch) (12 x 12 mm)		80-pin plastic QFP (14 x 14 mm) 80-pin plastic TQFP (fine pitch) (12 x 12 mm) 80-pin ceramic WQFN

APPENDIX B. DEVELOPMENT TOOLS

The following development tools have been provided for system development using the μPD75P3036. Use the common relocatable assembler for the series together with the device file according to the model.

RA75X relocatable assembler	Host machine			Part No. (name)
		OS	Supply medium	
	PC-9800 Series	MS-DOS™ (Ver.3.30 to Ver.6.2 Note)	3.5-inch 2HD	μS5A13RA75X
			5-inch 2HD	μS5A10RA75X
	IBM PC/AT™ or compatible	Refer to **"OS for IBM PCs"**	3.5-inch 2HC	μS7B13RA75X
			5-inch 2HC	μS7B10RA75X

*

Device file	Host machine			Part No. (name)
		OS	Supply medium	
	PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2 Note)	3.5-inch 2HD	μS5A13DF753036
			5-inch 2HD	μS5A10DF753036
	IBM PC/AT or compatible	Refer to **"OS for IBM PCs"**	3.5-inch 2HC	μS7B13DF753036
			5-inch 2HC	μS7B10DF753036

*

Note Ver. 5.00 or later includes a task swapping function, but this software is not able to use that function.

Remark Operations of the assembler and device file are guaranteed only when using the host machine and OS described above.

PROM Write Tools

Hardware	PG-1500	This is a PROM programmer that can program single-chip microcontroller with PROM in stand alone mode or under control of host machine when connected with supplied accessory board and optional programmer adapter. It can also program typical PROMs in capacities ranging from 256 K to 4 Mbits.			
	PA-75P328GC	This is a PROM programmer adapter for the μPD75P3036GC used by connecting to a PG-1500.			
	PA-75P336GK	This is a PROM programmer adapter for the μPD75P3036GK used by connecting to a PG-1500.			
*	PA-75P3036KK-T[Note 1]	This is a PROM programmer adapter for the μPD75P3036KK-T used by connecting to a PG-1500.			
Software	PG-1500 controller	Connects PG-1500 to host machine with serial and parallel interface and controls PG-1500 on host machine.			
		Host machine			Part No. (name)
			OS	Supply medium	
		PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2[Note 2])	3.5-inch 2HD	μS5A13PG1500
*				5-inch 2HD	μS5A10PG1500
		IBM PC/AT or compatible	Refer to **"OS for IBM PCs"**	3.5-inch 2HD	μS7B13PG1500
				5-inch 2HC	μS7B10PG1500

Notes 1. Under development

2. Ver. 5.00 or later includes a task swapping function, but this software is not able to use that function.

Remark Operation of the PG-1500 controller is guaranteed only when using the host machine and OS described above.

Debugging Tools

In-circuit emulators (IE-75000-R and IE-75001-R) are provided as program debugging tools for the μPD75P3036. Various system configurations using these in-circuit emulators are listed below.

Hardware	IE-75000-R[Note 1]	The IE-75000-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems using the 75X or 75XL Series products. For development of the μPD75P3036, the IE-75000-R is used with optional emulation board (IE-75300-R-EM) and emulation probe (EP-753036GC-R or EP-753036GK-R). Highly efficient debugging can be performed when connected to host machine and PROM programmer. The IE-75000-R includes a connected emulation board (IE-75000-R-EM).
	IE-75001-R	The IE-75001-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems using the 75X or 75XL Series products. The IE-75001-R is used with optional emulation board (IE-75300-R-EM) and emulation probe (EP-753036GC-R or EP-753036GK-R). Highly efficient debugging can be performed when connected to host machine and PROM programmer.
	IE-75300-R-EM[Note 2]	This is an emulation board for evaluating application systems using the μPD75P3036. It is used in combination with the IE-75000-R or IE-75001-R.
	EP-75336GC-R	This is an emulation probe for the μPD75P3036GC. When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM.
	EV-9200GC-80	It includes an 80-pin conversion socket (EV-9200GC-80) to facilitate connections with target system.
	EP-75336GK-R	This is an emulation probe for the μPD75P3036GK. When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM.
	EV-9500GK-80	It includes an 80-pin conversion adapter (EV-9500GK-80) to facilitate connections with target system.
Software	IE control program	This program can control the IE-75000-R or IE-75001-R on a host machine when connected to the IE-75000-R or IE-75001-R via an RS-232-C and Centronics interface.

Host machine			Part No. (name)
	OS	Supply medium	
PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2[Note 3])	3.5-inch 2HD	μS5A13IE75X
		5-inch 2HD	μS5A10IE75X
IBM PC/AT or compatible	Refer to **"OS for IBM PCs"**	3.5-inch 2HC	μS7B13IE75X
		5-inch 2HC	μS7B10IE75X

*

Notes 1. This is a maintenance product.

2. The IE-75300-R-EM is sold separately.

3. Ver. 5.00 or later includes a task swapping function, but this software is not able to use that function.

Remarks 1. Operation of the IE control program is guaranteed only when using the host machine and OS described above.

2. The μPD753036 and 75P3036 are commonly referred to as the μPD753036 Subseries.

OS for IBM PCs

The following operating systems for the IBM PC are supported.

OS	Version
PC DOS™	Ver.5.02 to Ver.6.3 J6.1/V to J6.3/V
MS-DOS	Ver.5.0 to Ver.6.22 5.0/V to 6.2/V
IBM DOS™	J5.02/V

Caution Ver. 5.0 or later includes a task swapping function, but this software is not able to use that function.

* APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Device

Document	Document No.	
	Japanese	English
μPD75P3036 Data Sheet	U11575J	U11575E (this document)
μPD753036 Data Sheet	U11353J	Planned
μPD753036 User's Manual	U10201J	U10201E
μPD753036 Instruction Table	IEM-5063	—
75XL Series Selection Guide	U10453J	U10453E

Documents Related to Development Tools

Document			Document No.	
			Japanese	English
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-846	EEU-1416
	IE-75300-R-EM User's Manual		U11354J	EEU-1493
	EP-75336GC/GK-R User's Manual		U10644J	U10644E
	PG-1500 User's Manual		EEU-651	EEU-1335
Software	RA75X Assembler Package User's Manual	Operation	EEU-731	EEU-1346
		Language	EEU-730	EEU-1363
	PG-1500 Controller User's Manual	PC-9800 Series (MS-DOS) base	EEU-704	EEU-1291
		IBM PC Series (PC DOS) base	EEU-5008	U10540E

Other Related Documents

Document	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Devices	MEI-603	MEI-1202
Microcomputer – Related Product Guide – Third Party Products –	MEI-604	—

Caution The related documents listed above are subject to change without notice. Be sure to use the latest documents for designing, etc.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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