WM8738 EV1M

WM8738 Evaluation Board User Handbook

INTRODUCTION

The WM8738 is a 24-bit Stereo ADC.

This evaluation platform and documentation should be used in conjunction with the latest version of the WM8738 datasheet. The datasheet gives device functionality information as well as timing and data format requirements.

This evaluation platform has been designed to allow the user ease of use and give optimum performance in device measurement.

GETTING STARTED

PACKING LIST

The WM8738 Evaluation Kit Contains:

- 1 WM8738-EV1B Evaluation Board
- This manual -1 WM8738-EV1M

CUSTOMER REQUIREMENTS

Minimum Customer Requires:

- D.C. Power supply of +5V
- D.C. Power supply of +3.0V to +5.5V
- D.C. Power supply of +3.0V to +3.6V
- D.C. Power supply of +12V and -12V

ADC Signal Path Requires (minimum):

- Analogue coaxial jack plug data source
- Digital coaxial data receiving unit
- Master Clock source

POWER SUPPLIES

Using appropriate power leads with 4mm connectors, +5V should be applied to the +5V panel socket J1.

+3.0V to +3.6V should be applied to the DVDD panel socket J3 and +3.0V to +5.5V should be applied to the AVDD panel socket J5.

+12V should be applied to the +12V panel socket J7 and -12V should be applied to the -12V panel socket J10.

DGND should be connected to the DGND panel socket J2 and AGND to the AGND panel socket J6.

The DGND and AGND connections may be connected to a common GND on the supply with no reduction in performance.

Note: Refer to WM8738 datasheet for limitations on individual supply voltages.

BOARD FUNCTIONALITY

There are three options for inputting the required digital clocks to the WM8738 evaluation board. There is a coaxial input (J14) via a standard phono connector or a direct digital input is available via one side of a 2x6 pin header (H1). A further option is to input a MCLK via connector J9 and use the CPLD (U1) to generate BCLK and LRCLK.

The analogue input signals are applied to the evaluation board via phono connectors through either passive or active anti-alias filters. For passive filtering J17 (LIN) and J16 (RIN) can be used and for active filtering J12 (LIN) and J13 (RIN).

There are two options for outputting digital data from the WM8738 evaluation board. There is a coaxial output (J8) via a standard phono connector or the digital signals output from the WM8738 may be accessed via one side of a 2x6 pin header (H2).

All WM8738 device pins are accessible for easy measurement via the 8 pin headers (J11 & J15) running up each side of the device.

BOARD INPUT

Analogue input to the WM8738 is selectable via switches SW5 and SW6. This allows the analogue input to either pass through a passive anti-aliasing filter, using J17 (LIN) and JI6 (RIN), or an active anti-aliasing filter, using J12 (LIN) and J13 (RIN).

Digital clock signals must be supplied to the WM8738. A digital (AES/EBU, UEC958, S/PDIF, EIAJ CP340/1201) signal input may be applied to the coaxial input (J14), allowing the CS8427 (U3) to generate the necessary clocks. A direct digital input is also available via one side of a 2x6 pin header (H1). There is also the facility to generate multi-rate clocks from U1 using SW7 as the rate selection and either the MCLK from the CS8427 (U3) or an independent MCLK input to SMB connector J9.

The digital inputs of the WM8738 are +5V tolerant (independent of supplies), however, a level shift IC (U2) has been included in the audio interface signal path to buffer the input signals when applied via header (H1) and minimise any performance degradation this may cause..

Note: The level shift IC's (U2 and U6) are set to shift from +5V to DVDD when shipped from Wolfson.

BOARD OUTPUT

The output interface from the board is via a coaxial (J8) digital (AES/EBU, UEC958, S/PDIF, EIAJ CP340/1201) signal output. A direct signal output is available via one side of a 2x6 pin header (H2). Data is output in one of the WM8738 supported formats - see datasheet.

A level shift IC (U6) has been included in the audio output interface path to provide signal buffering when output signals are taken from 2x6 pin header H2 will meet external receiver requirements.

INTERFACES

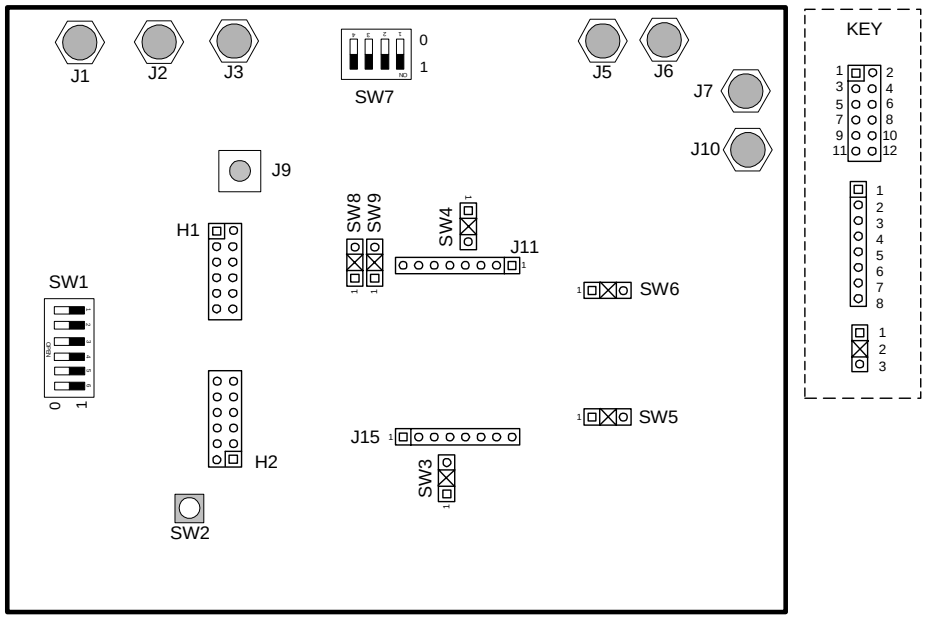

Figure 1 Interfaces

HEADERS

H1	SIGNAL
1/2	MCLK
3/4	GND
5/6	SLAVE_LRC
7/8	GND
9/10	SLAVE_BCLK
11/12	GND

H2	SIGNAL
12/11	GND
10/9	SDOUT
8/7	GND
6/5	BCLK_OUT
4/3	GND
2/1	ADC_LRCLK

J15	WM8738	SIGNAL
1	1	DVDD
2	2	SDOUT
3	3	BCLK
4	4	FMT
5	5	CAP
6	6	VREF
7	7	RIN
8	10	AGND

J11	WM8738	SIGNAL
1	8	LIN
2	9	AVDD
3	10	AGND
4	11	NOHP
5	12	LRCLK
6	13	MCLK
7	14	DGND
8	14	DGND

Table 1 Headers

LINKS

LINKS & JUMPERS	DESCRIPTION
SW3 (FMT)	Pins 1 & 2 SHORT – Left Justified mode Pins 2 & 3 SHORT – I2S mode
SW4 (NOHP)	Pins 1 & 2 SHORT – Digital HPF Disabled Pins 2 & 3 SHORT – Digital HPF Enabled
SW5	Pins 1 & 2 SHORT – Active anti-alias filter input selected Pins 2 & 3 SHORT – RC filter only selected
SW6	Pins 1 & 2 SHORT – Active anti-alias filter input selected Pins 2 & 3 SHORT – RC filter only selected
SW8	Pins 1 & 2 SHORT – Standard CS8427 BCLK selected Pins 2 & 3 SHORT – Multi-rate BCLK selected
SW9	Pins 1 & 2 SHORT – Standard CS8427 LRCLK selected Pins 2 & 3 SHORT – Multi-rate LRCLK selected
J9	External multi-rate MCLK input

Table 2 Links

SWITCHES

SWITCH	DESCRIPTION
SW1 (DATA FORMAT)	6 5 4 3 2 1 DATA FORMAT 0 0 1 0 0 1 I2S Compatible 0 0 0 0 0 1 Left Justified
SW2	The CS8427 may be RESET by pressing and releasing switch SW2. This is required if the switches on SW1 are changed after the board is powered up.
SW7 (MCLK RATE)	4 3 2 1 MCLK RATE 1 0 0 0 256fs 0 1 0 0 384fs 0 0 1 0 512fs 0 0 0 1 768fs

Table 3 Switches

WM8738 OPERATION

STANDARD CONTROL & USING MULTI-RATE MCLK

The WM8738 is a hardware control only device and must be dealt with as a slave (i.e. all clocks must be supplied to the WM8738 from another source).

There are only 2 pins that can be used to change the setup of the WM8738, these are pin 4 (FMT) and pin 11 (NOHP). 3 pin link switch SW3 is used to control the FMT pin, putting this switch high (short pins 1 & 2) will set the output data format from the WM8738 to Left Justified mode while putting the switch low (short pins 2 & 3) will set the output data format to I2S mode. 3 pin link switch SW4 is used to control the NOHP pin, putting this switch high (short pins 1 & 2) will disable the internal digital High Pass Filter while putting the switch low (short pins 2 & 3) will enable the internal digital High Pass Filter.

Figure **2** shows the basic 'getting started' setup required to operate the board. In this example the data format is set to I2S with the digital HPF set active.

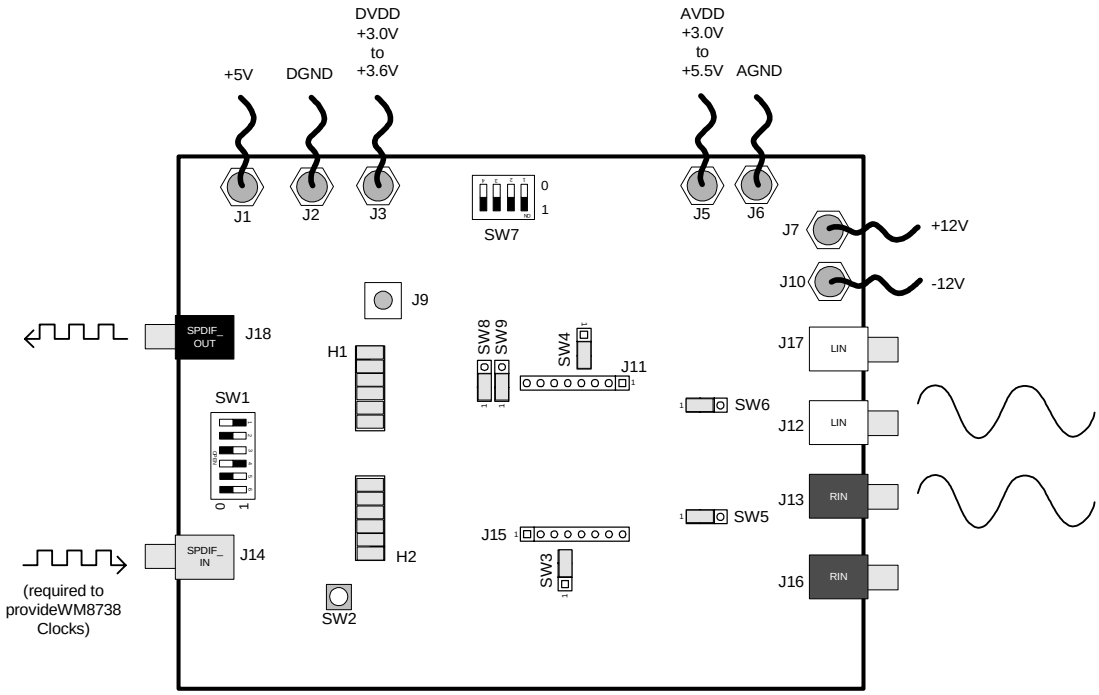

Figure 2 Basic Setup Example

LINKS & JUMPERS	DESCRIPTION
H1	All Links ON
H2	All Links ON
SW3 (FMT)	Pins 2 & 3 SHORT – I2S mode
SW4 (NOHP)	Pins 2 & 3 SHORT – Digital HPF Enabled
SW5	Pins 1 & 2 SHORT – Active anti-alias filter input selected
SW6	Pins 1 & 2 SHORT – Active anti-alias filter input selected
SW8	Pins 1 & 2 SHORT – Standard CS8427 BCLK selected
SW9	Pins 1 & 2 SHORT – Standard CS8427 LRCLK selected

Table 4 Basic Setup Example Settings

An additional feature that has been provided on the WM8738 evaluation board is the ability to run with multi-rate MCLK's. This is achieved through the use of the CPLD (U1) and the relevant switch setting of SW7. Four MCLK rates are supported, 256fs, 384fs, 512fs and 768fs. To operate the evaluation board in this mode, 3 pin jumper switches SW8 and SW9 should be set so that pins 2 and 3 are shorted, an external MCLK should be supplied through the SMB connector J9, the MCLK is then passed through the CPLD which divides it down to generate the equivalent LRCLK and BCLK frequencies.

Figure 3 shows the setup required if using an external MCLK. In this example the data format is set to I2S digital HPF is active and the MCLK is running at 512fs.

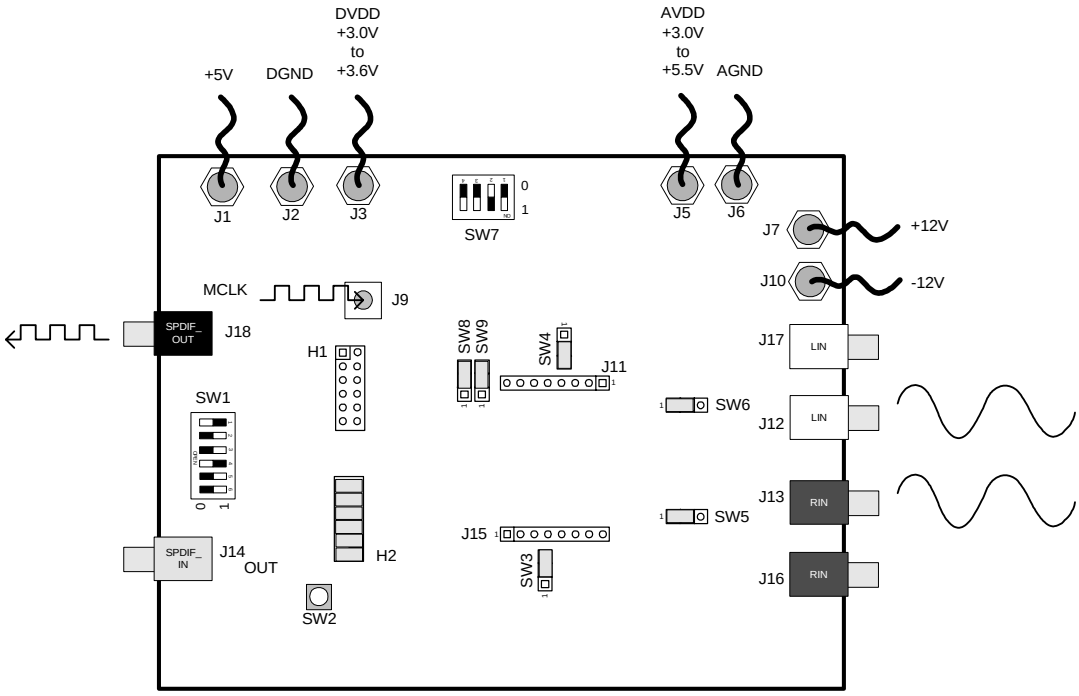

Figure 3 Using an External MCLK Example

LINKS & JUMPERS	DESCRIPTION
H1	All Links OFF
H2	All Links ON
SW3 (FMT)	Pins 2 & 3 SHORT – I2S mode
SW4 (NOHP)	Pins 2 & 3 SHORT – Digital HPF Enabled
SW5	Pins 1 & 2 SHORT – Active anti-alias filter input selected
SW6	Pins 1 & 2 SHORT – Active anti-alias filter input selected
SW8	Pins 2 & 3 SHORT – Multi-rate BCLK selected
SW9	Pins 2 & 3 SHORT – Multi-rate LRCLK selected
J9	External multi-rate MCLK input

Table 5 Using an External MCLK Example Settings

WM8738-EV1B SCHEMATIC

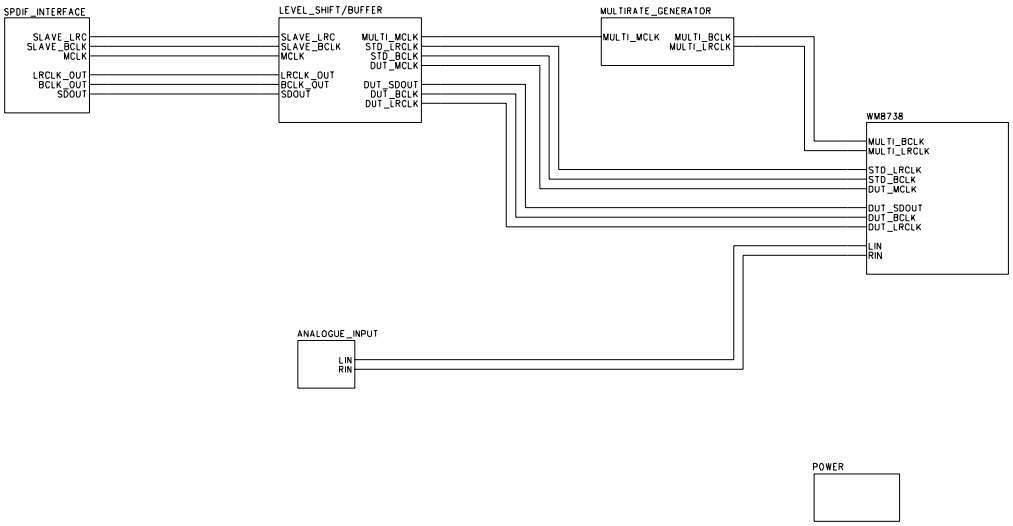

Figure 4 Functional Diagram

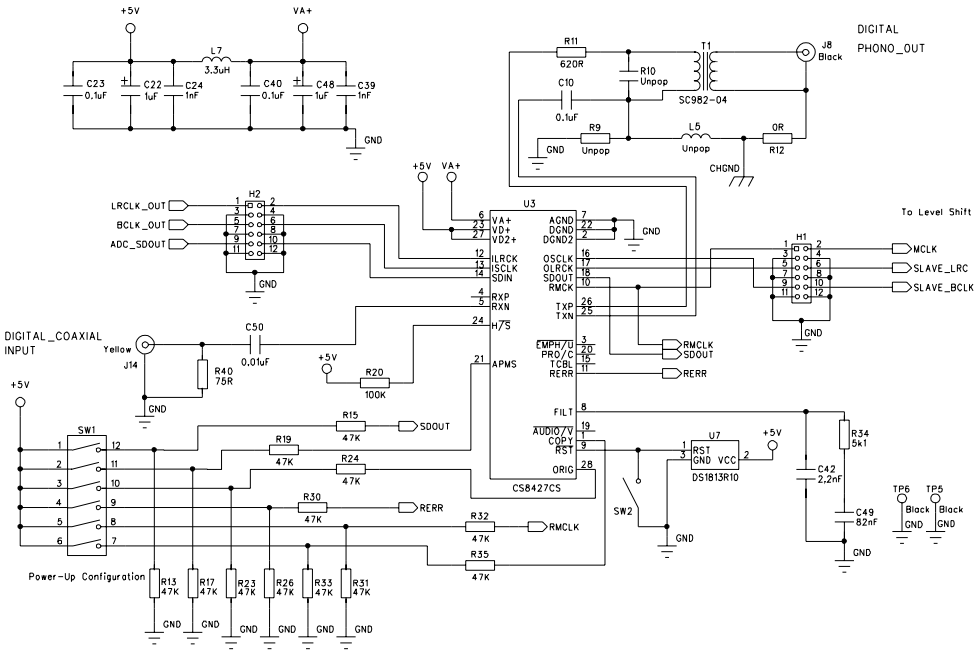

Figure 5 Digital Interface

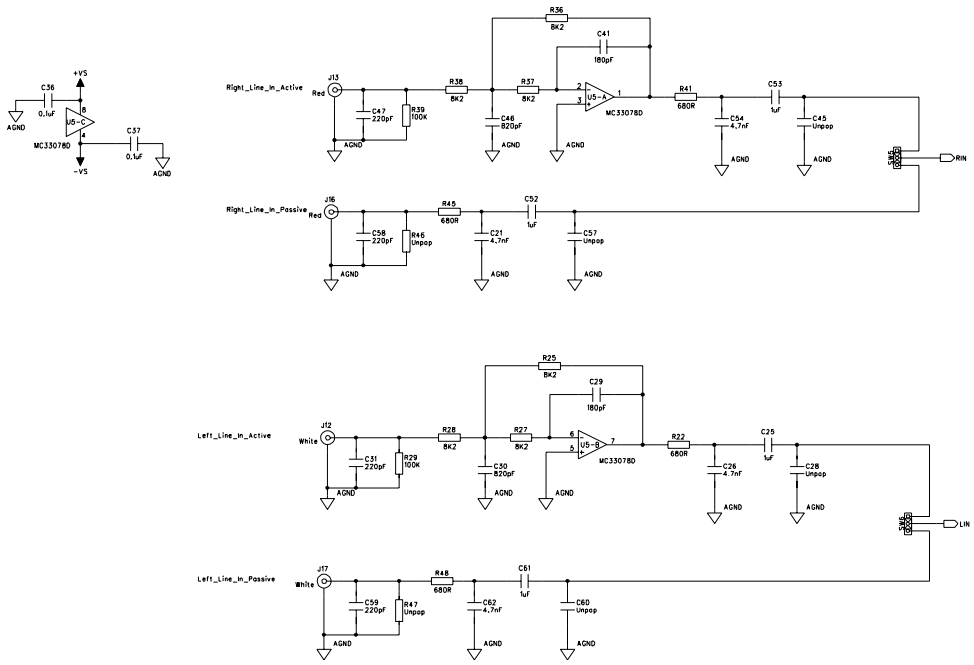

Figure 6 Analogue Input

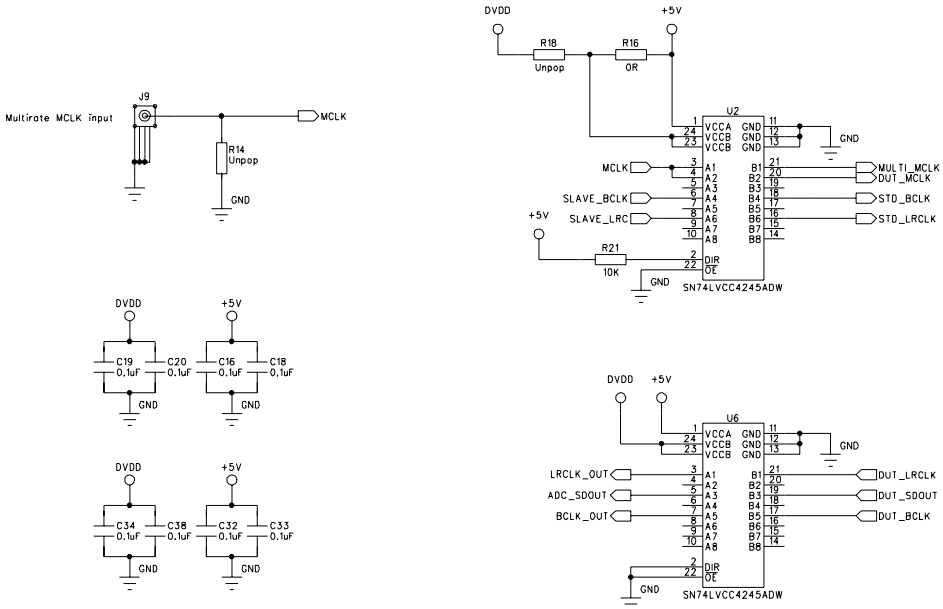

Figure 7 Level Shift / Buffer

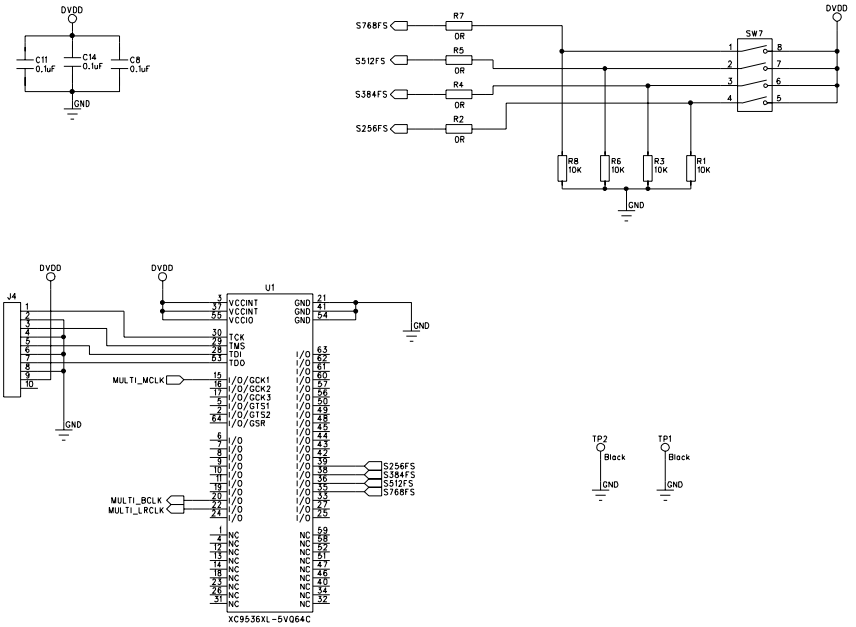

Figure 8 Multi-Rate Generator

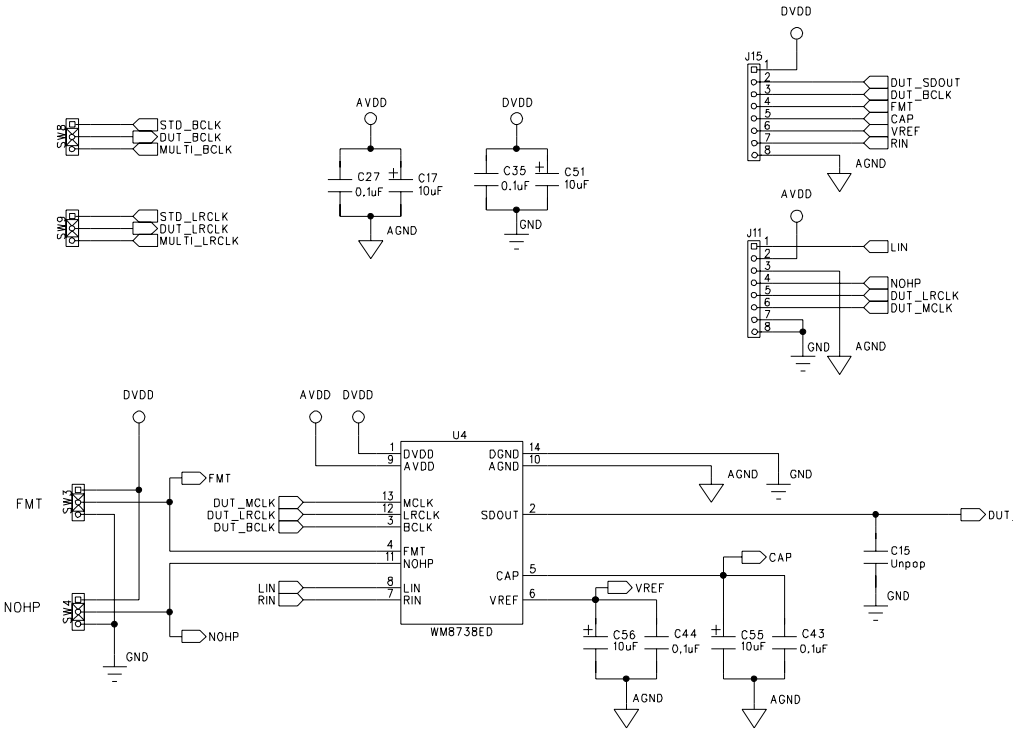

Figure 9 WM8738

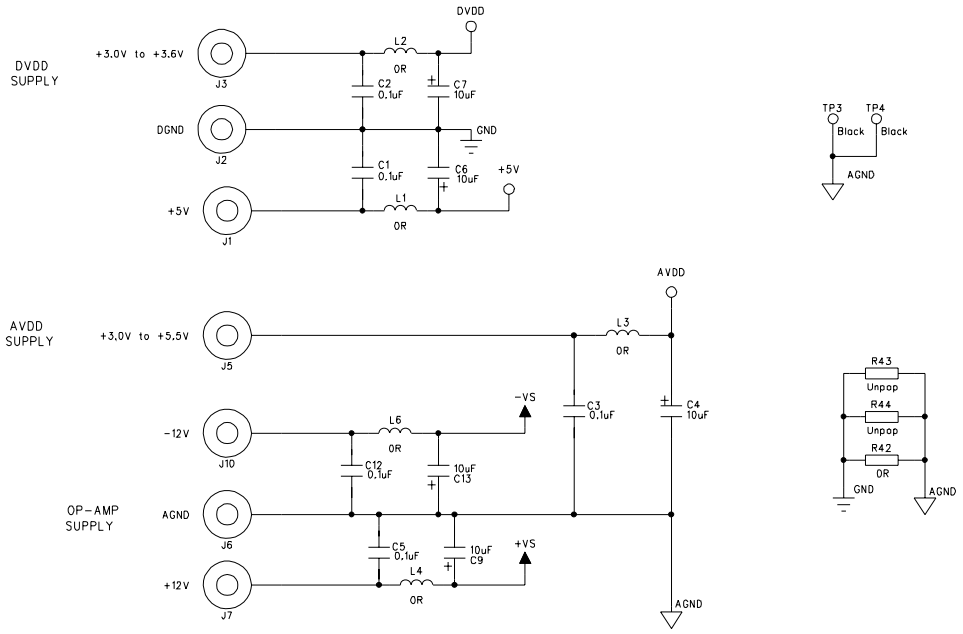

Figure 10 Power

WM8738-EV1B PCB LAYOUT

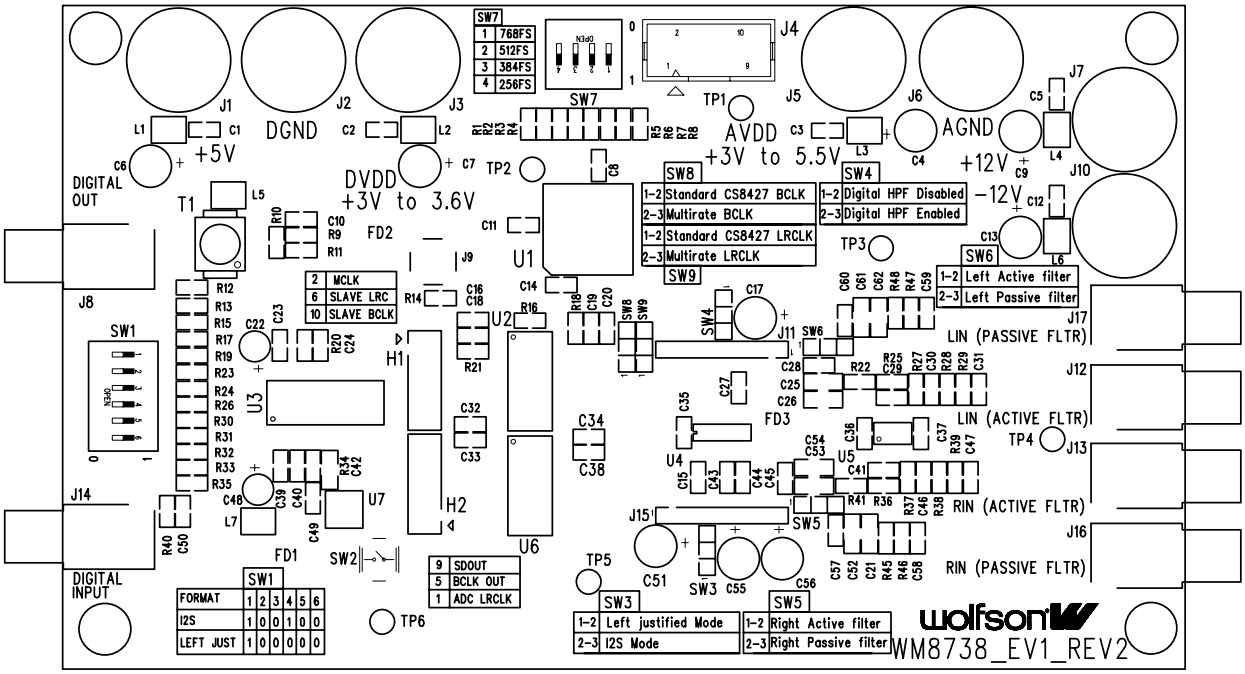

Figure 11 Top Layer Silkscreen

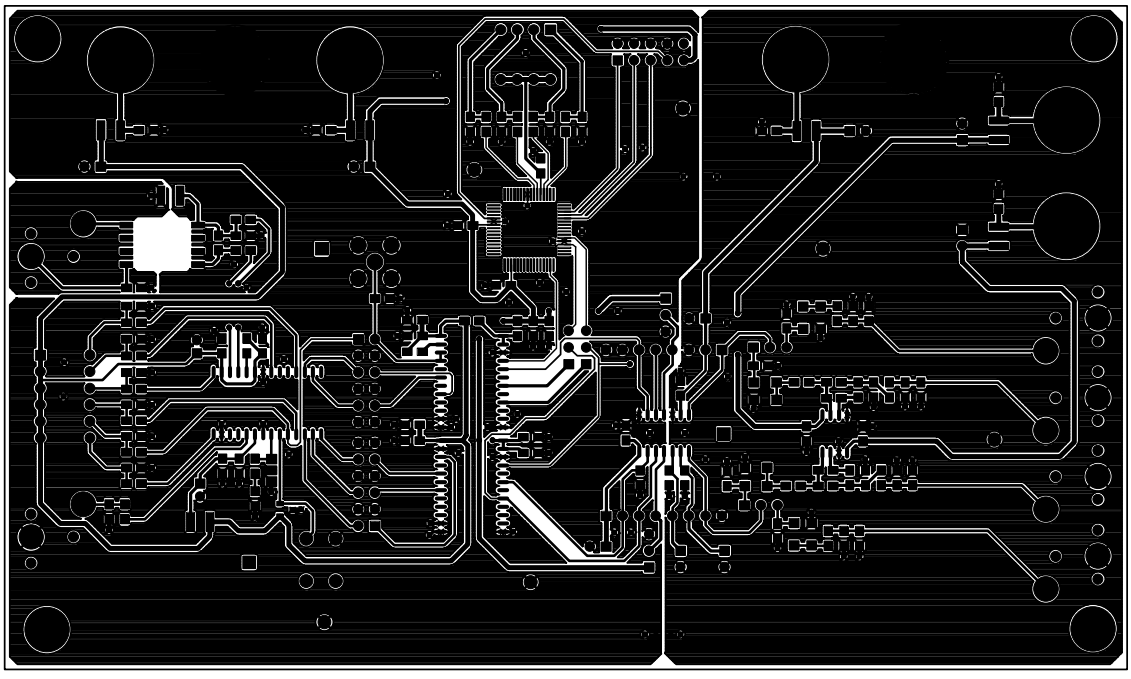

Figure 12 Top Layer

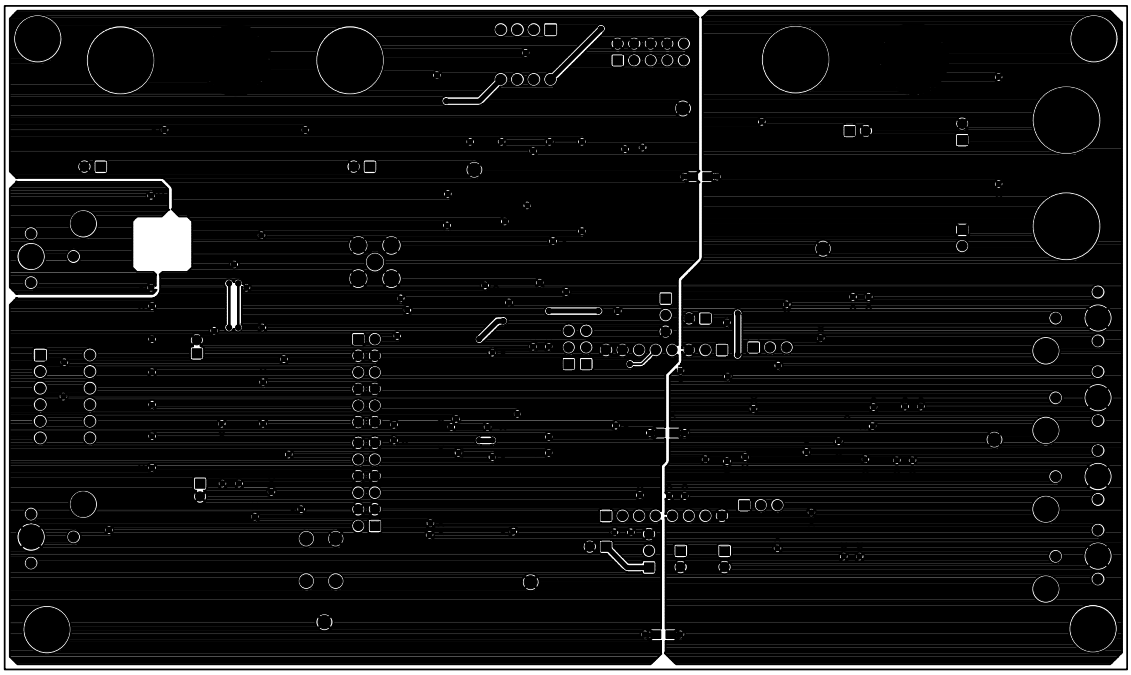

Figure 13 Bottom Layer

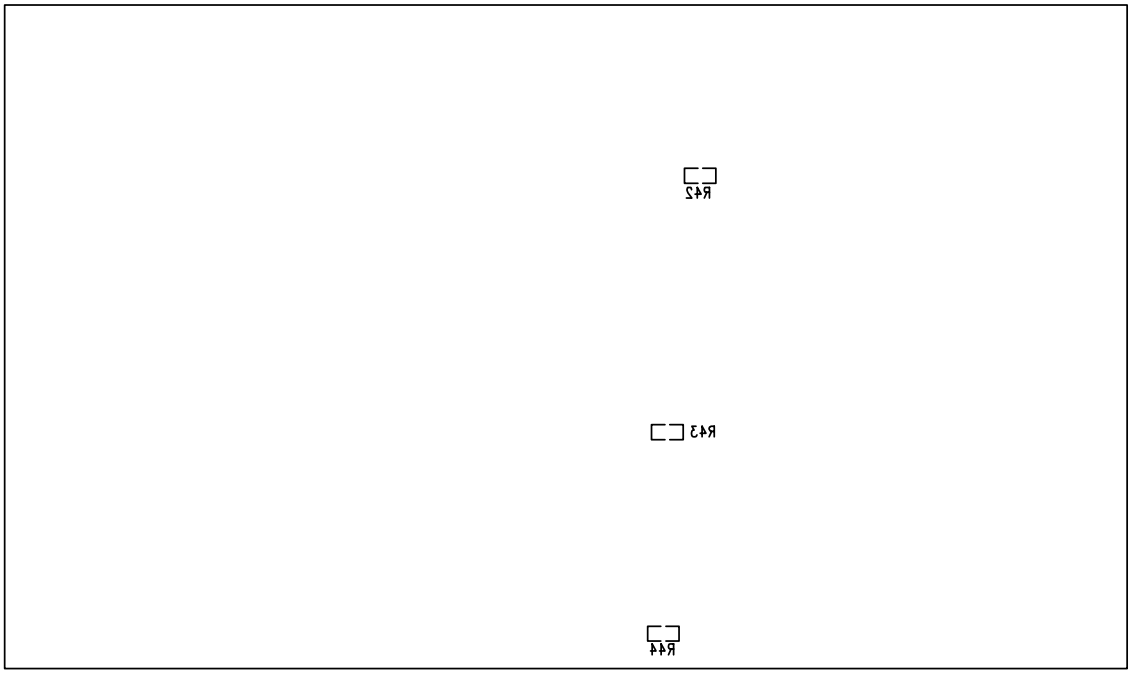

Figure 14 Bottom Layer Silkscreen

WM8738-EV1B BILL OF MATERIAL

Description	REF-DES	QTY
10uF 6.3 Dia 2.5 pitch Oscon Through Hole Cap. 16V 20%	C4 C6-7 C9 C13 C17 C51 C55-56	9
1uF 4 Dia 2 pitch Oscon Through Hole Cap. 25V 20%	C22 C48	2
0.01uF 0805 SMD Ceramic Capacitor 50V X7R	C50	1
0.1uF 0805 SMD Ceramic Capacitor 50V X7R	C1-3 C5 C8 C10-12 C14 C16 C18-20 C23 C27 C32-38 C40 C43-44	25
180pF 0805 SMD Ceramic Capacitor 50V NPO	C29 C41	2
1nF 0805 SMD Ceramic Capacitor 50V NPO	C24 C39	2
220pF 0805 SMD Ceramic Capacitor 50V X7R	C31 C47 C58 C59	4
820pF 0805 SMD Ceramic Capacitor 50V NPO	C30 C46	2
82nF 0805 SMD Ceramic Capacitor 25V X7R	C49	1
1uF 1206 SMD Ceramic Capacitor 16V X7R	C25 C52 C53 C61	4
2.2nF 1206 SMD Ceramic Capacitor 50V NPO	C42	1
4.7nF 1206 SMD Ceramic Capacitor 50V COG	C21 C26 C54 C62	4
2x5 2.54mm Male PCB Header LoPro VERTICAL	J4	1
1x8 2.54mm pitch PCB Pin Header VERTICAL	J11 J15	2
2x6 2.54mm pitch PCB Pin Header VERTICAL	H1-2	2
JSK9-16-G0 PCB 1x3 Jumper Switch 0.1" Center-off VERTICAL	SW3-6 SW8-9	6
4mm Non-Insulated Panel Socket 16A	J1-3 J5-7 J10	7
Phono Socket PCB mount BLACK	J8	1
Phono Socket PCB mount RED	J13 J16	2
Phono Socket PCB mount WHITE	J12 J17	2
Phono Socket PCB mount YELLOW	J14	1
SMB Connector PCB Mount 50 Ohm VERTICAL	J9	1
CD8427 96KHz Audio Transceiver	U3	1
DS1813 5V active Low Power-On-Reset chip SOT	U7	1
0R 1206 Resistor on 1210 Inductor site	L1-4 L6	5
3.3uH 1210 Surface Mount Inductor '1210A series'	L7	1
MC33078 Low Noise Dual Op-Amp SO	U5	1
0R 0805 SMD chip resistor 1% 0.1W	R2 R4 R5 R7 R12 R16 R42	7
100K 0805 SMD chip resistor 1% 0.1W	R20 R29 R39	3
10K 0805 SMD chip resistor 1% 0.1W	R1 R3 R6 R8 R21	5
47K 0805 SMD chip resistor 1% 0.1W	R13 R15 R17 R19 R23-24 R26 R30-33 R35	12
5k1 0805 SMD chip resistor 1% 0.125W	R34	1
620R 0805 SMD chip resistor 1% 0.1W	R11	1
680R 0805 SMD chip resistor 1% 0.1W	R22 R41 R45 R48	4
75R 0805 SMD chip resistor 1% 0.125W	R40	1
8K2 0805 SMD chip resistor 1% 0.1W	R25 R27-28 R36-38	6
SN74LVCC4245A Octal Dual Supply(5V, 3-5V) Transceiver SO	U2 U6	2
DIL Switch 4-Way Rocker	SW7	1
DIL Switch 6-Way Rocker	SW1	1
B3F1000 SPNO PCB mount switch	SW2	1
1.32mm PCB Test Terminal BLACK	TP1-6	6
2:1 Ratio 96KHz SPDIF Digital Audio transformer SOIC	T1	1
WM8738 Stereo ADC	U4	1
XC9536XL-15 3.3V 36 macrocell CPLD	U1	1

Note: [1] The audio transformer (T1) used on this board is manufactured by Scientific Conversion Inc. (www.scientificonversion.com).

EVALUATION SUPPORT

The aim of this evaluation kit is to help you to become familiar with the functionality and performance of the WM8738, stereo audio ADC.

If you require more information or require technical support please contact Wolfson Microelectronics Applications group through the following channels:

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Fax: (+44) 131 272 7001
Mail: Applications at the address on the last page.

or contact your local Wolfson representative.

Additional information may be made available from time to time on our web site at:

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