

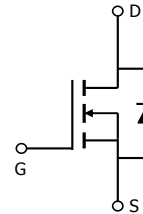
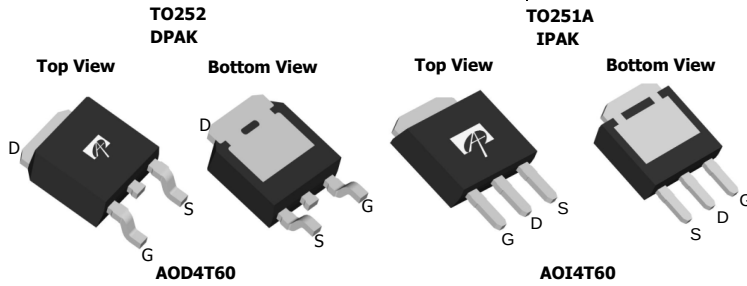
General Description

The AOD4T60 & AOI4T60 are fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low $R_{DS(on)}$, C_{iss} and C_{rss} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

Product Summary

$V_{DS} @ T_{j,max}$	700V
I_{DM}	16A
$R_{DS(ON),max}$	< 2.1 Ω
$Q_{g,typ}$	9nC
$E_{oss} @ 400V$	1.6 μ J

100% UIS Tested!
100% R_g Tested!



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ^B	I_D	4	A
		2.5	
	$T_C=25^\circ\text{C}$		
	$T_C=100^\circ\text{C}$		
Pulsed Drain Current ^C	I_{DM}	16	
Avalanche Current ^{C,K}	I_{AR}	4	A
Repetitive avalanche energy ^{C,K}	E_{AR}	8	mJ
Single pulsed avalanche energy ^H	E_{AS}	145	mJ
MOSFET dv/dt ruggedness	dv/dt	50	V/ns
Peak diode recovery dv/dt		5	
Power Dissipation ^B	P_D	83	W
		0.7	W/ $^\circ\text{C}$
	$T_C=25^\circ\text{C}$		
	Derate above 25°C		
Junction and Storage Temperature Range	T_J, T_{STG}	-50 to 150	$^\circ\text{C}$
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient ^{A,G}	$R_{\theta JA}$	40	50	$^\circ\text{C/W}$
Maximum Case-to-sink ^A	$R_{\theta CS}$	-	0.5	$^\circ\text{C/W}$
Maximum Junction-to-Case ^{D,F}	$R_{\theta JC}$	1.25	1.5	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	600			V
		I _D =250μA, V _{GS} =0V, T _J =150°C		700		
BV _{DSS} /ΔT _J	Zero Gate Voltage Drain Current	I _D =250μA, V _{GS} =0V		0.6		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =600V, V _{GS} =0V			1	μA
		V _{DS} =480V, T _J =125°C			10	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	3	4.2	5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =1A		1.75	2.1	Ω
g _{FS}	Forward Transconductance	V _{DS} =40V, I _D =2A		2.8		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.79	1	V
I _S	Maximum Body-Diode Continuous Current				4	A
I _{SM}	Maximum Body-Diode Pulsed Current ^C				16	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		460		pF
C _{oss}	Output Capacitance			22		pF
C _{o(er)}	Effective output capacitance, energy related ^I	V _{GS} =0V, V _{DS} =0 to 480V, f=1MHz		19		pF
C _{o(tr)}	Effective output capacitance, time related ^J			31		pF
C _{rss}	Reverse Transfer Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		3.5		pF
R _g	Gate resistance	f=1MHz		5.7		Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =480V, I _D =4A		9	15	nC
Q _{gs}	Gate Source Charge			3.5		nC
Q _{gd}	Gate Drain Charge			2.4		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =300V, I _D =4A, R _G =25Ω		20		ns
t _r	Turn-On Rise Time			27		ns
t _{D(off)}	Turn-Off DelayTime			25		ns
t _f	Turn-Off Fall Time			17		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =4A, dI/dt=100A/μs, V _{DS} =100V		384		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =4A, dI/dt=100A/μs, V _{DS} =100V		3.9		μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25°C.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C in a TO252 package, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C.

G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

H. L=60mH, I_{AS}=2.2A, V_{DD}=150V, R_G=10Ω, Starting T_J=25°C.

I. C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

J. C_{o(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

K. L=1.0mH, V_{DD}=150V, R_G=25Ω, Starting T_J=25°C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

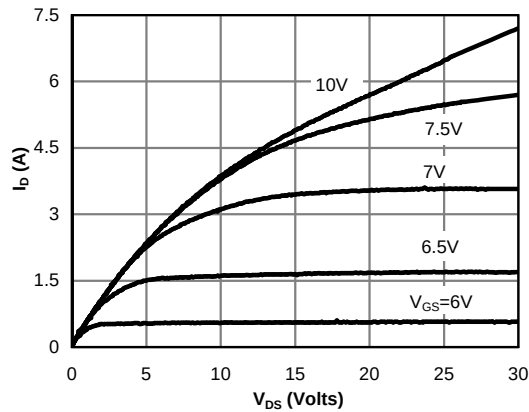


Fig 1: On-Region Characteristics

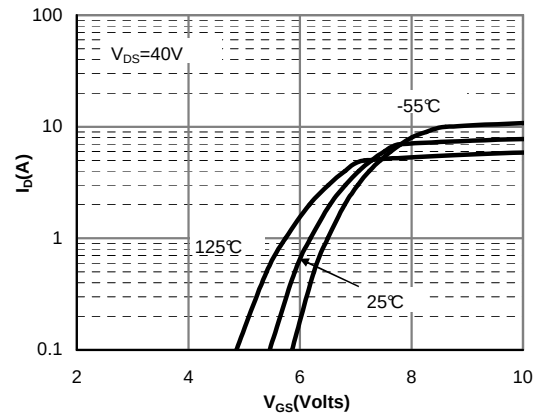


Figure 2: Transfer Characteristics

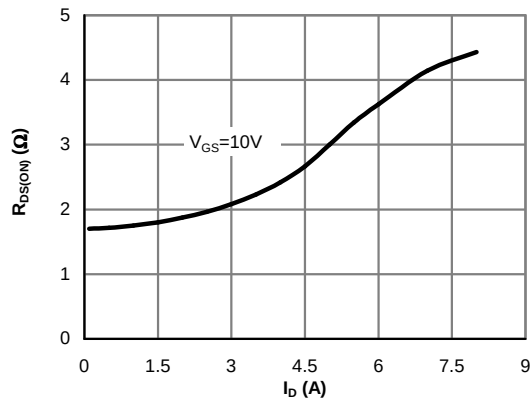


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

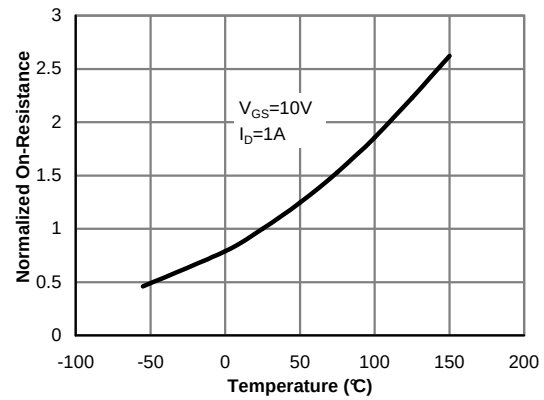


Figure 4: On-Resistance vs. Junction Temperature

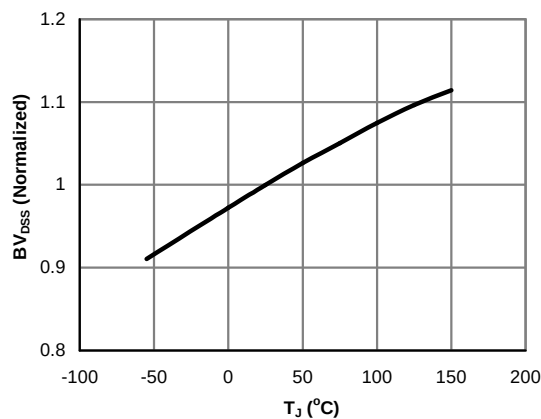


Figure 5: Break Down vs. Junction Temperature

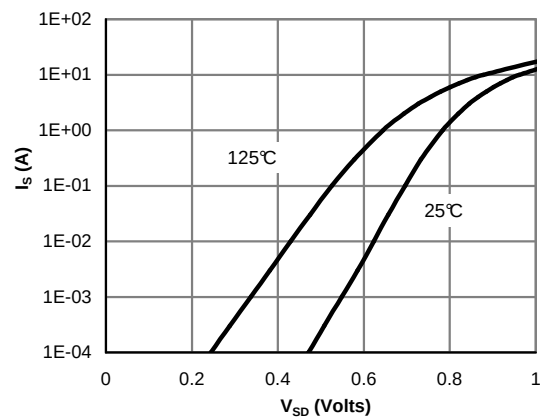


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

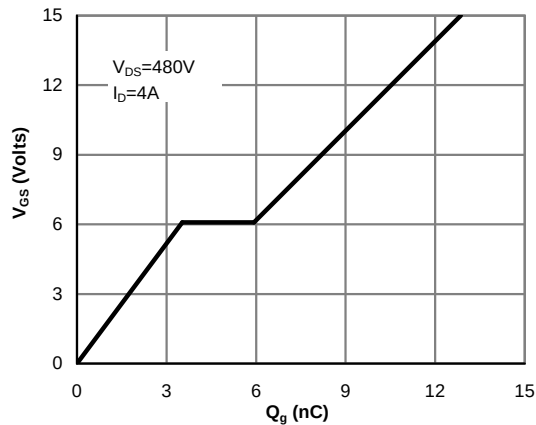


Figure 7: Gate-Charge Characteristics

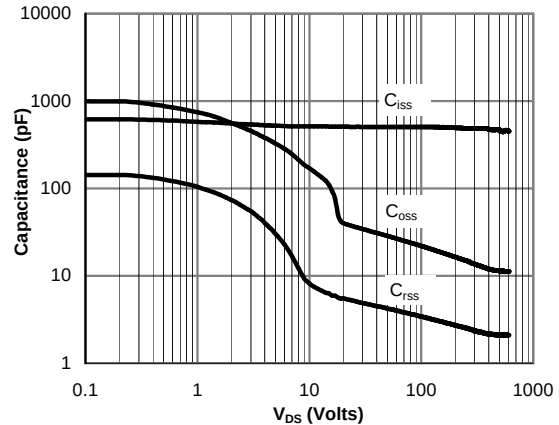


Figure 8: Capacitance Characteristics

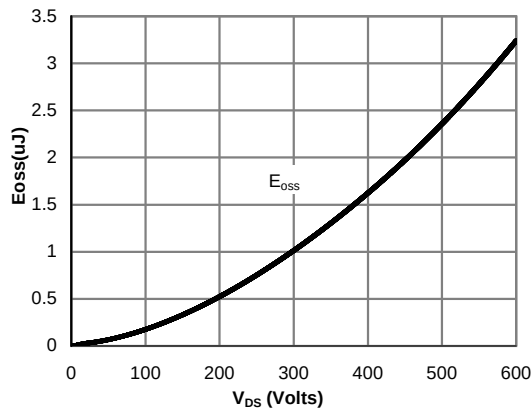


Figure 9: Coss stored Energy

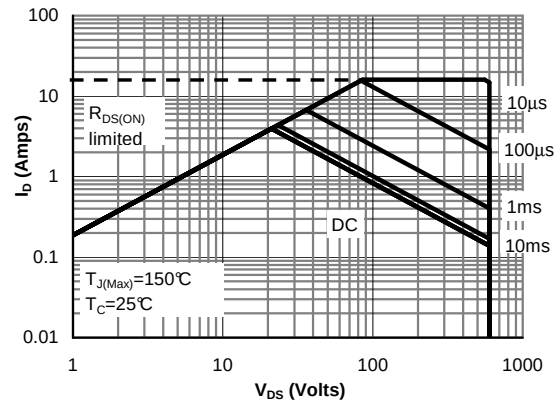


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

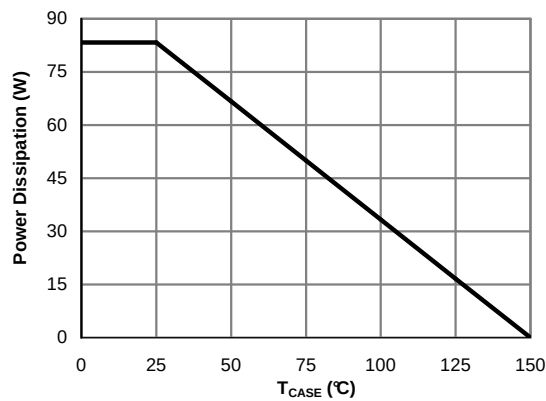


Figure 11: Power De-rating (Note B)

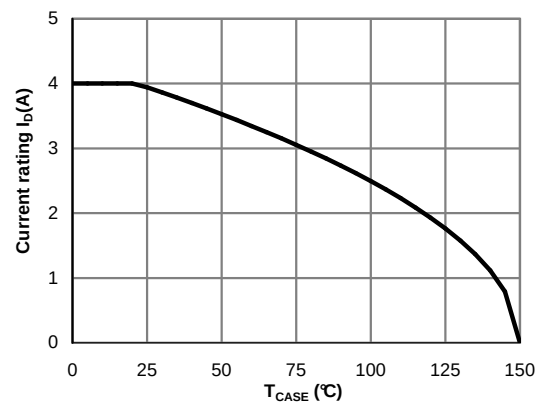


Figure 12: Current De-rating (Note B)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

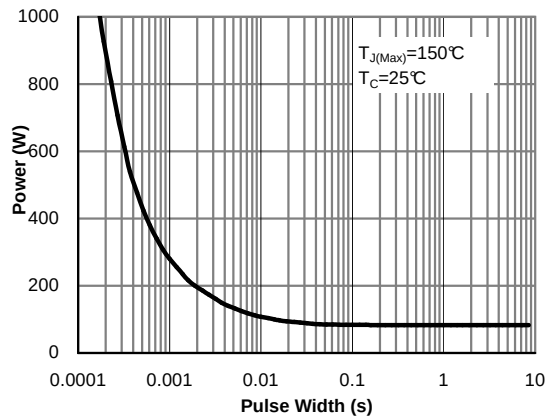


Figure 13: Single Pulse Power Rating Junction-to-Case (Note F)

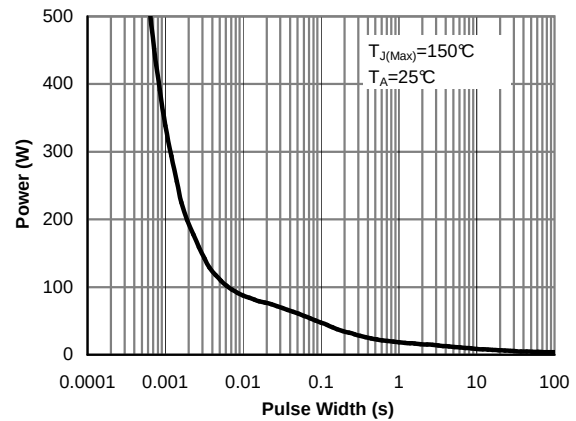


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

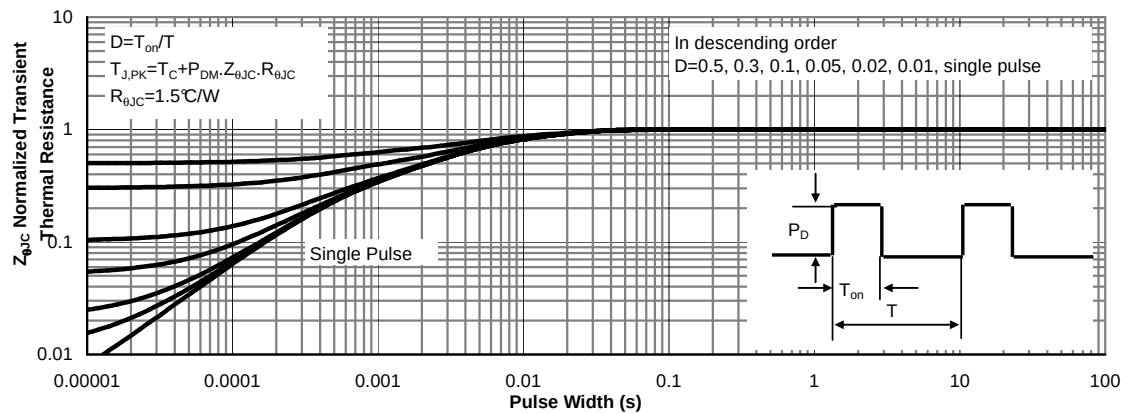


Figure 15: Normalized Maximum Transient Thermal Impedance (Note F)

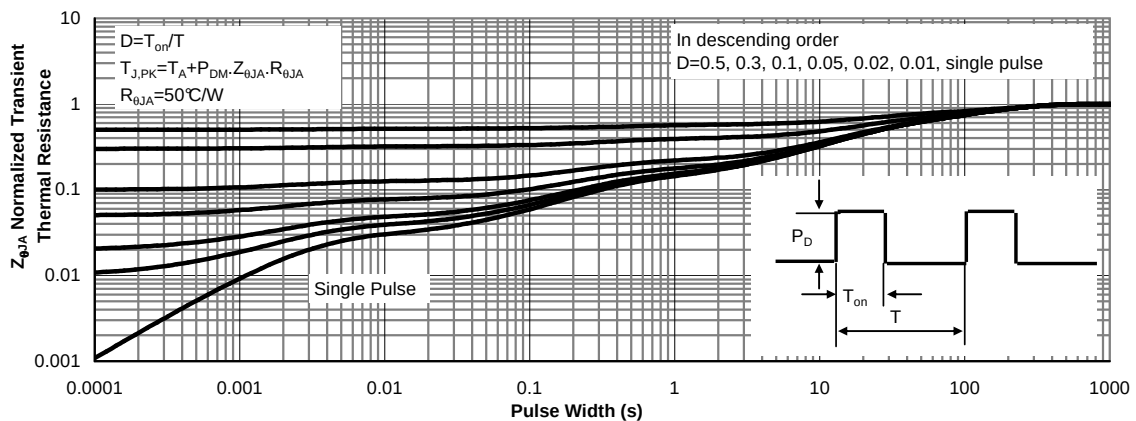
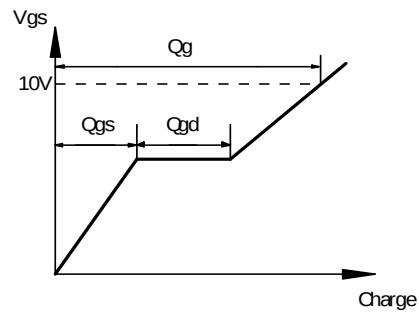
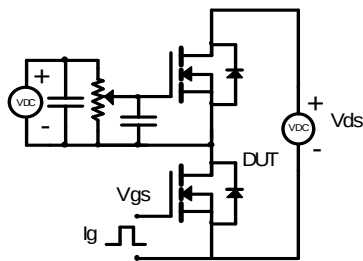
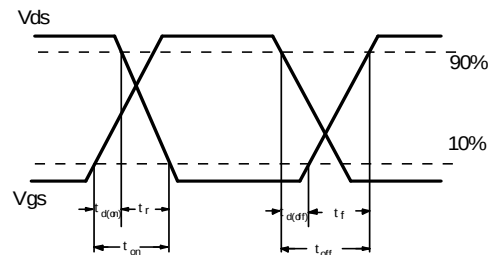
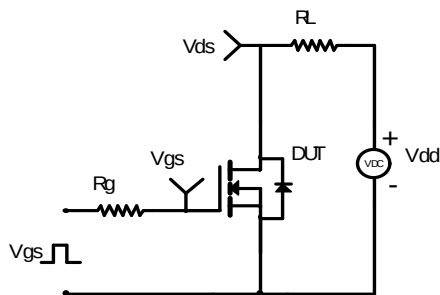


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

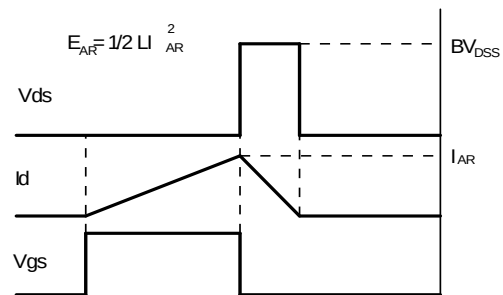
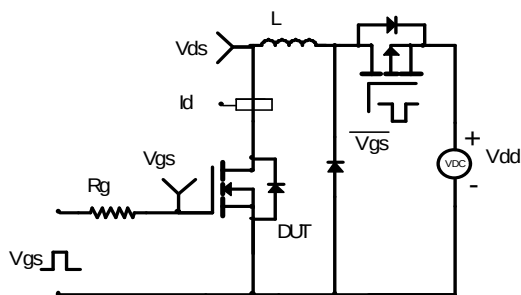
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

