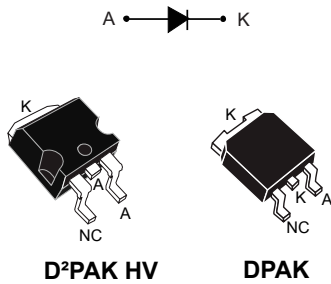


Automotive 650 V, 8 A high surge silicon carbide power Schottky diode

Features



- AEC-Q101 qualified 
- No reverse recovery charge in application current range
- Switching behavior independent of temperature
- Recommended to PFC applications
- PPAP capable
- V_{RRM} guaranteed from -40 to 175 °C
- D²PAK HV creepage distance (anode to cathode) = 5.38 mm min. (with top coating)
- ECOPACK2 compliant component

Applications

- On board battery charger (OBC)

Description

The SiC diode is an ultrahigh performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature.

Especially suited for use in PFC applications, the SiC diode will boost performance in hard switching conditions.

Product label



Product status

STPSC8H065-Y

Product summary

Symbol	Value
$I_{F(AV)}$	8 A
V_{RRM}	650 V
$T_{J(max.)}$	175 °C

1 Characteristics

Table 1. Absolute ratings (limiting values at 25 °C unless otherwise specified)

Symbol	Parameter		Value	Unit
V _{RRM}	Repetitive peak reverse voltage	T _j = -40 °C to + 175 °C	650	V
I _{F(RMS)}	Forward rms current		22	A
I _{F(AV)}	Average forward current	T _c = 145 °C ⁽¹⁾ , DC	8	A
I _{FSM}	Surge non repetitive forward current	t _p = 10 ms sinusoidal, T _c = 25 °C	75	A
		t _p = 10 ms sinusoidal, T _c = 125 °C	69	
		t _p = 10 μs square, T _c = 25 °C	420	
I _{FRM}	Repetitive peak forward current	T _c = 145 °C ⁽¹⁾ , T _j = 175 °C, δ = 0.1	33	A
T _{stg}	Storage temperature range		-55 to +175	°C
T _j	Operating junction temperature range		-40 to +175	°C

1. Value based on R_{th(j-c)} max.

Table 2. Thermal resistance parameters

Symbol	Parameter	Typ. value	Max. value	Unit
R _{th(j-c)}	Junction to case	1.3	1.6	°C/W

Table 3. Static electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I _R ⁽¹⁾	Reverse leakage current	T _j = 25 °C	V _R = V _{RRM}	-	7	80	μA
		T _j = 150 °C		-	65	335	
V _F ⁽²⁾	Forward voltage drop	T _j = 25 °C	I _F = 8 A	-	1.45	1.65	V
		T _j = 150 °C		-	1.7	2.05	

1. t_p = 10 ms, δ < 2%

2. t_p = 500 μs, δ < 2%

To evaluate the conduction losses, use the following equation:

$$P = 0.972 \times I_{F(AV)} + 0.135 \times I_{F(RMS)}^2$$

Table 4. Dynamic electrical characteristics

Symbol	Parameter	Test conditions	Typ.	Unit
Q _{cj} ⁽¹⁾	Total capacitive charge	V _R = 400 V	23.5	nC
C _j	Total capacitance	V _R = 0 V, T _c = 25 °C, F = 1 MHz	414	pF
		V _R = 400 V, T _c = 25 °C, F = 1 MHz	38	

1. Most accurate value for the capacitive charge: $Q_{cj}(V_R) = \int_0^{V_R} C_j(V) dV$

1.1 Characteristics (curves)

Figure 1. Forward voltage drop versus forward current (typical values, low level)

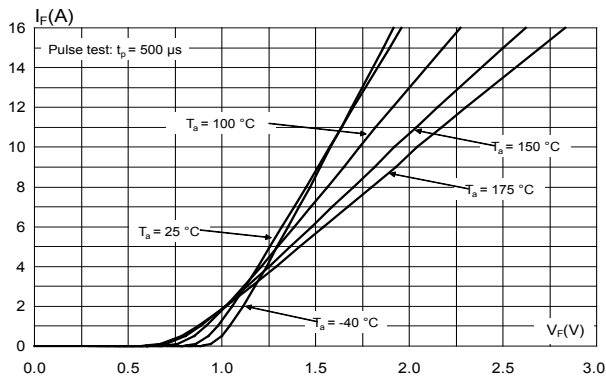


Figure 2. Forward voltage drop versus forward current (typical values, high level)

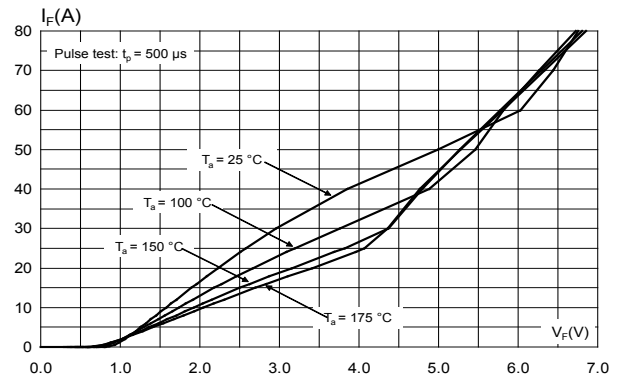


Figure 3. Reverse leakage current versus reverse voltage applied (typical values)

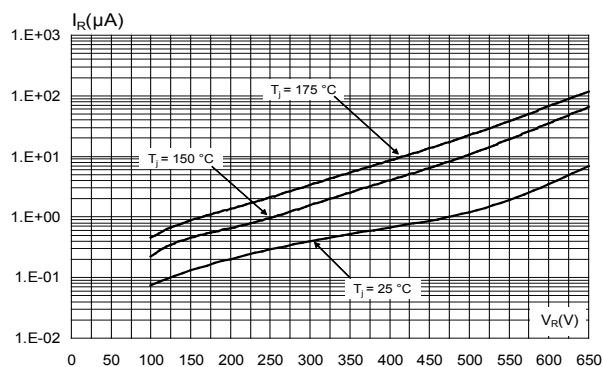


Figure 4. Peak forward current versus case temperature

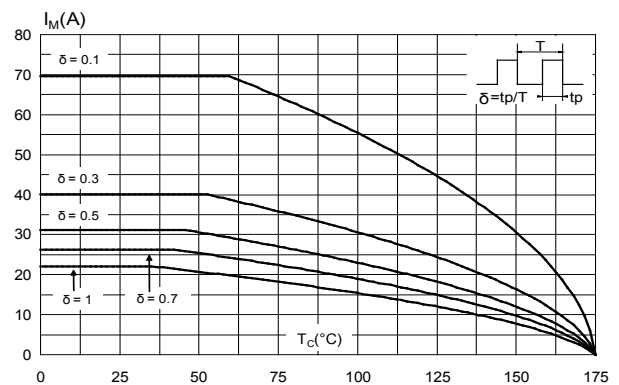


Figure 5. Junction capacitance versus reverse voltage applied (typical values)

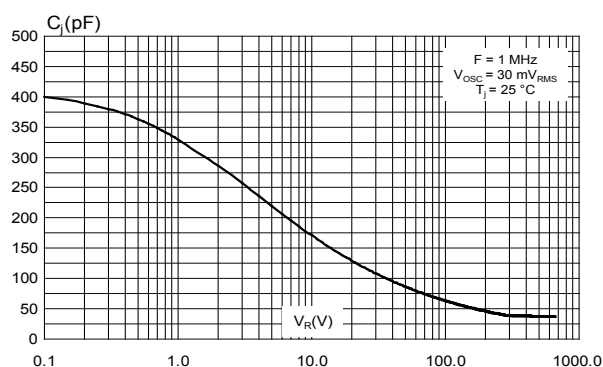


Figure 6. Relative variation of thermal impedance junction to case versus pulse duration

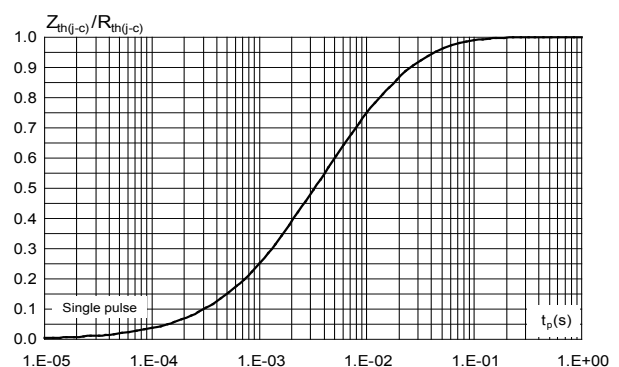


Figure 7. Non-repetitive peak surge forward current versus pulse duration (sinusoidal waveform)

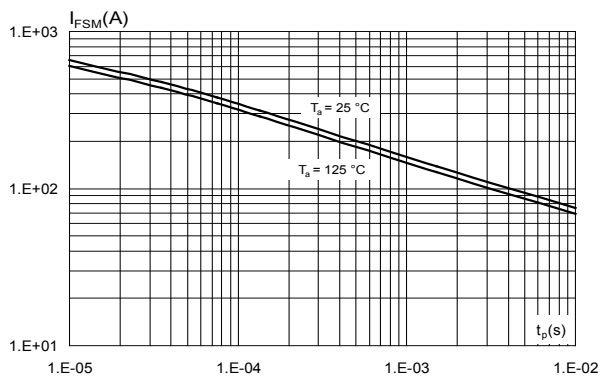


Figure 8. Total capacitive charges versus reverse voltage applied (typical values)

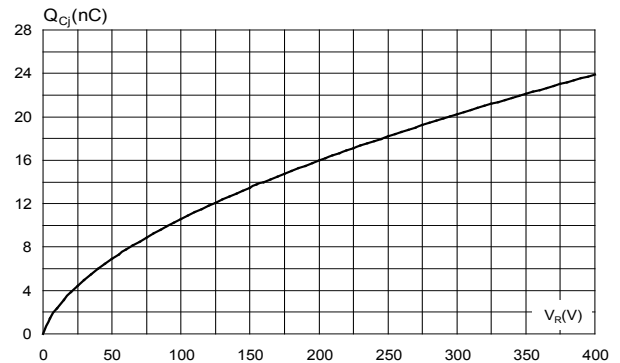
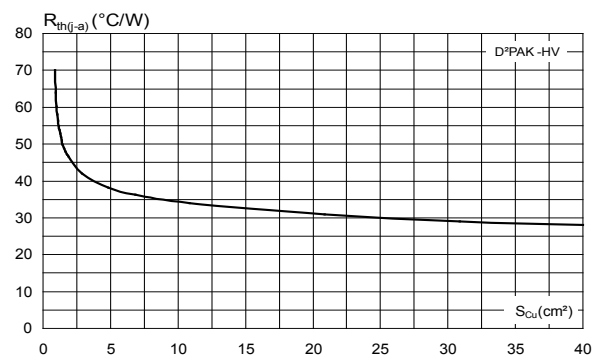


Figure 9. Thermal resistance junction to ambient versus copper surface under tab (typical values, epoxy printed board FR4, $e_{Cu} = 35\text{ }\mu\text{m}$) (D²PAK-HV)



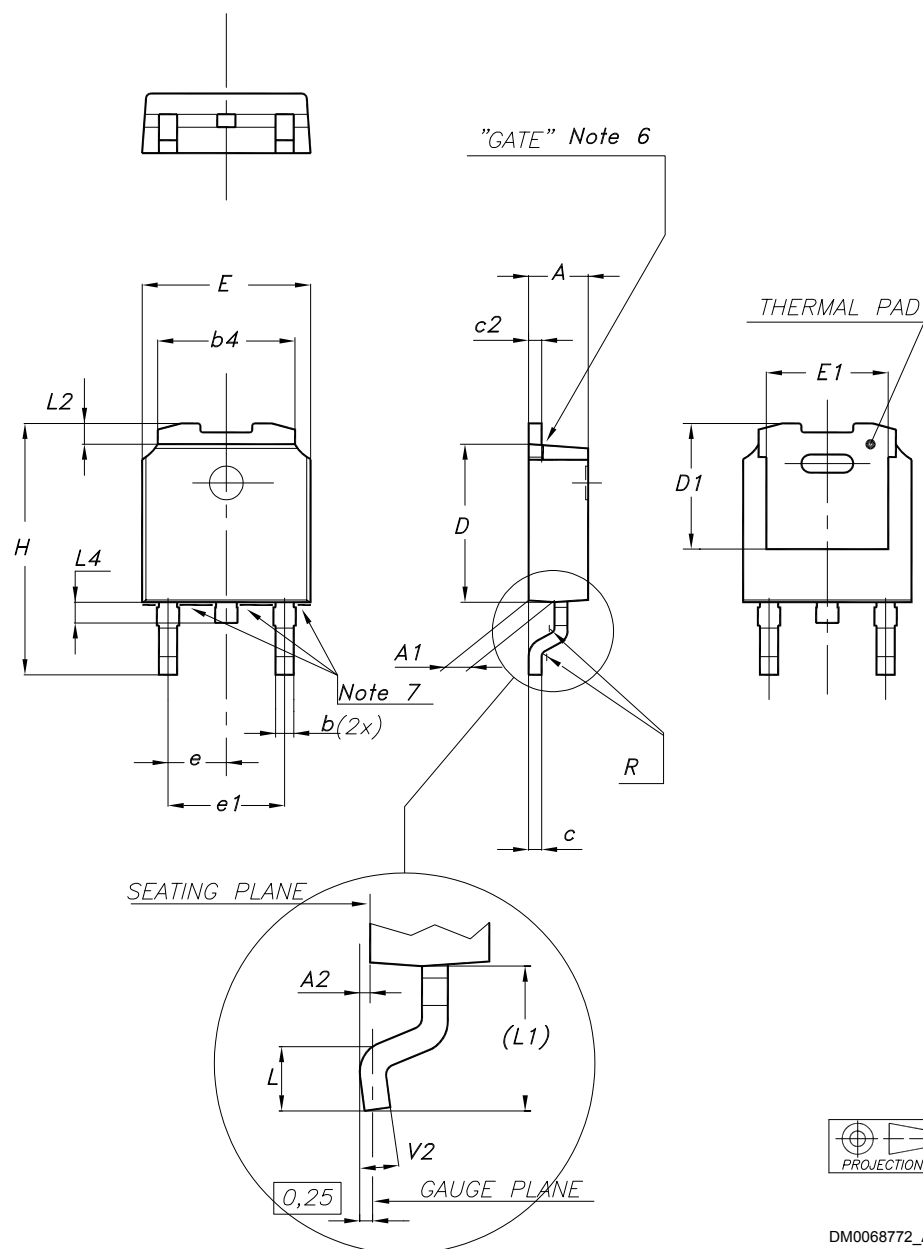
2 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 DPAK package information

- Epoxy meets UL94, V0

Figure 10. DPAK package outline



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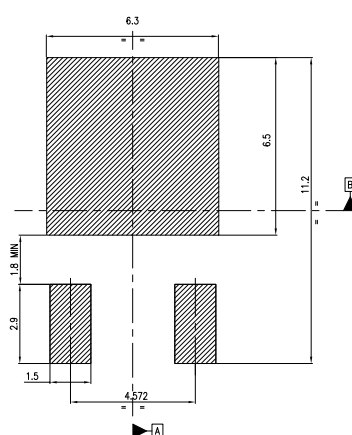
Note: This package drawing may slightly differ from the physical package. However, all the specified dimensions are guaranteed.

Table 5. DPAK mechanical data

Dim.	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
b	0.64		0.90	0.025		0.035
b4	5.20		5.40	0.205		0.213
c	0.45		0.60	0.018		0.024
c2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
D1	4.95	5.10	5.25	0.195	0.201	0.207
E	6.40		6.60	0.252		0.260
E1	4.60	4.70	4.80	0.181	0.185	0.189
e	2.159	2.286	2.413	0.085	0.090	0.095
e1	4.445	4.572	4.699	0.175	0.180	0.185
H	9.35		10.10	0.368		0.398
L	1.00		1.50	0.039		0.059
(L1)	2.60	2.80	3.00	0.102	0.110	0.118
L2	0.65	0.80	0.95	0.026	0.031	0.037
L4	0.60		1.00	0.024		0.039
R		0.20			0.008	
V2	0°		8°	0°		8°

1. Inches dimensions given for reference only

Figure 11. DPAK recommended footprint (dimensions are in mm)



Notes:

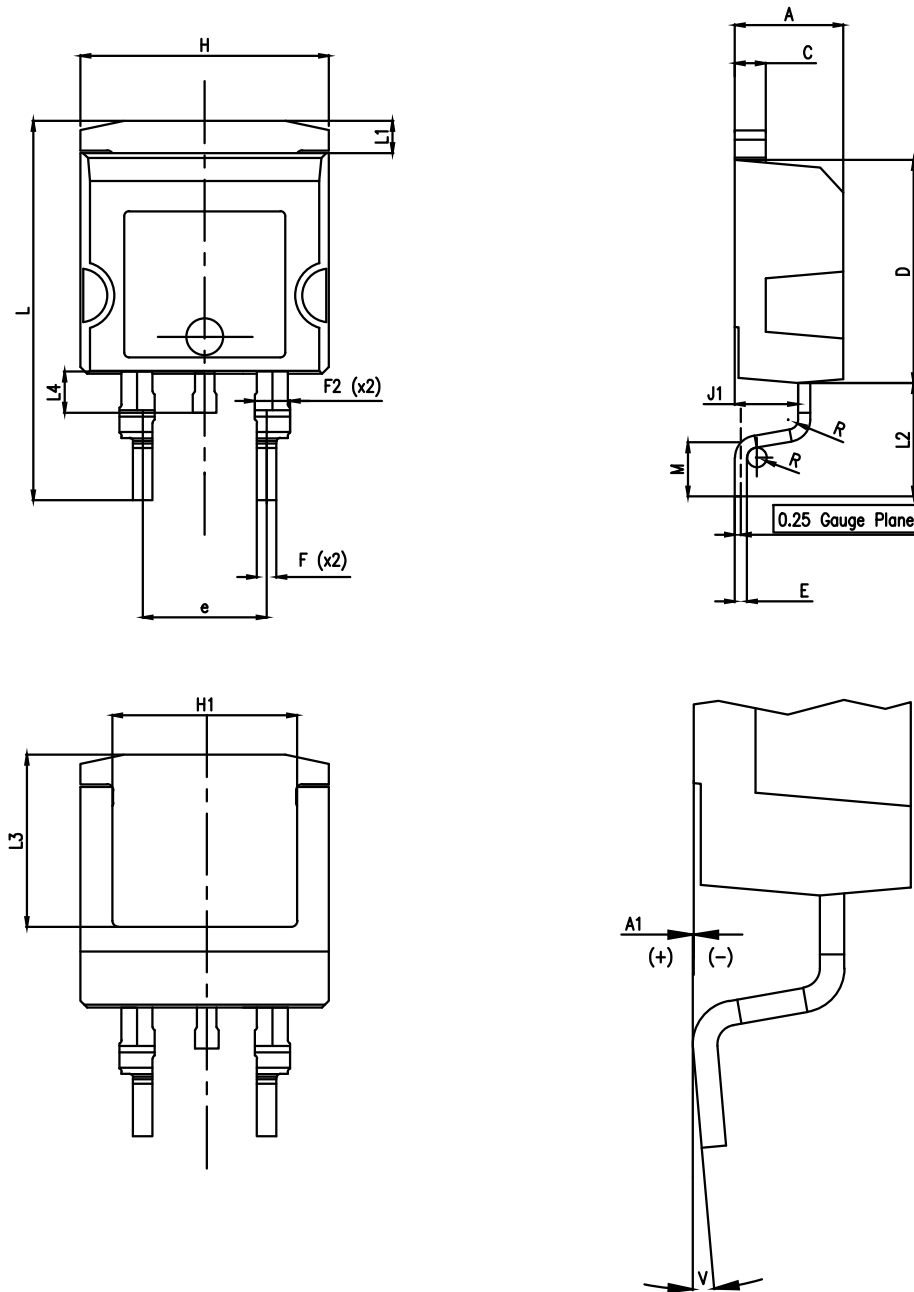
- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within $\Phi 0.05$ A B

EP 0068772 B

Note: For package and tape orientation, reel and inner box dimensions and tape outline see [TN1173](#).

2.2 D²PAK HV package information

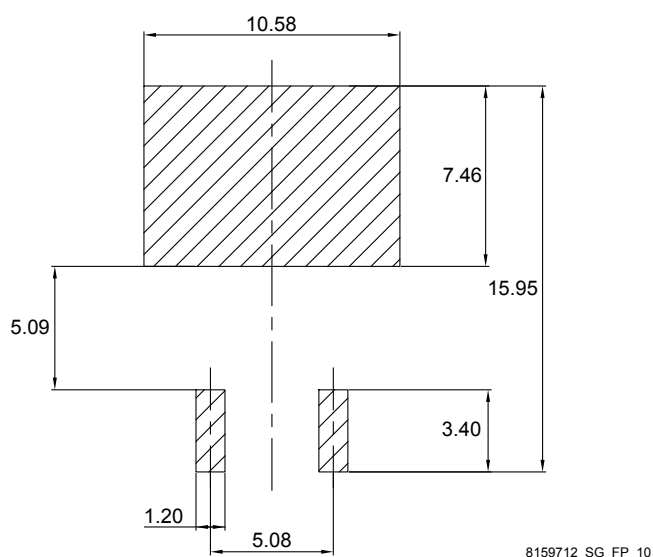
Figure 12. D²PAK high voltage package outline



8159712_SG_10

Table 6. D²PAK high voltage package mechanical data

Ref.	Dimensions		
	Min.	Typ.	Max.
A	4.30	-	4.70
A1	-0.05	-	0.08
C	1.17	-	1.37
D	8.95	-	9.35
e	4.98	-	5.18
E	0.50	-	0.90
F	0.78	-	0.85
F2	1.14	-	1.70
H	10.00	-	10.40
H1	7.40	-	7.80
J1	2.49	-	2.69
L	15.30	-	15.80
L1	1.27	-	1.40
L2	4.93	-	5.23
L3	6.85	-	7.25
L4	1.5	-	1.7
M	2.6	-	2.9
R	0.20	-	0.60
V	0°	-	8°

Figure 13. D²PAK high voltage footprint in mm


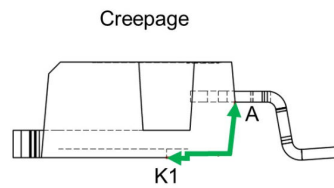
2.2.1 Creepage distance between anode and cathode

Table 7. Creepage distance between anode and cathode

Symbol	Parameter		Value	Unit
Cd _{A-K1}	Minimum creepage distance between A and K1 (with top coating)	D ² PAK HV	5.38	mm
Cd _{A-K2}	Minimum creepage distance between A and K2 (without top coating)		3.48	

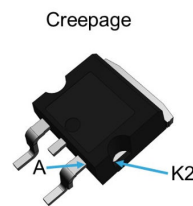
Note: D²PAK HV creepage distance (anode to cathode) = 5.38 mm min. (refer to IEC 60664-1)

Figure 14. Creepage with top coating



Minimum distance between A & K1 = 5.38 mm (with top coating)

Figure 15. Creepage without top coating



Minimum distance between A & K2 = 3.48 mm (without top coating)

3 Ordering Information

Table 8. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
STPSC8H065BY-TR	PSC8H 065Y	DPAK	0.32 g	2500	Tape and reel
STPSC8H065G2Y-TR	PSC8H065G2Y	D ² PAK HV	1.48 g	1000	Tape and reel

Revision history

Table 9. Document revision history

Date	Version	Changes
08-Mar-2018	1	Initial release.
11-Sep-2018	2	Added D ² PAK HV package.
06-Dec-2018	3	Updated Section 2.2.1 : Creepage distance between anode and cathode. Minor text changes to improve readability. Updated title of document.
08-Oct-2025	4	Updated Section Features , Table 6 , and Table 8 .

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