SM802128

ClockWorks™ 10GbE Octal 156.25MHz, 312.5MHz, Ultra-Low Jitter, LVPECL Frequency Synthesizer

General Description

The SM802128 is a member of the ClockWorks™ family of devices from Micrel and provides an extremely low-noise timing solution for 10GbE Ethernet clock signals. It is based upon a unique patented RotaryWave® architecture that provides very low phase noise.

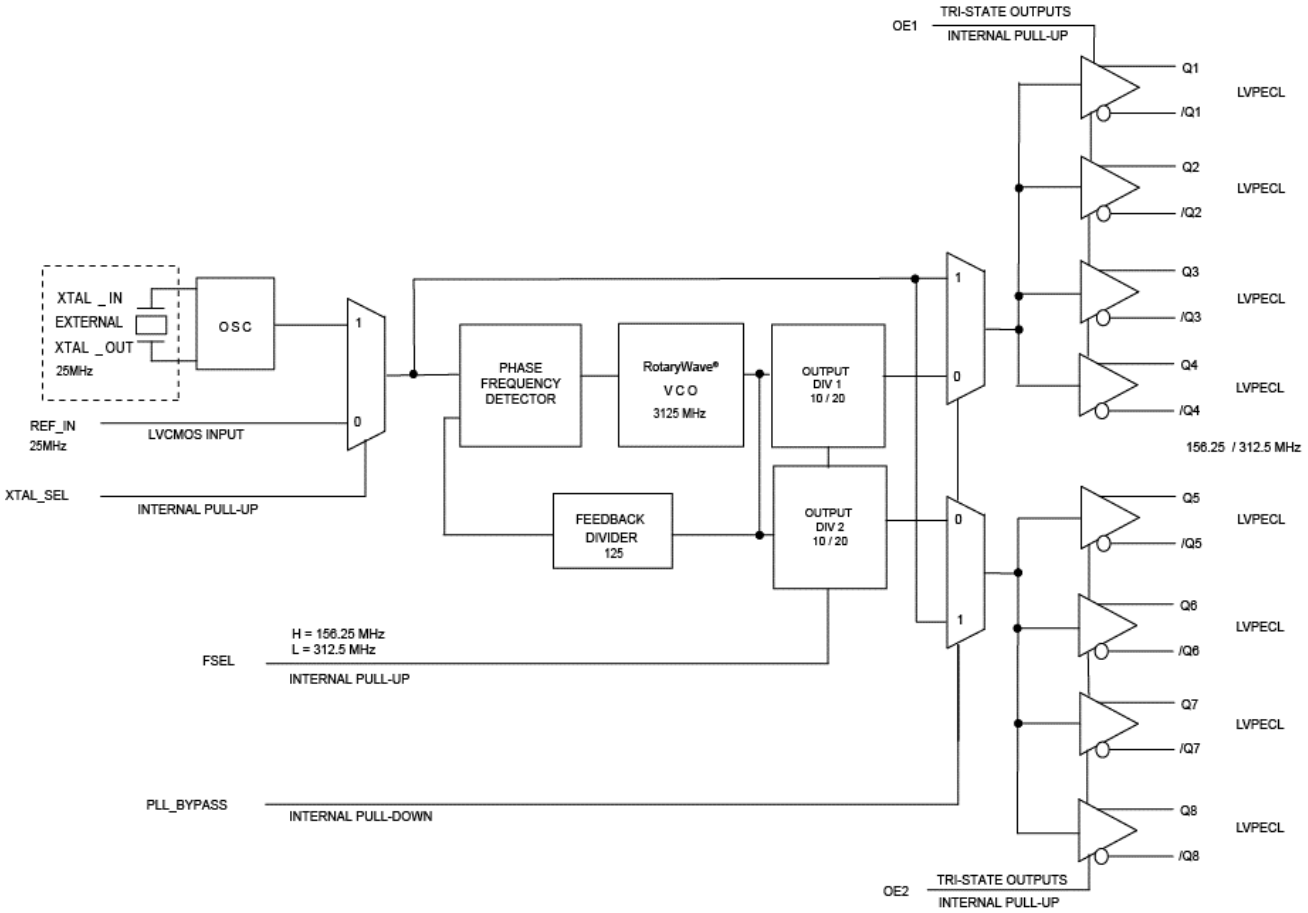
The device operates from a 3.3V or 2.5V power supply and synthesizes eight LVPECL output clocks at 156.25MHz or 312.5MHz. The SM802128 accepts a 25 MHz crystal or LVCMOS reference clock.

Data sheet and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Generates eight LVPECL clocks at 156.25MHz or 312.5MHz
- 2.5V or 3.3V operating range
- Typical phase jitter @ 156.25MHz (1.875MHz to 20MHz): 110fs with crystal reference
- Industrial temperature range (–40°C to +85°C)
- Green, RoHS, and PFOS compliant
- Available in 44-pin 7mm × 7mm QFN package

Block Diagram



ClockWorks is a trademark of Micrel, Inc
RotaryWave is a registered trademark of Multigig, Inc.

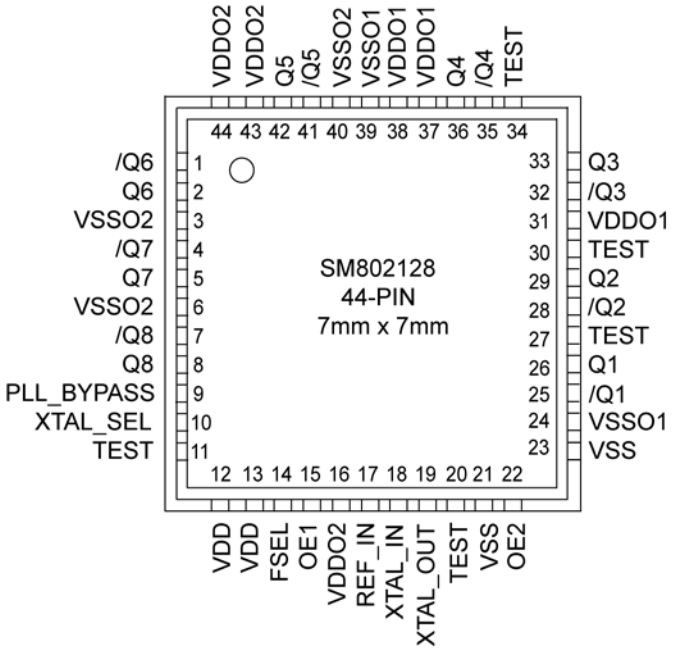
Ordering Information [1]

Part Number	Marking	Shipping	Temperature Range	Package
SM802128UMG	802128	Tray	–40°C to +85°C	44-Pin QFN
SM802128UMGTR	802128	Tape and Reel	–40°C to +85°C	44-Pin QFN

Note:

1. Devices are Green, RoHS, and PFOS compliant.

Pin Configuration



44-Pin QFN
(Top View)

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
25, 26 28, 29 32, 33 35, 36	/Q1, Q1 /Q2, Q2 /Q3, Q3 /Q4, Q4	O, (DIF)	LVPECL	Differential Clock Outputs from Bank 1 (156.25MHz or 312.5MHz).
41, 42 1, 2 4, 5 7, 8	/Q5, Q5 /Q6, Q6 /Q7, Q7 /Q8, Q8	O, (DIF)	LVPECL	Differential Clock Outputs from Bank 2 (156.25MHz or 312.5MHz).
31, 37, 38	VDDO1	PWR		Power Supply for the Outputs on Bank 1.
43, 44, 16	VDDO2	PWR		Power Supply for the Outputs on Bank 2.
24, 39	VSSO1	PWR		Power Supply Ground for the Outputs on Bank 1.

Pin Description (continued)

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
3, 6, 40	VSSO2	PWR		Power Supply Ground for the Outputs on Bank 2
11, 20, 27, 30, 34	TEST			Factory Test Pins. Do not connect anything to these pins.
12, 13	VDD	PWR		Core Power Supply
21, 23	VSS (Exposed Pad)	PWR		Core Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
17	REF_IN	I, (SE)	LVCMOS	Reference Clock Input
18	XTAL_IN	I, (SE)	Crystal	Crystal Reference Input, no load caps needed (See Figure 5).
19	XTAL_OUT	O, (SE)	Crystal	Crystal Reference Output, no load caps needed (See Figure 5).
15	OE1	I, (SE)	LVCMOS	Output Enable, Q1-Q4 disables to tri-state, 0 = Disabled, 1 = Enabled, 45KΩ Pull-Up.
22	OE2	I, (SE)	LVCMOS	Output Enable, Q5-Q8 disables to tri-state, 0 = Disabled, 1 = Enabled, 45KΩ Pull-Up.
9	PLL_BYPASS	I, (SE)	LVCMOS	PLL Bypass, Selects Output Source 0 = Normal PLL Operation 1 = Output from Input Reference Clock or Crystal 45KΩ Pull-Down
10	XTAL_SEL	I, (SE)	LVCMOS	Selects PLL Input Reference Source 0 = REF_IN, 1 = XTAL, 45KΩ Pull-Up
14	FSEL	I, (SE)	LVCMOS	Frequency Select, 1 = 156.25MHz, 0 = 312.5MHz, 45KΩ Pull-Up

Truth Tables

OE1/2	
0	Tri-state
1	LVPECL

FSEL	Output Frequency (MHz)
0	312.5
1	156.25

PLL_BYPASS/CSB	XTAL_SEL		
0	–	–	PLL
1	–	–	XTAL/REF_IN
–	0	REF_IN	–
–	1	XTAL	–

Absolute Maximum Ratings [1]

Supply Voltage (V_{DD}, $V_{DDO1/2}$) ……..…….+4.6V
Input Voltage (V_{IN})……-0.50V to V_{DD}+0.5V
Lead Temperature (soldering, 20sec.)……260°C
Case Temperature……115°C
Storage Temperature (T_s)……...-65°C to +150°C

Operating Ratings [2]

Supply Voltage ($V_{DD,}$ $V_{DDO1/2}$)..... +2.375V to +3.465V
Ambient Temperature (T_A)..... –40°C to +85°C
Junction Thermal Resistance[3]
QFN (θ_{JA})
Still-Air ..... 24°C/W
QFN (ψ_{JB})
Junction-to-Board ..... 8°C/W

DC Electrical Characteristics [4]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
T_A = -40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}, $V_{DDO1/2}$	2.5V Operating Voltage	V_{DDO1}=V_{DDO2}	2.375	2.5	2.625	V
V_{DD}, $V_{DDO1/2}$	3.3V Operating Voltage	V_{DDO1}=V_{DDO2}	3.135	3.3	3.465	V
I_{DD}	Supply current V_{DD} + V_{DDO} Outputs open	156.25MHz		220	275	mA
		312.5MHz		275	345	

LVPECL DC Electrical Characteristics [4]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
T_A = –40°C to +85°C. R_L = 50Ω to V_{DDO}-2V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage		V_{DDO} – 1.145	V_{DDO} – 0.97	V_{DDO} – 0.845	V
V_{OL}	Output Low Voltage		V_{DDO} – 1.945	V_{DDO} – 1.77	V_{DDO} – 1.645	V
V_{SWING}	Output Voltage Swing		0.6	0.8	1.0	V

LVCMOS (PLL_BYPASS, XTAL_SEL, OE1, OE2, FSEL) DC Electrical Characteristics [4]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	–150			µA

REF_IN DC Electrical Characteristics[4]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = -40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		1.1		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.6	V
I_{IN}	Input Current	XTAL_SEL = V_{IL}, V_{IN} = 0V to V_{DD}	–5		5	µA
		XTAL_SEL = V_{IH}, V_{IN} = V_{DD}		20		µA

Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	10pF Load	Fundamental, Parallel Resonant			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitor, C0			1	5	pF
Correlation Drive Level			10	100	uW

AC Electrical Characteristics[4, 5]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C. R_L = 50Ω to V_{DDO} – 2V

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{OUT1}	Output Frequency 1	FSEL = 1		156.25		MHz
F_{OUT2}	Output Frequency 2	FSEL = 0		312.5		MHz
F_{REF}	Reference Input Frequency			25		MHz
T_R/T_F	LVPECL Output Rise/Fall Time	20% – 80%	80	175	350	ps
ODC	Output Duty Cycle		48	50	52	%
T_{SKEW}	Output-to-Output Skew	Q1 – Q8 [6]			45	ps
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter[7]	156.25MHz Integration Range (1.875MHz – 20MHz) Integration Range (12kHz – 20MHz) 312.5MHz Integration Range (1.875MHz – 20MHz) Integration Range (12kHz – 20MHz)		110 250 110 250		fs
	Spurious Noise Components	6.25MHz using 156.25MHz 12.5MHz using 312.5MHz		-80 -85		dBc

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the above table after thermal equilibrium has been established.
5. All phase–noise measurements were taken with an Agilent 5052B phase–noise system.
6. Defined as skew between outputs at the same supply voltage and with equal load conditions and same frequency; measured at the output differential crossing points.
7. Measured using a 25MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz offset frequency.

Application Information

Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

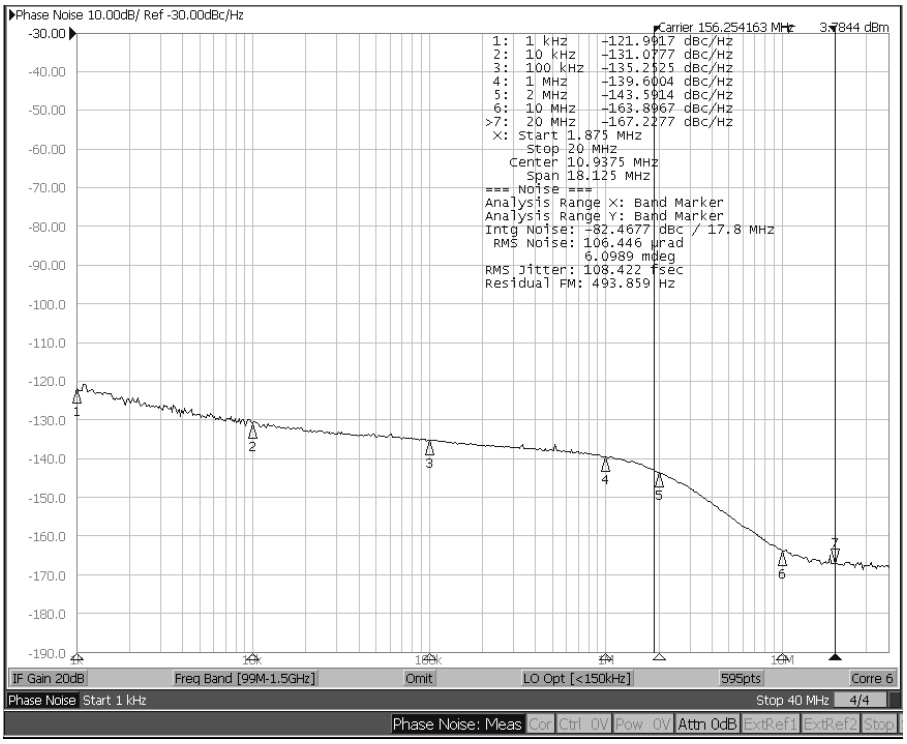
Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal.

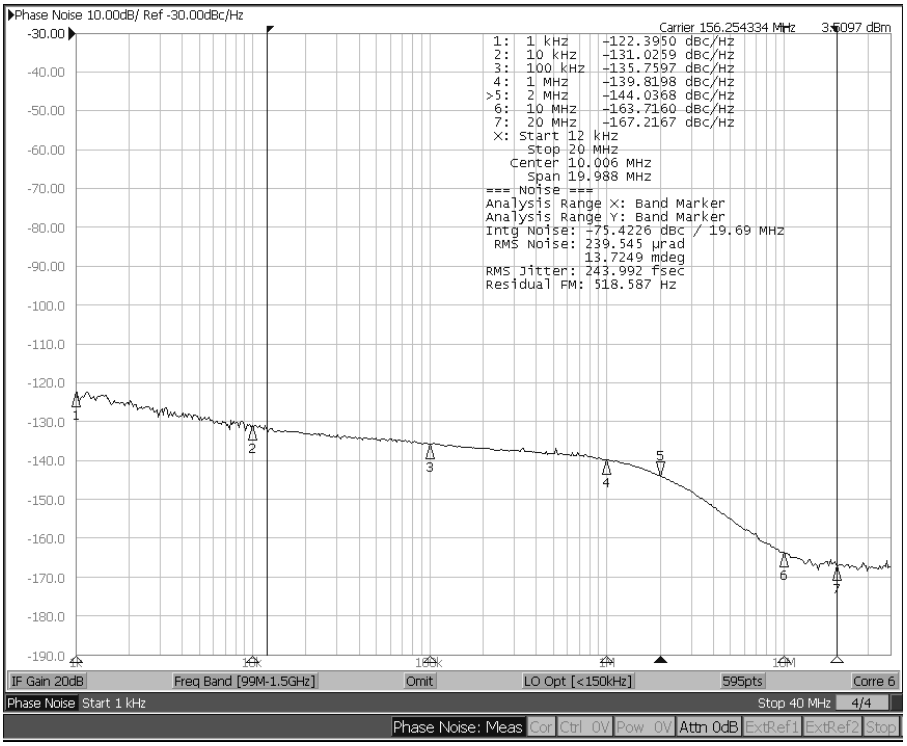
Crystal load capacitance is built inside the die so no external capacitance is needed. See the *Selecting a quartz crystal for the Clockworks Flex I Family of Precision Synthesizers* application note for further details.

Contact Micrel's HBW applications group if you need assistance on selecting a suitable crystal for your application at: hbwhelp@micrel.com.

Phase Noise Plots

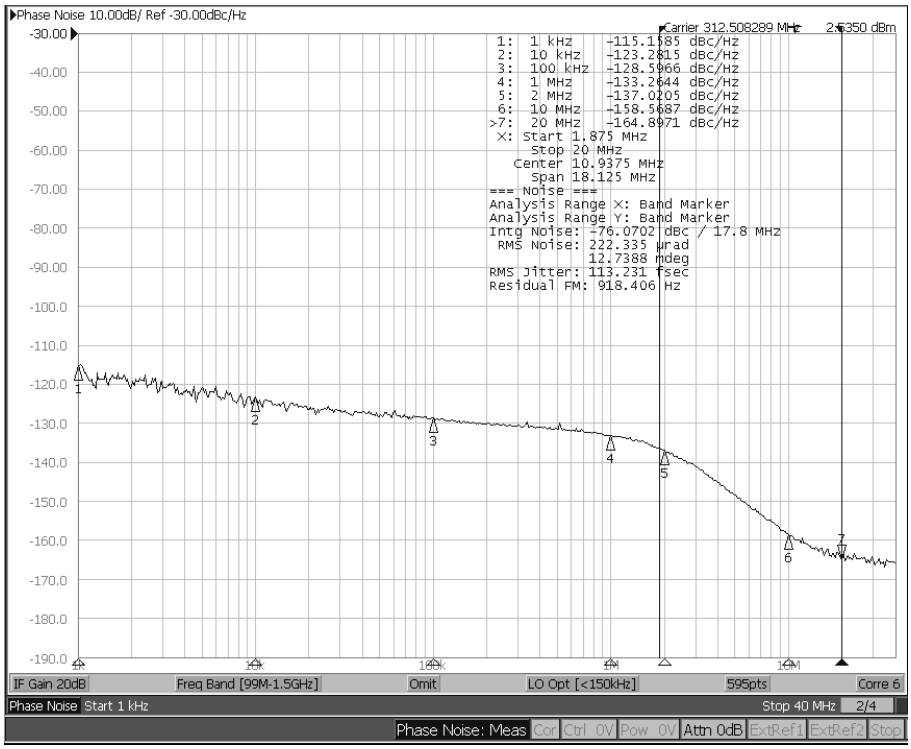


Phase Noise Plot: 156.25MHz, 1.875MHz – 20MHz 108fs

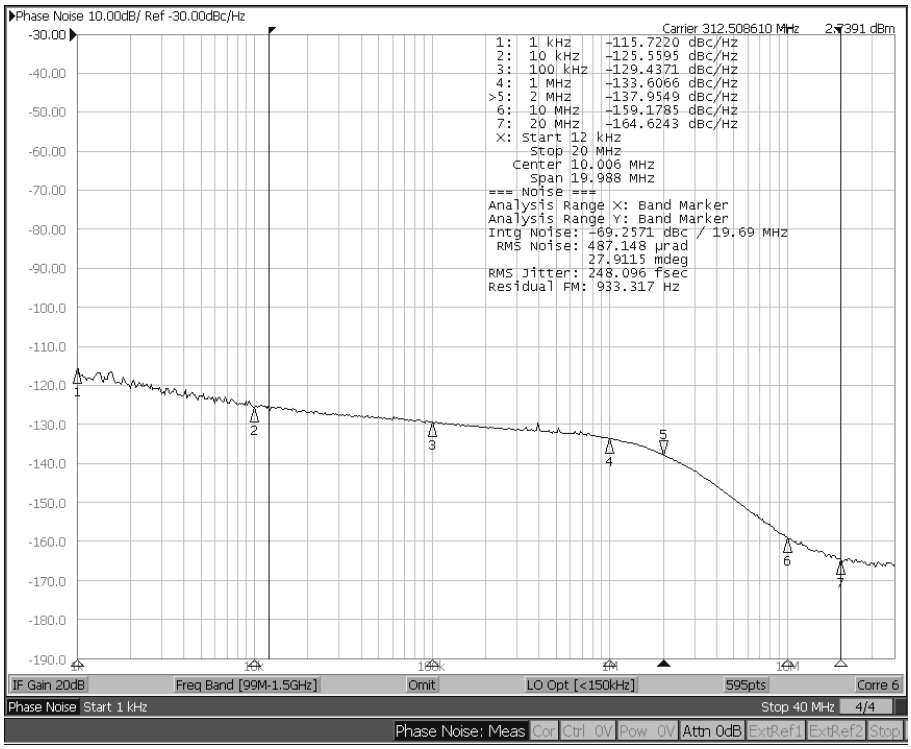


Phase Noise Plot: 156.25MHz, 12kHz – 20MHz 244fs

Phase Noise Plots (Continued)



Phase Noise Plot: 312.5MHz, 1.875MHz – 20MHz 113fs



Phase Noise Plot: 312.5MHz, 12kHz – 20MHz 248fs

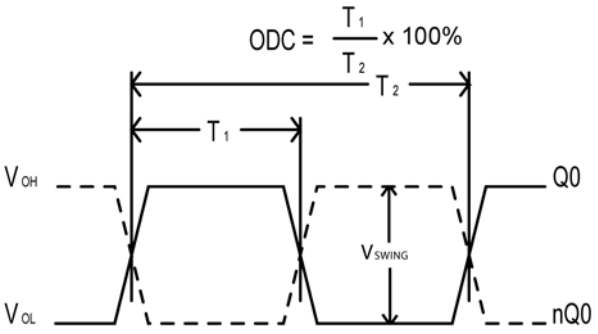


Figure 1. Duty Cycle Timing

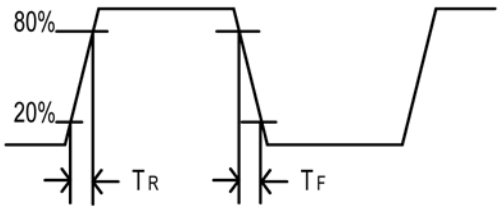


Figure 2. All Outputs Rise/Fall Time

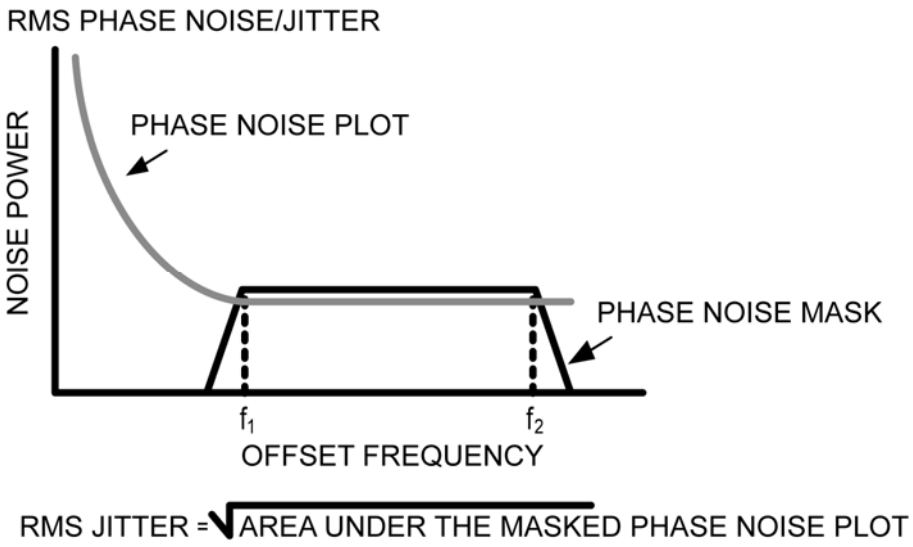


Figure 3. RMS Phase/Noise/Jitter

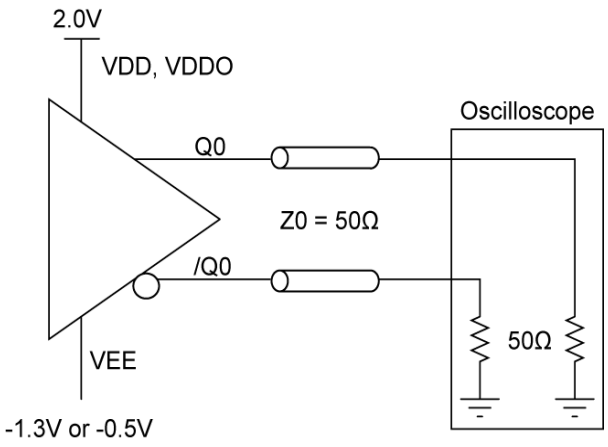


Figure 4. LVPECL Output Load

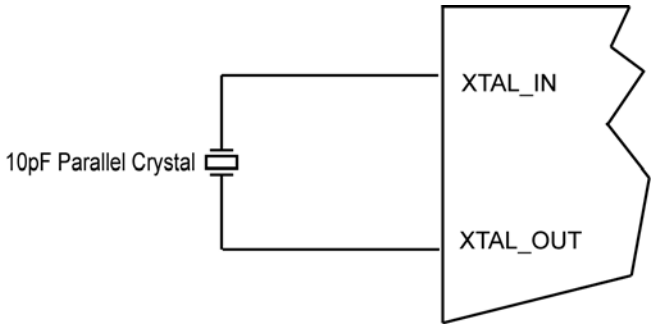
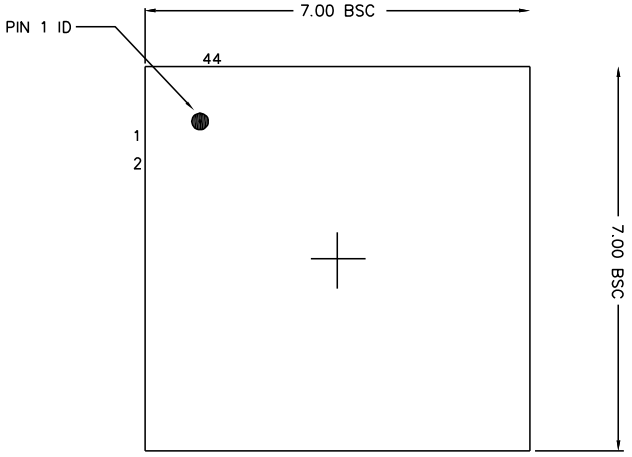
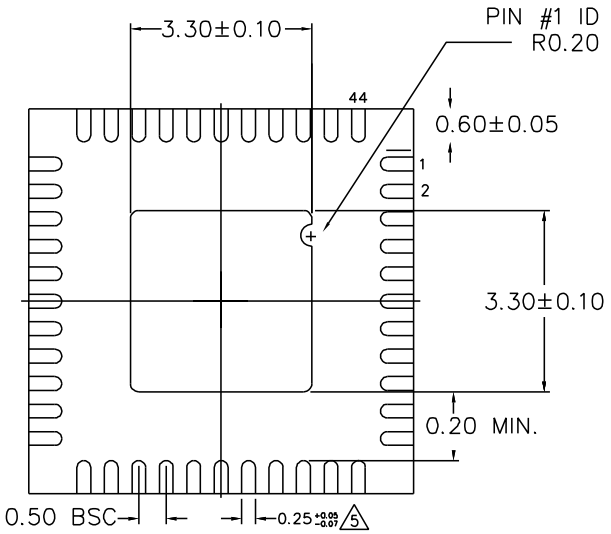


Figure 5. Crystal Input Interface

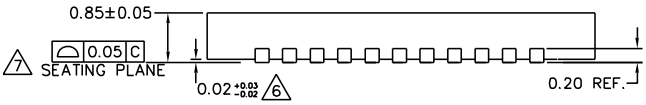
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

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