

16-Bit Registered Transceivers

Features

- I_{off} supports partial-power-down mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

CY74FCT16652T Features:

- 64 mA sink current, 32 mA source current
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

CY74FCT162652T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

Functional Description

These 16-bit, high-speed, low-power, registered transceivers that are organized as two independent 8-bit bus transceivers with three-state D-type registers and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. OEAB and OEBA control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer.

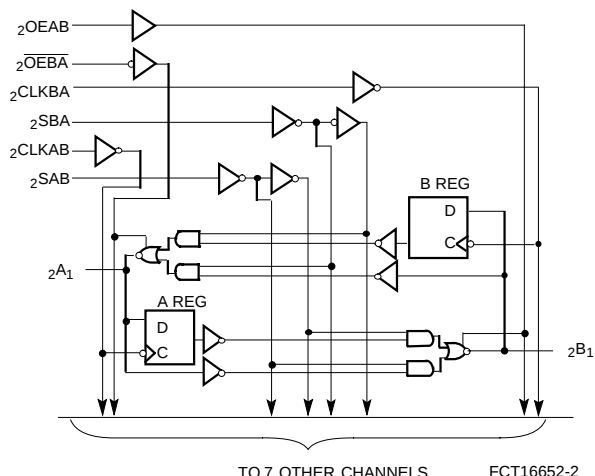
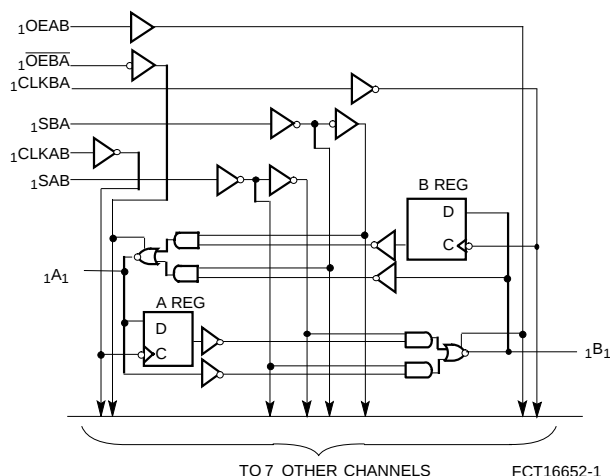
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CLKAB or CLKBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16652T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162652T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162652T is ideal for driving transmission lines.

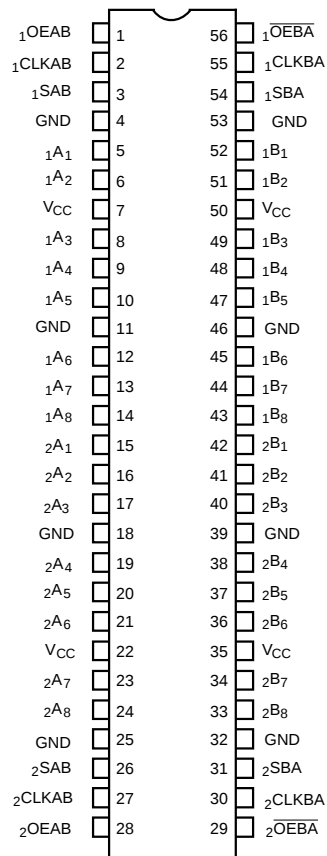
Logic Block Diagrams



Pin Configuration

SSOP/TSSOP

Top View



FCT16652-3

Pin Description

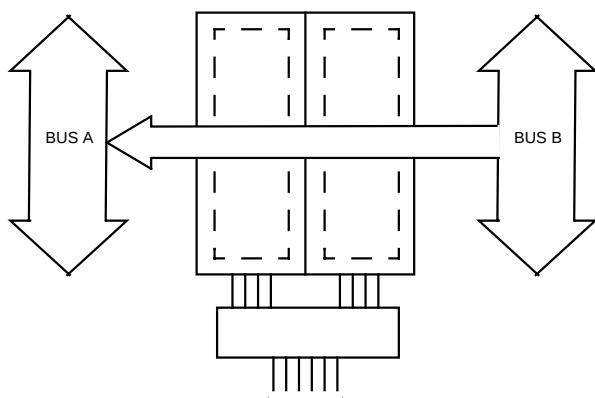
Name	Description
A	Data Register A Inputs Data Register B Outputs
B	Data Register B Inputs Data Register A Outputs
CLKAB, CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
OEAB, OEBA	Output Enable Inputs

Function Table^[1]

Inputs						Data I/O ^[2]		Operation or Function
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A	B	
L L	H H	H or L ┐	H or L ┐	X X	X X	Input	Input	Isolation Store A and B Data
X H	H H	┐ ┐	H or L ┐	X X ^[3]	X X	Input Input	Unspecified ^[2] Output	Store A, Hold B Store A in Both Registers
L L	X L	H or L ┐	┐ ┐	X X	X X ^[3]	Unspecified ^[2]	Input Input	Hold A, Store B Store B in both Registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

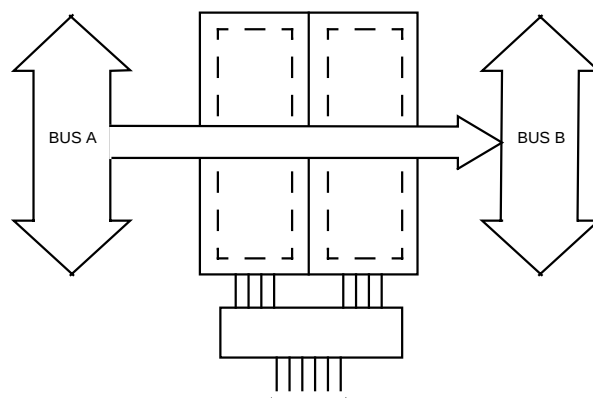
Notes:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
┐ = LOW-to-HIGH Transition
2. The data output functions may be enabled or disabled by various signals at the OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
3. Select control=L; clocks can occur simultaneously.
Select control=H; clocks must be staggered to load both registers.



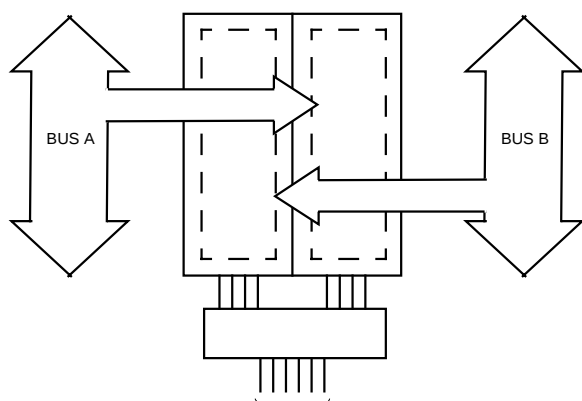
OEAB L OEBA L CLKAB X CLKBA X SAB X SBA L

**Real-Time Transfer
Bus B to Bus A**



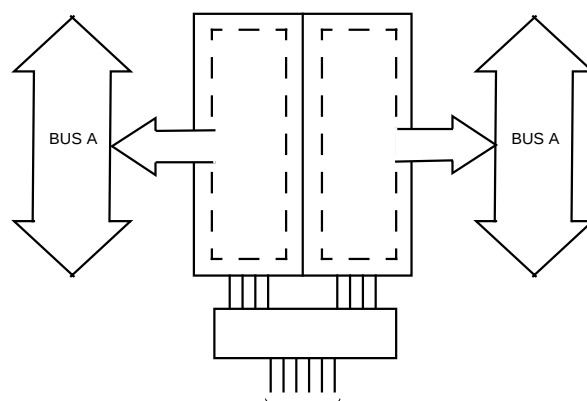
OEAB H OEBA L CLKAB X CLKBA X SAB L SBA X

**Real-Time Transfer
Bus A to Bus B**



OEAB X L L OEBA H X H CLKAB X CLKBA X SAB X X X SBA X X X

**Storage from
A and/or B**



OEAB H OEBA L CLKAB H or L CLKBA H or L SAB H SBA H

**Transfer Stored Data
to A and/or B**

Maximum Ratings^[4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage TemperatureCom'l -55°C to +125°C

Ambient Temperature with
Power AppliedCom'l -55°C to +125°C

DC Input Voltage-0.5V to +7.0V

DC Output Voltage-0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin)-60 to +120 mA

Power Dissipation1.0W

Static Discharge Voltage.....>2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	5V ± 10%

Note:

- Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions ^[5]	Min.	Typ. ^[6]	Max.	Unit
V _{IH}	Input HIGH Voltage	Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Logic LOW Level			0.8	V
V _H	Input Hysteresis			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	μA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	μA
I _{OS}	Short Circuit Current ^[8]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[8]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V ^[7]			±1	μA

Output Drive Characteristics for CY74FCT16652T

Parameter	Description	Test Conditions ^[5]	Min.	Typ. ^[6]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162652T

Parameter	Description	Test Conditions ^[5]	Min.	Typ. ^[6]	Max.	Unit
I _{ODL}	Output LOW Current ^[8]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[8]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance (T_A = +25°C, f = 1.0 MHz)

Parameter	Description ^[10]	Test Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Notes:

5. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
6. Typical values are at V_{CC}=5.0V, +25°C ambient.
7. Tested at T_A= +25°C.
8. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
9. Duration of the condition cannot exceed one second.
10. This parameter is measured at characterization but not tested.

Power Supply Characteristics

Param.	Description	Test Conditions ^[11]		Min.	Typ. ^[12]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$	—	5	500	μA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V$ ^[13]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ^[14]	$V_{CC} = \text{Max.}$ Outputs Open $OEAB = \overline{OEAB} = GND$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ or $V_{IN} = GND$	—	75	120	$\mu A / MHz$
I_C	Total Power Supply Current ^[15]	$V_{CC} = \text{Max.}$ Outputs Open $f_0 = 10 \text{ MHz (CLKBA)}$ 50% Duty Cycle $OEAB = \overline{OEAB} = GND$ One-Bit Toggling $f_1 = 5 \text{ MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ or $V_{IN} = GND$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ or $V_{IN} = GND$	—	1.3	3.2	mA
		$V_{CC} = \text{Max.}$ Outputs Open $f_0 = 10 \text{ MHz (CLKBA)}$ 50% Duty Cycle $OEAB = \overline{OEAB} = GND$ Sixteen Bits Toggling $f_1 = 2.5 \text{ MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ or $V_{IN} = GND$	—	3.8	6.5 ^[16]	mA
			$V_{IN} = 3.4V$ or $V_{IN} = GND$	—	8.3	20.0 ^[16]	mA

Notes:

11. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
12. Typical values are at $V_{CC} = 5.0V$ +25° ambient.
13. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
14. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
15. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
All currents are in milliamps and all frequencies are in megahertz.
16. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range^[17]

Parameter	Description	CY74FCT16652AT CY74FCT162652AT		Unit	Fig. No. ^[18]
		Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	1.5	6.3	ns	1, 3
t _{PZH} t _{PHL}	Output Enable Time OEAB or $\overline{\text{OEBA}}$ to Bus	1.5	9.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OEAB or $\overline{\text{OEBA}}$ to Bus	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	1.5	6.3	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to Bus	1.5	7.7	ns	1, 5
t _{SU}	Set-Up time HIGH or LOW Bus to Clock	2.0	—	ns	4
t _H	Hold Time HIGH or LOW Bus to Clock	1.5	—	ns	4
t _W	Clock Pulse Width HIGH or LOW	5.0	—	ns	5
t _{SK(O)}	Output Skew ^[19]	—	0.5	ns	

Parameter	Description	CY74FCT16652CT CY74FCT162652CT		Unit	Fig. No. ^[18]
		Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	1.5	5.4	ns	1, 3
t _{PZH} t _{PHL}	Output Enable Time OEAB or $\overline{\text{OEBA}}$ to Bus	1.5	7.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OEAB or $\overline{\text{OEBA}}$ to Bus	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	1.5	5.7	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to Bus	1.5	6.2	ns	1, 5
t _{SU}	Set-Up Time HIGH or LOW Bus to Clock	2.0	—	ns	4
t _H	Hold Time HIGH or LOW Bus to Clock	1.5	—	ns	4
t _W	Clock Pulse Width HIGH or LOW	5.0	—	ns	5
t _{SK(O)}	Output Skew ^[19]	—	0.5	ns	

Notes:

17. Minimum limits are specified, but not tested, on propagation delays.

18. See "Parameter Measurement Information" in the General Information section.

19. Skew between any two outputs of the same package switching in the same direction. This parameter ensured by design.

Ordering Information CY74FCT16652

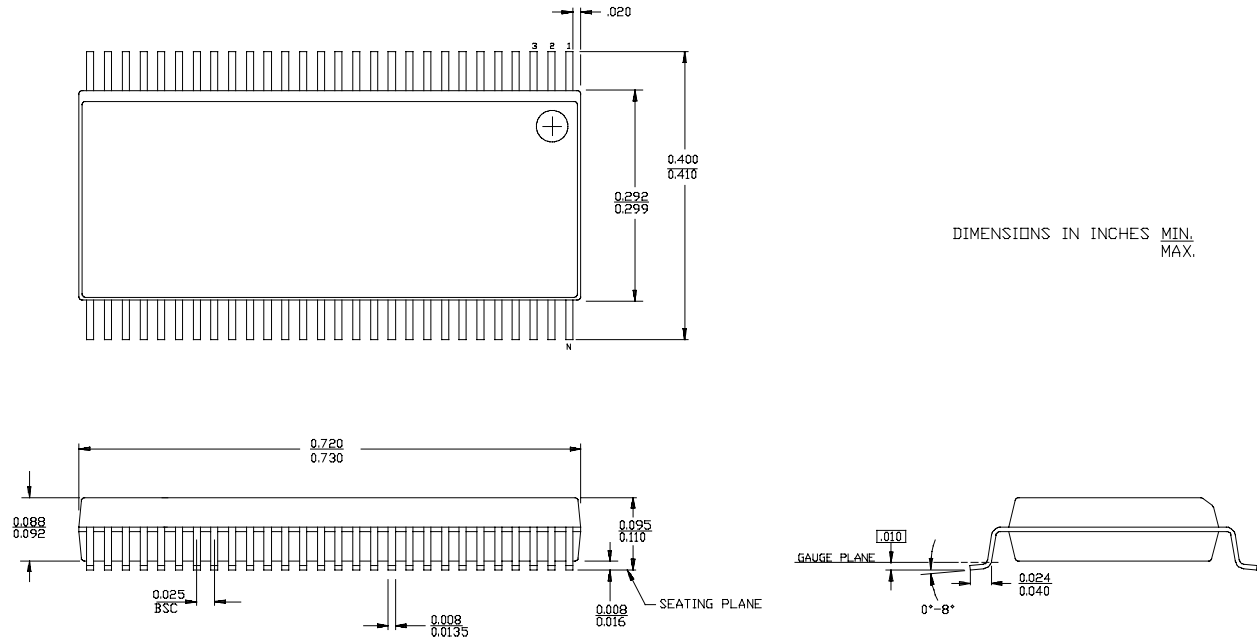
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT16652CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial
6.3	CY74FCT16652ATPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial

Ordering Information CY74FCT162652

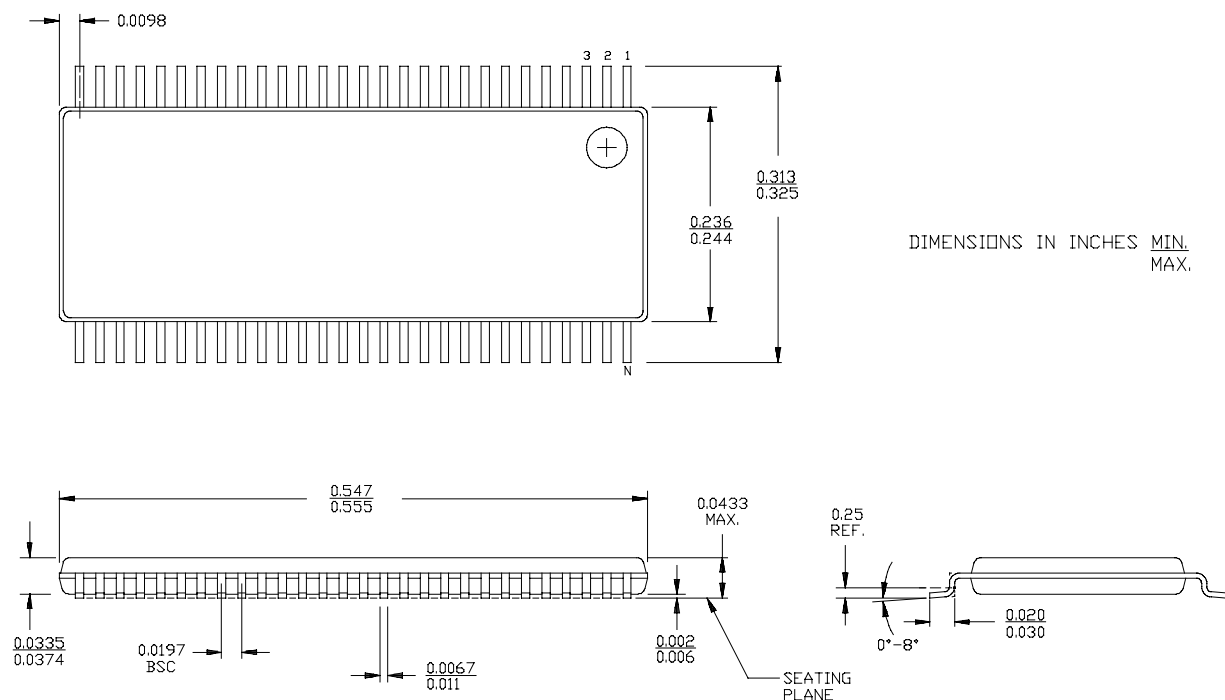
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	74FCT162652CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162652CTPVC	O56	56-Lead (300-Mil) SSOP	
	74FCT162652CTPVCT	O56	56-Lead (300-Mil) SSOP	
6.3	CY74FCT162652ATPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162652ATPVCT	O56	56-Lead (300-Mil) SSOP	

Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74FCT162652CTPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85	FCT162652C	
CY74FCT16652ATPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85	FCT16652A	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

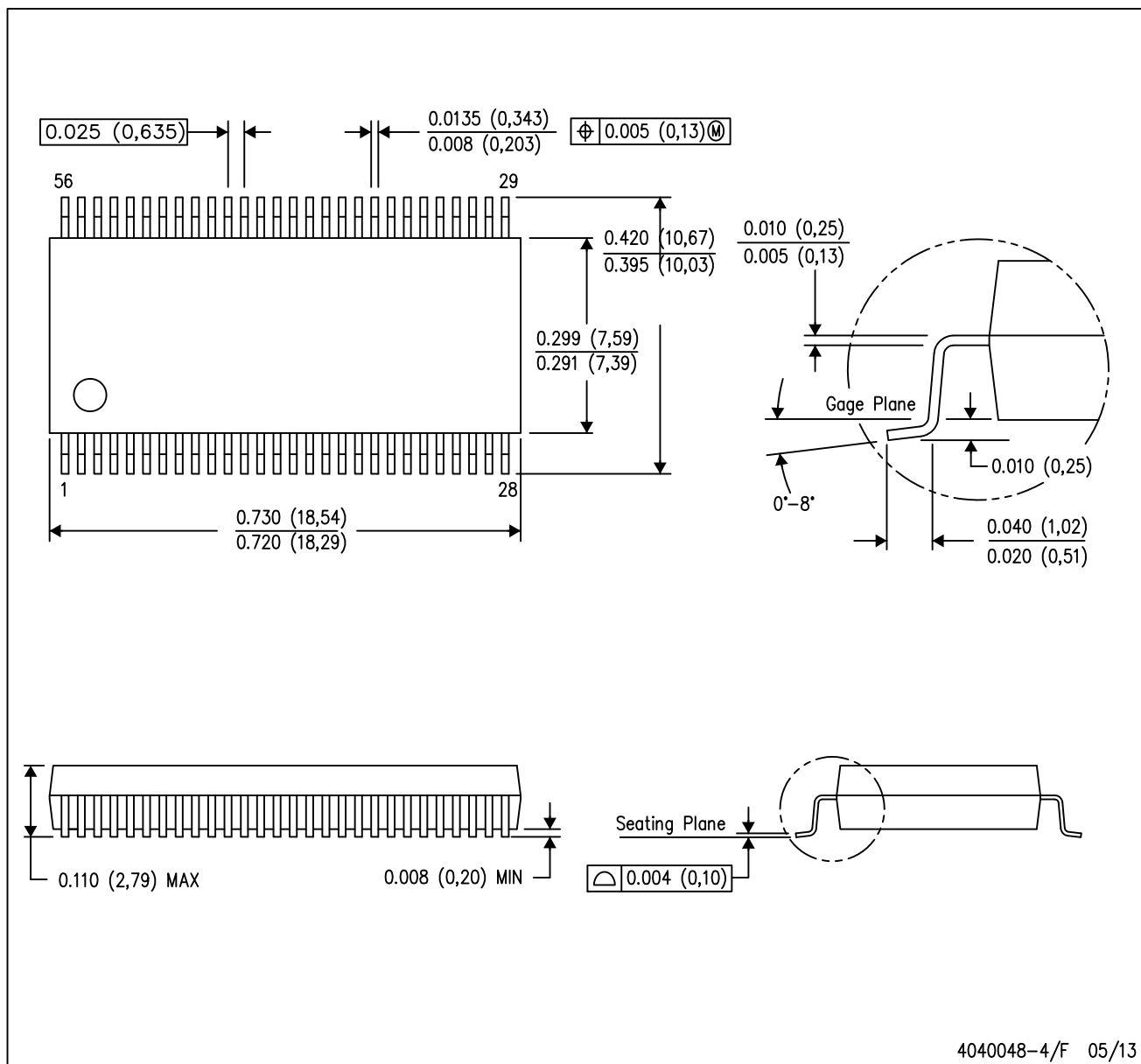
⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

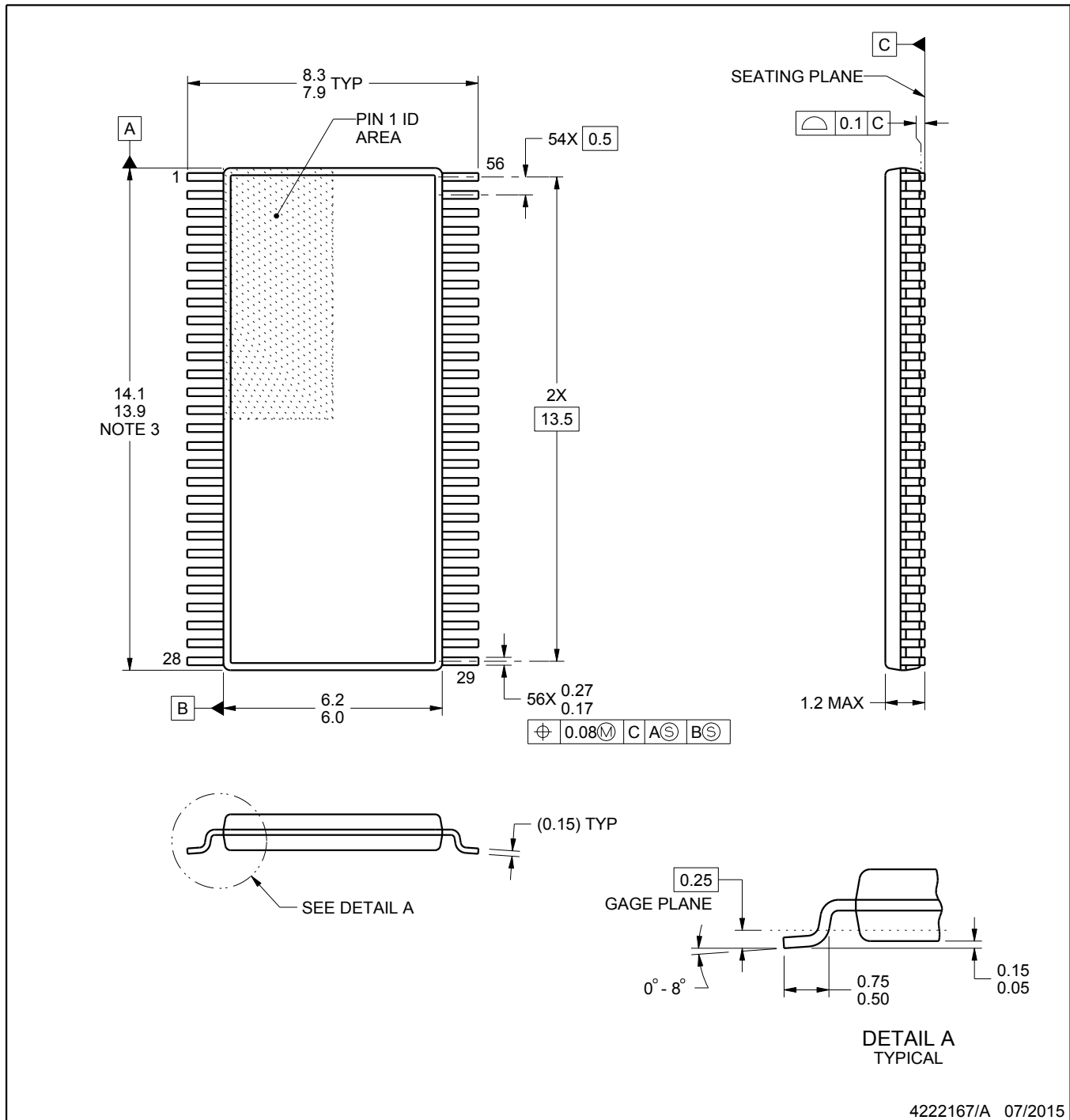
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118



4222167/A 07/2015

NOTES:

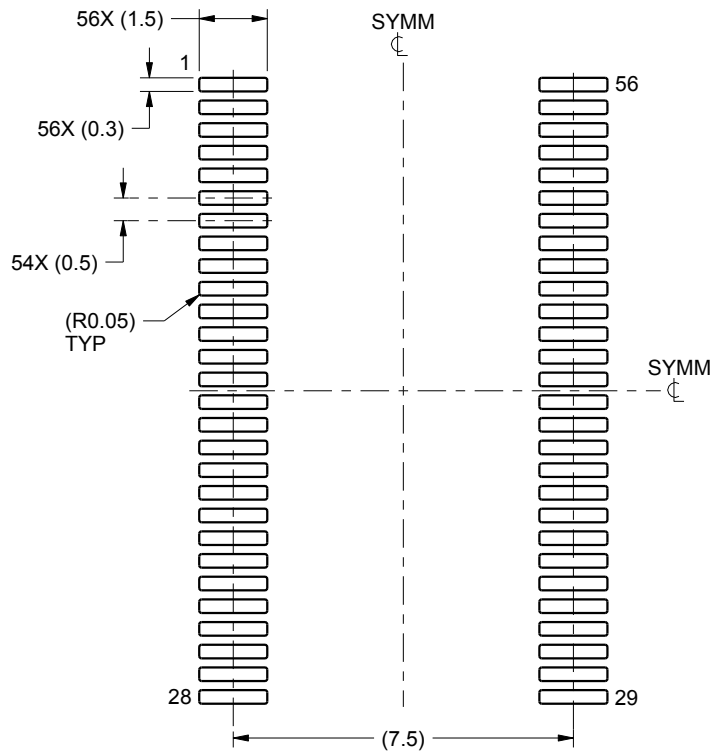
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

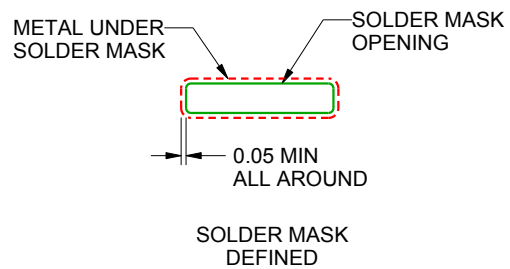
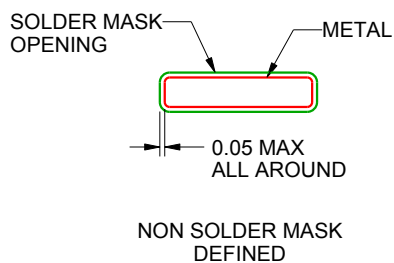
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

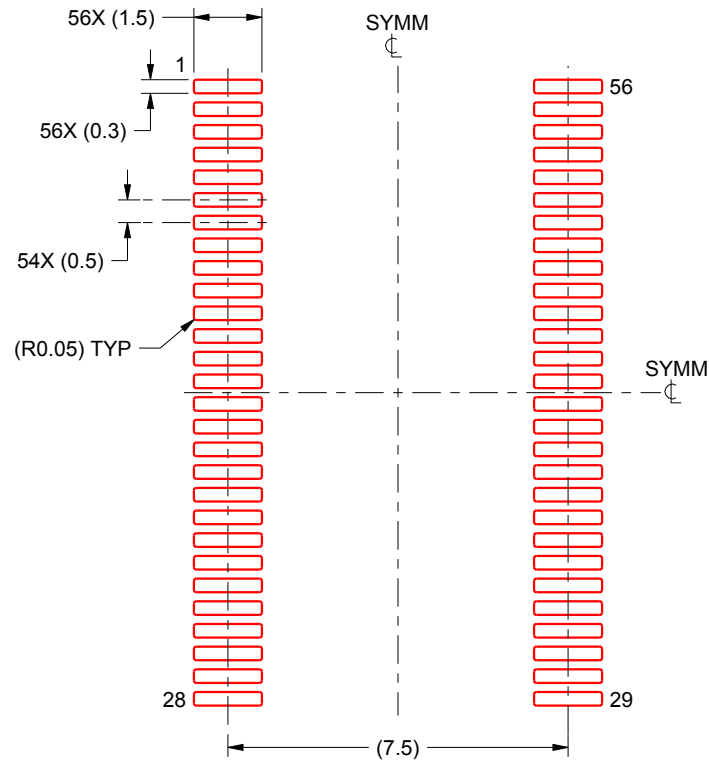
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated