AN-1958 LMP860x SOIC Evaluation Board

1 Introduction

The LMP860x SOIC Evaluation Board, Figure 1, is designed to evaluate current sense amplifiers like the LMP8601, LMP8602, and LMP8603. These all are 60V Common Mode, Bidirectional Precision Current Sensing amplifier with different gain. This board has a LMP860X part mounted on the PCB together with the required de-coupling capacitor, power supply connections, Input and Output connectors and a 3 pin header for connecting the offset pin to either GND or V_S.

2 General Description

The LMP860x and LMP860xQ are fixed gain precision amplifiers. The part amplifies and filters small differential signals in the presence of high common mode voltages. The input common mode voltage range is −22V to +60V when operating from a single 5V supply. With 3.3V supply, the input common mode voltage range is from −4V to +27V. The LMP860x and LMP860xQ are members of the Linear Monolitic Precision (LMP™) family and are ideal parts for unidirectional and bidirectional current sensing applications.

The parts have a precise gain (LMP8601 20x, LMP8602 50x, LMP8603 100x) that is adequate in most targeted applications to drive an ADC to its full scale value. The fixed gain is achieved in two separate stages, a preamplifier with a gain of 10x and an output stage buffer amplifier with a gain of 2x, 5x, 10x. The connection between the two stages of the signal path is brought out on two pins to enable the possibility to create an additional filter network around the output buffer amplifier. These pins can also be used for alternative configurations with different gain as described in the applications information section of the data sheet (SNOSAR2 or SNOSB36).

The mid-rail offset adjustment pin enables the user to use these devices for bidirectional single supply voltage current sensing. The output signal is bidirectional and mid-rail referenced when this pin is connected to the positive supply rail. With the offset pin connected to ground, the output signal is unidirectional and ground-referenced.

The LMP860xQ incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC Q100 standard.

3 LMP860x Operating Conditions

- Temperature Range −40°C to 125°C
- Power Supply Voltage 3.0V ≤ V_S ≤ 5.5V
- CMVR at V_S = 3.3V −4V to 27V
- CMVR at V_S = 5.0V −22V to 60V

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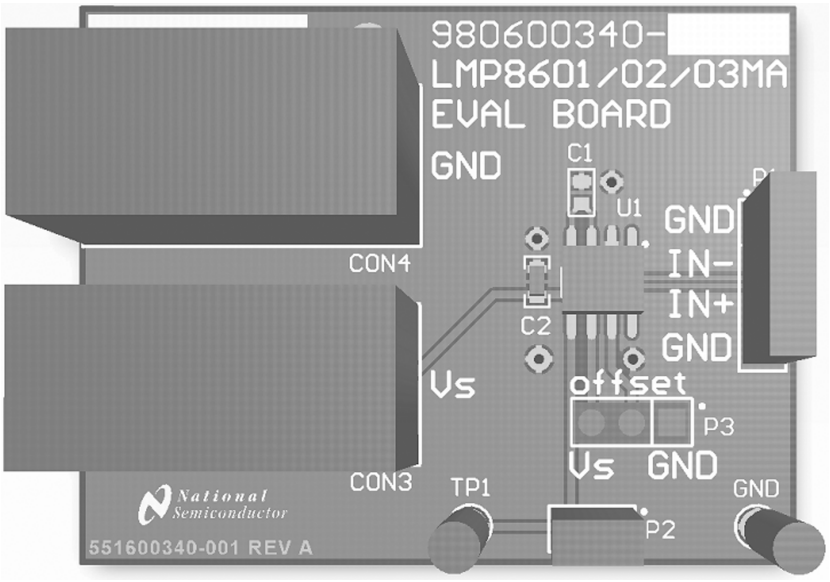

Figure 1. LMP860x Evaluation Board

4 Description of the LMP860x Evaluation Board

The LMP860x evaluation board requires a power supply with a voltage between 3.0V and 5.5V , the supply current will be <2 mA in normal operation with high impedance load on the output of the part. The positive supply voltage is connected to V_S (CON3) The negative supply voltage is connected to GND (CON4).

The offset voltage on the output of the LMP860x is determined by the voltage on the offset pin which is connected to pin2 of P3 and the offset voltage will be $V_{Offset}/2$. This pin is normally connected with a jumper to GND or V_S , but this pin can also be driven from a low impedance source (<10 Ω).

With a jumper on P3 between 2-3 the offset pin is connected to V_S and the offset voltage is half the value of V_S. In this configuration the LMP860x can be used for measuring bidirectional currents.

With a jumper on P3 between 1-2 the offset pin is connected to GND and the output voltage is ground referenced. In this configuration the LMP860x is used for measuring unidirectional currents.

The input signal is connected between -IN and +IN (P1 pin 2,3) and the output signal is available at OUT (P2).

On the board there is the possibility to place a capacitor C1 which creates a low pass filter between the first and second stage. This can be used to reduce the output noise and glitches that might appear from switching large common mode voltages with very fast transients at the input. (For more details about this filter, see the application information section of the LMP860x data sheet (SNOSAR2 or SNOSB36)).

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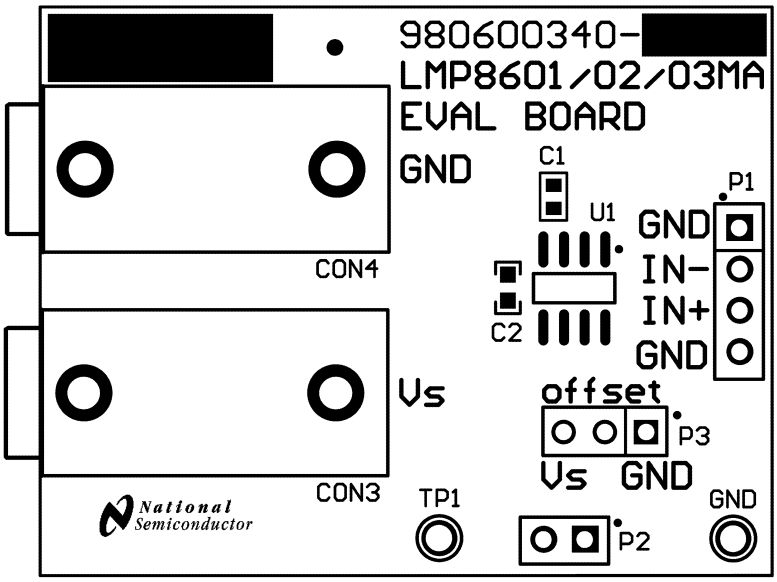

Figure 2. Power Supply Connectors and Headers

5 PCB Layout Guidelines

This section provides general practical guidelines for PCB layouts that use various power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results are predicated on the final layout.

5.1 Differential Signals

The two input pins of the LMP860x form a differential pair that must be handled following the rules given below:

- Keep both signals coupled by routing them closely together and keeping them of equal length.
- Do not allow any other signal in between these two signals of the differential pair.
- Keep all impedances in both traces of the signal equal.

5.2 Power, Ground, and De-Coupling

Keep the power supply de-coupling capacitor close to the power supply pin (V_S of the part.)

Make sure all return currents of the signals can flow next to the originating signals.

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6 Description of Headers and Connectors of the LMP860x Evaluation Board

The LMP860x Evaluation Board provides the following headers and connectors for connecting test equipment and supplying the LMP860x part.

Designator	Function or Use	Comment
P3	Offset selection	2–3 Mid rail offset (Bi-directional)1–2 Ground Referenced (unidirectional)
P1	GND	Pin1
	Input	Pin2 = Negative Input
		Pin3 = Positive Input
	GND	Pin4
P2	Output	Pin1 = GND Pin2 =ouput
CON3	supply V_S	
CON4	ground connection (GND)	

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7 Schematic With LMP8602MM Mounted

Figure 3 shows the LMP860x Evaluation board with a LMP8602MM mounted on the PCB. For versions of the MCB stuffed with LMP8601 or LMP8603, the only difference will be the gain of the part in the second stage.

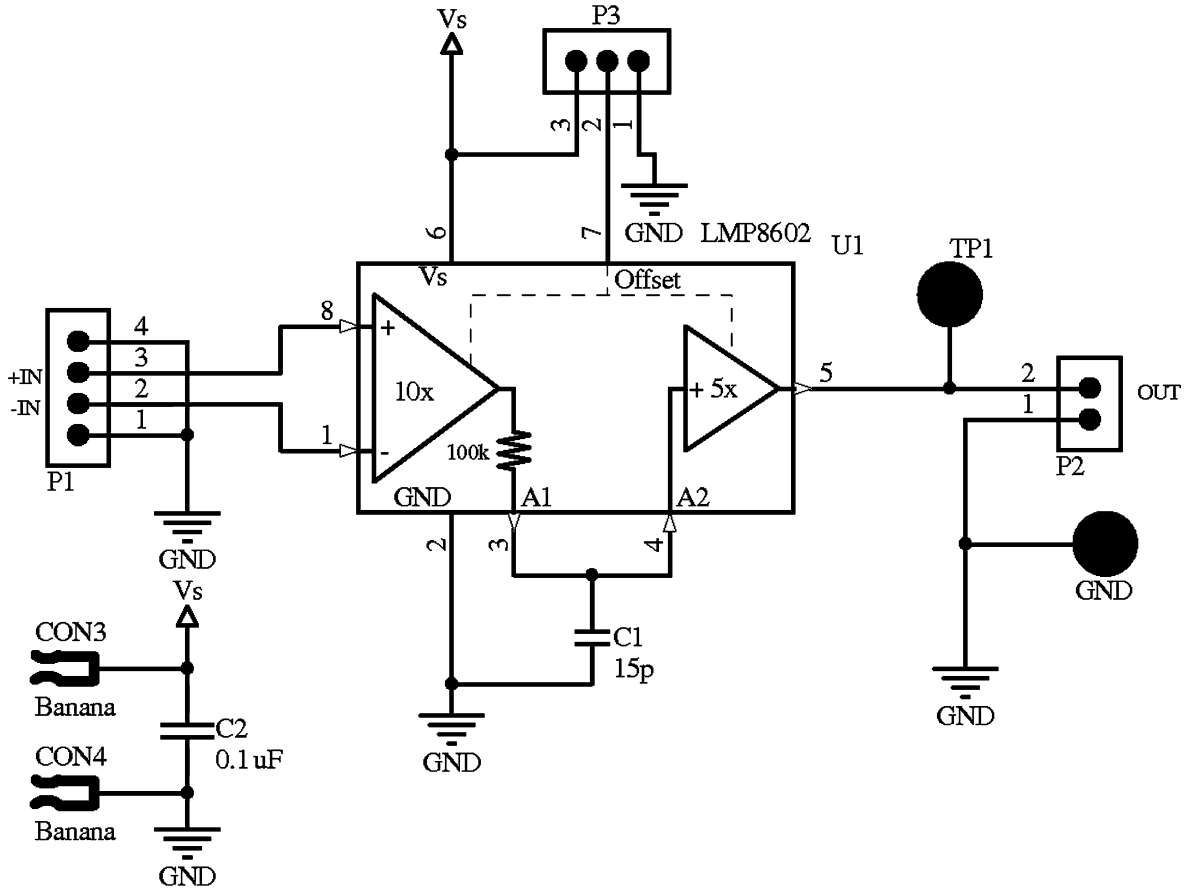

Figure 3. Schematic Diagram

8 Bill of Materials

Designator	Component	Value	Tolerance	Comment	Package Type
C1	Capacitor	N/A			0603
C2	Capacitor	100 nF			0603
P1	Header 4 pin			Input	
P2	Header 2 pin			Output	
P3	Header3 pin			Mid-rail Offset	Banana_COLOR
CON3	Banana plug	RED		V_S	Banana_COLOR
CON4	Banana plug	BLACK		GND	Banana_COLOR
U1	LMP860	LMP860			SOT

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9 Layout

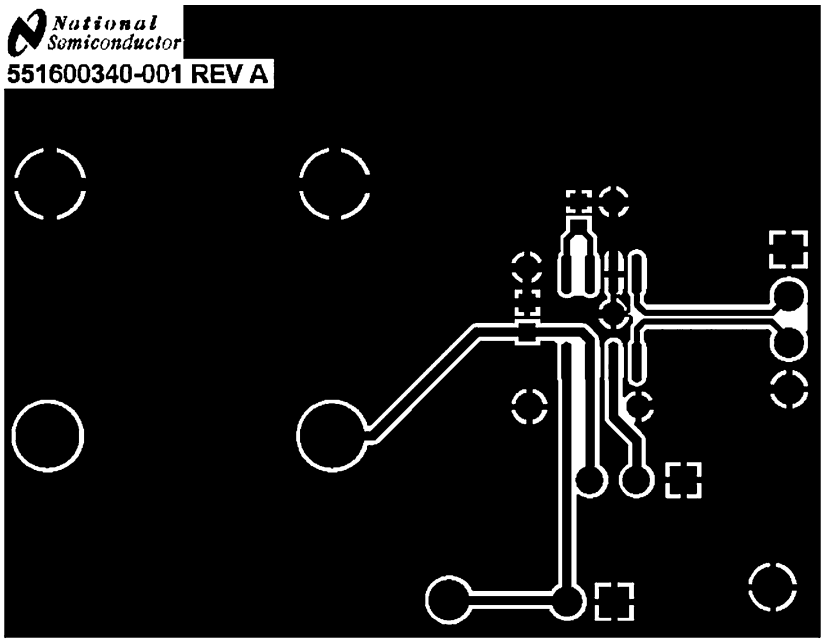

Figure 4. Layout, Top Layer

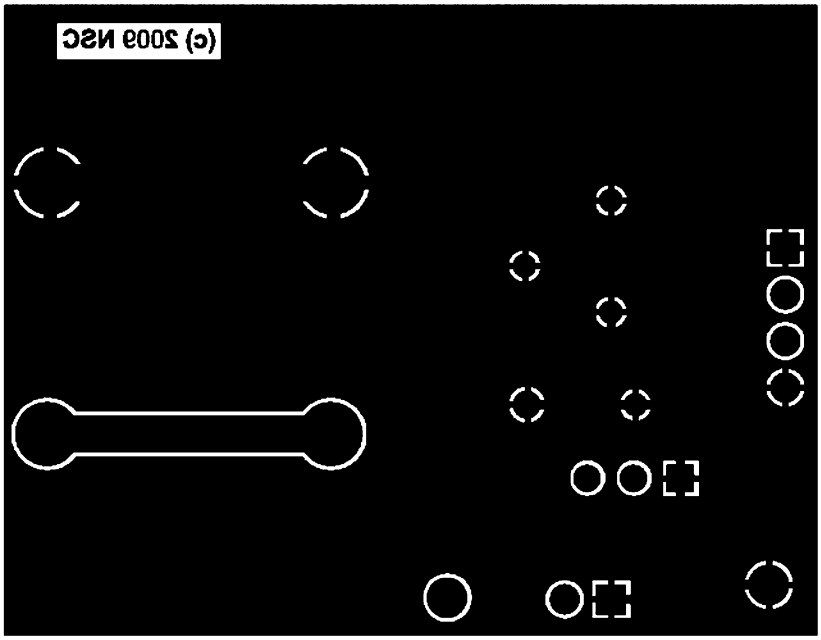

Figure 5. Layout, Bottom layer

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