

## Features

- Pin- and function-compatible with CY7C1049B
- High speed
  - $t_{AA} = 10$  ns
- Low active power
  - $I_{CC} = 90$  mA at 10 ns
- Low CMOS Standby power
  - $I_{SB2} = 10$  mA
- 2.0 V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Pb-free 36-pin (400-Mil) Molded SOJ package

## Functional Description

The CY7C1049D [1] is a high-performance CMOS static RAM organized as 512K words by 8 bits. Easy memory expansion is

provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

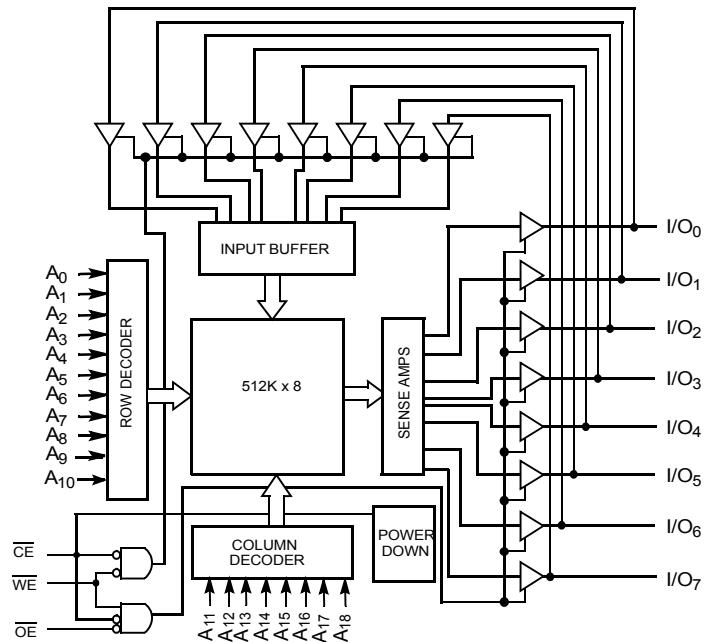
The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $CE$  LOW, and  $WE$  LOW).

The CY7C1049D is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.

The CY7C1049D is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



### Note

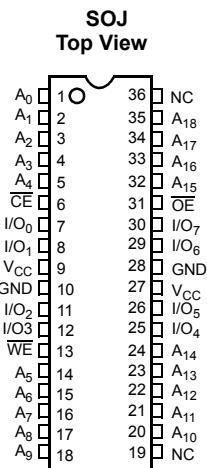
1. For guidelines on SRAM system design, refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

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## Pin Configuration

Figure 1. 36-pin SOJ pinout (Top View)



## Selection Guide

Description	-10	Unit
Maximum access time	10	ns
Maximum operating current	90	mA
Maximum CMOS standby current	10	mA

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient Temperature with Power Applied .....  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Supply Voltage on  $V_{\text{CC}}$  to Relative GND [2] .....  $-0.5\text{ V}$  to  $+6.0\text{ V}$

DC Voltage Applied to Outputs in High Z State [2] .....  $-0.5\text{ V}$  to  $V_{\text{CC}} + 0.5\text{ V}$

DC Input Voltage [2]	.....	$-0.5\text{ V}$ to $V_{\text{CC}} + 0.5\text{ V}$
Current into Outputs (LOW)	.....	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	.....	$>2001\text{ V}$
Latch-Up Current	.....	$>200\text{ mA}$

## Operating Range

Range	Ambient Temperature	$V_{\text{CC}}$
Industrial	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	4.5 V–5.5 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		<b>-10</b>		Unit
				Min	Max	
$V_{\text{OH}}$	Output HIGH Voltage	$V_{\text{CC}} = \text{Min}$	$I_{\text{OH}} = -4.0\text{ mA}$	2.4	–	V
		$V_{\text{CC}} = \text{Max}$	$I_{\text{OH}} = -0.1\text{ mA}$	–	3.4 [3]	
$V_{\text{OL}}$	Output LOW Voltage	$V_{\text{CC}} = \text{Min.}$ , $I_{\text{OL}} = 8.0\text{ mA}$		–	0.4	V
$V_{\text{IH}}^{[2]}$	Input HIGH Voltage			2.0	$V_{\text{CC}} + 0.5$	V
$V_{\text{IL}}^{[2]}$	Input LOW Voltage [2]			-0.5	0.8	V
$I_{\text{IX}}$	Input Leakage Current	$\text{GND} < V_{\text{I}} < V_{\text{CC}}$		-1	+1	$\mu\text{A}$
$I_{\text{OZ}}$	Output Leakage Current	$\text{GND} < V_{\text{OUT}} < V_{\text{CC}}$ , Output Disabled		-1	+1	$\mu\text{A}$
$I_{\text{CC}}$	VCC Operating Supply Current	$V_{\text{CC}} = \text{Max.}$ , $f = f_{\text{MAX}} = 1/t_{\text{RC}}$	100 MHz	–	90	mA
			–			
			83 MHz	–	80	mA
			–			
			66 MHz	–	70	mA
			–			
			40 MHz	–	60	mA
			–			
$I_{\text{SB1}}$	Automatic CE Power-Down Current – TTL Inputs	Max. $V_{\text{CC}}$ , $\text{CE} > V_{\text{IH}}$ , $V_{\text{IN}} > V_{\text{IH}}$ or $V_{\text{IN}} < V_{\text{IL}}$ , $f = f_{\text{MAX}}$		–	20	mA
$I_{\text{SB2}}$	Automatic CE Power-Down Current – CMOS Inputs	Max. $V_{\text{CC}}$ , $\text{CE} > V_{\text{CC}} - 0.3\text{ V}$ , $V_{\text{IN}} > V_{\text{CC}} - 0.3\text{ V}$ or $V_{\text{IN}} < 0.3\text{ V}$ , $f = 0$		–	10	mA

### Notes

2. Minimum voltage is  $-2.0\text{ V}$  and  $V_{\text{IH}}(\text{max}) = V_{\text{CC}} + 2\text{ V}$  for pulse durations of less than 20 ns.

3. Please note that the maximum  $V_{\text{OH}}$  limit does not exceed minimum CMOS  $V_{\text{IH}}$  of  $3.5\text{ V}$ . If you are interfacing this SRAM with 5 V legacy processors that require a minimum  $V_{\text{IH}}$  of  $3.5\text{ V}$ , please refer to Application Note [AN6081](#) for technical details and options you may consider.

## Capacitance

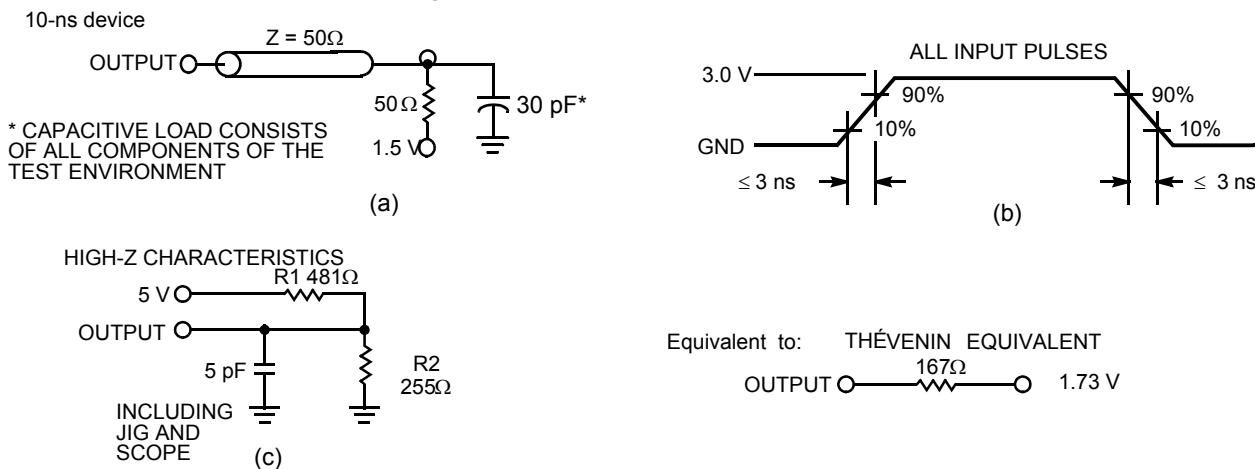
Parameter <sup>[4]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ C, f = 1 \text{ MHz}, V_{CC} = 5.0 \text{ V}$	8	pF
$C_{OUT}$	I/O capacitance		8	pF

## Thermal Resistance

Parameter <sup>[4]</sup>	Description	Test Conditions	SOJ Package	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.91	°C/W
$\Theta_{JC}$	Thermal resistance (junction to case)		36.73	°C/W

## AC Test Loads and Waveforms

**Figure 2. AC Test Loads and Waveforms** [5]



## Note

4. Tested initially and after any design or process changes that may affect these parameters.
5. AC characteristics (except High-Z) for 10-ns parts are tested using the load conditions shown in [Figure 2 \(a\)](#). High-Z characteristics are tested for all speeds using the test load shown in [Figure 2 \(c\)](#).

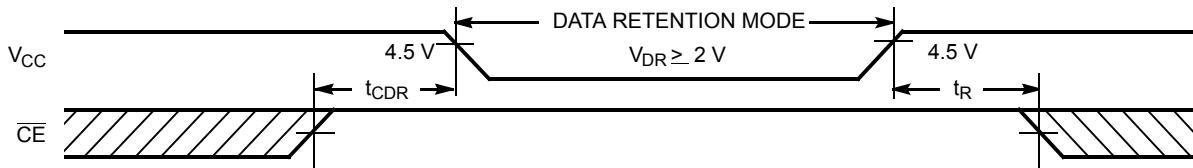
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions <sup>[6]</sup>	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0	–	V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ ,	–	10	mA
$t_{CDR}$ <sup>[7]</sup>	Chip Deselect to Data Retention Time		0	–	ns
$t_R$ <sup>[8]</sup>	Operation Recovery Time	$V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	$t_{RC}$	–	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

6. No input may exceed  $V_{CC} + 0.5\text{ V}$ .
7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\min.)} \geq 50\text{ }\mu\text{s}$  or stable at  $V_{CC(\min.)} \geq 50\text{ }\mu\text{s}$ .

## Switching Characteristics

Over the Operating Range

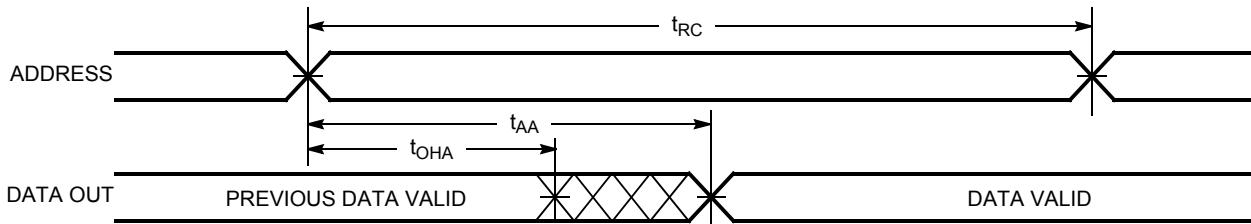
Parameter <sup>[9]</sup>	Description	-10		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{\text{power}}$	$V_{\text{CC}}$ (typical) to the First Access <sup>[10]</sup>	100	—	μs
$t_{\text{RC}}$	Read Cycle Time	10	—	ns
$t_{\text{AA}}$	Address to Data Valid	—	10	ns
$t_{\text{OHA}}$	Data Hold from Address Change	3	—	ns
$t_{\text{ACE}}$	$\overline{\text{CE}}$ LOW to Data Valid	—	10	ns
$t_{\text{DOE}}$	$\overline{\text{OE}}$ LOW to Data Valid	—	5	ns
$t_{\text{LZOE}}$	$\overline{\text{OE}}$ LOW to Low Z <sup>[11]</sup>	0	—	ns
$t_{\text{HZOE}}$	$\overline{\text{OE}}$ HIGH to High Z <sup>[11, 12]</sup>	—	5	ns
$t_{\text{LZCE}}$	$\overline{\text{CE}}$ LOW to Low Z <sup>[11]</sup>	3	—	ns
$t_{\text{HZCE}}$	$\overline{\text{CE}}$ HIGH to High Z <sup>[11, 12]</sup>	—	5	ns
$t_{\text{PU}}$	$\overline{\text{CE}}$ LOW to Power-Up	0	—	ns
$t_{\text{PD}}$	$\overline{\text{CE}}$ HIGH to Power-Down	—	10	ns
<b>Write Cycle</b> <sup>[13, 14]</sup>				
$t_{\text{WC}}$	Write Cycle Time	10	—	ns
$t_{\text{SCE}}$	$\overline{\text{CE}}$ LOW to Write End	7	—	ns
$t_{\text{AW}}$	Address Set-Up to Write End	7	—	ns
$t_{\text{HA}}$	Address Hold from Write End	0	—	ns
$t_{\text{SA}}$	Address Set-Up to Write Start	0	—	ns
$t_{\text{PWE}}$	$\overline{\text{WE}}$ Pulse Width	7	—	ns
$t_{\text{SD}}$	Data Set-Up to Write End	6	—	ns
$t_{\text{HD}}$	Data Hold from Write End	0	—	ns
$t_{\text{LZWE}}$	$\overline{\text{WE}}$ HIGH to Low Z <sup>[11]</sup>	3	—	ns
$t_{\text{HZWE}}$	$\overline{\text{WE}}$ LOW to High Z <sup>[11, 12]</sup>	—	5	ns

### Notes

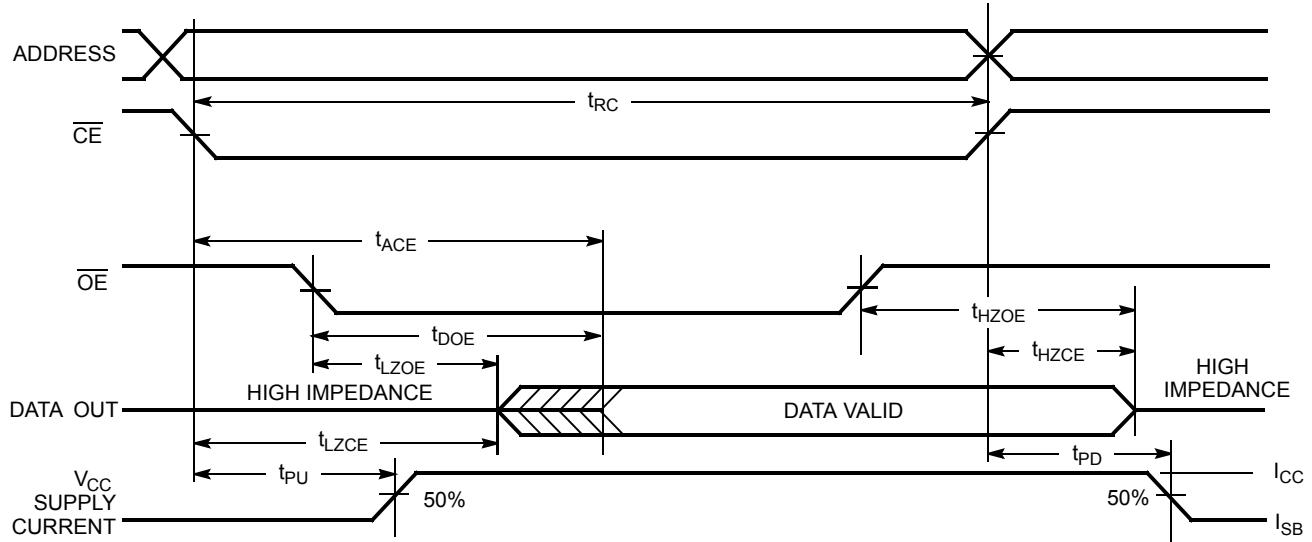
9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{\text{OL}}/I_{\text{OH}}$  and 30-pF load capacitance.
10.  $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at typical  $V_{\text{CC}}$  values until the first memory access can be performed.
11. At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.
12.  $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (c) of [Figure 2](#). Transition is measured when the outputs enter a high impedance state.
13. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
14. The minimum write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

## Switching Waveforms

**Figure 4. Read Cycle No. 1** [15, 16]



**Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [16, 17]



### Notes

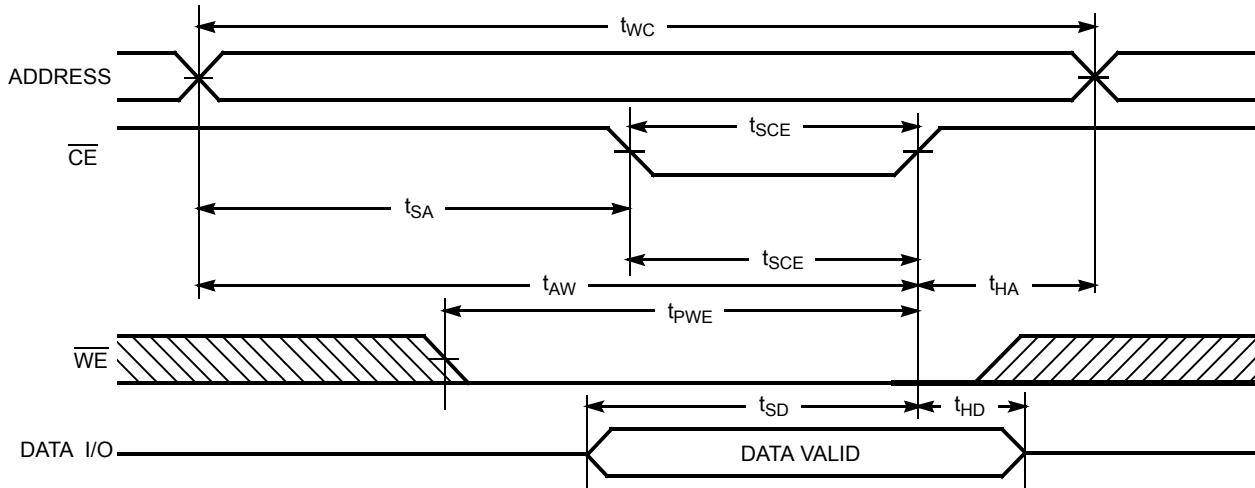
15. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ .

16.  $\overline{WE}$  is HIGH for read cycle.

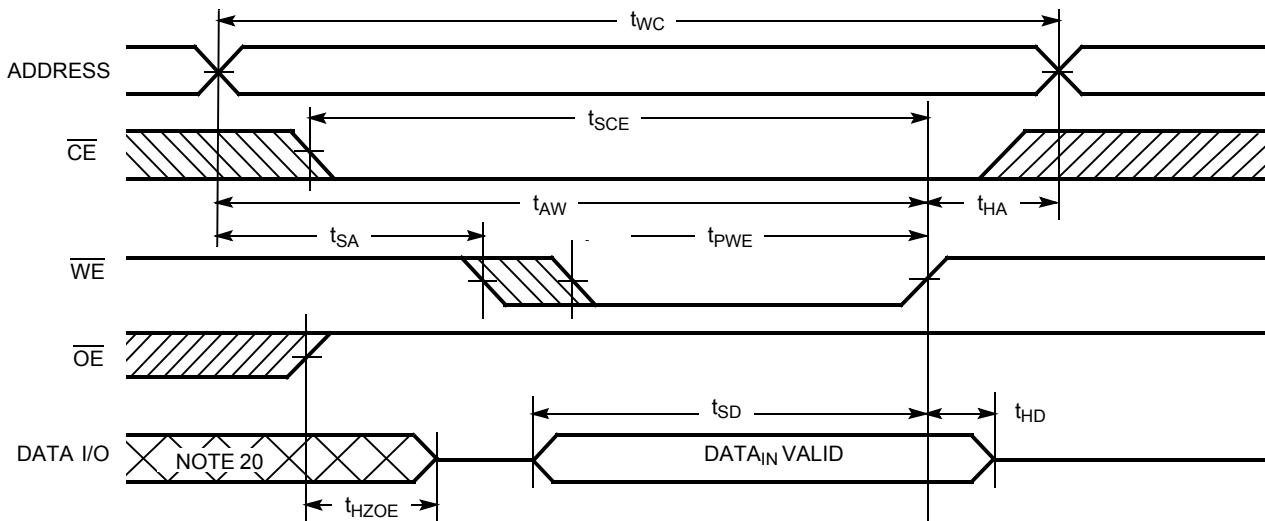
17. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

## Switching Waveforms(continued)

**Figure 6. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [18, 19]**



**Figure 7. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  HIGH During Write) [18, 19]**

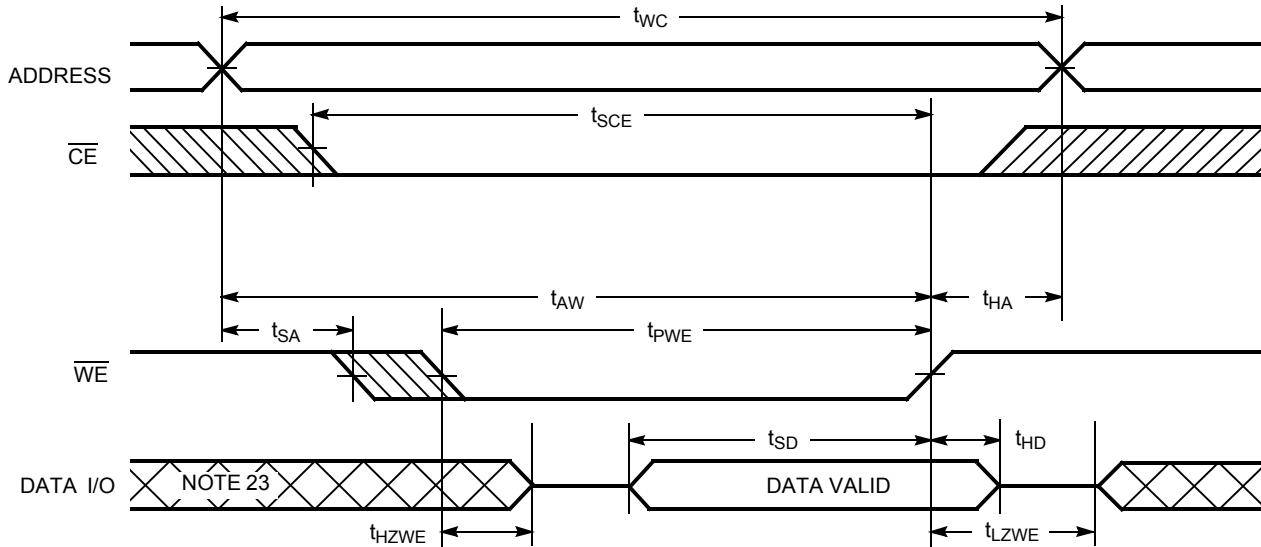


### Notes

18. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$
19. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.
20. During this period the I/Os are in the output state and input signals should not be applied.

## Switching Waveforms(continued)

**Figure 8. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) <sup>[21, 22]</sup>**



**Note**

21. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

22. The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

23. During this period the I/Os are in the output state and input signals should not be applied.

## Truth Table

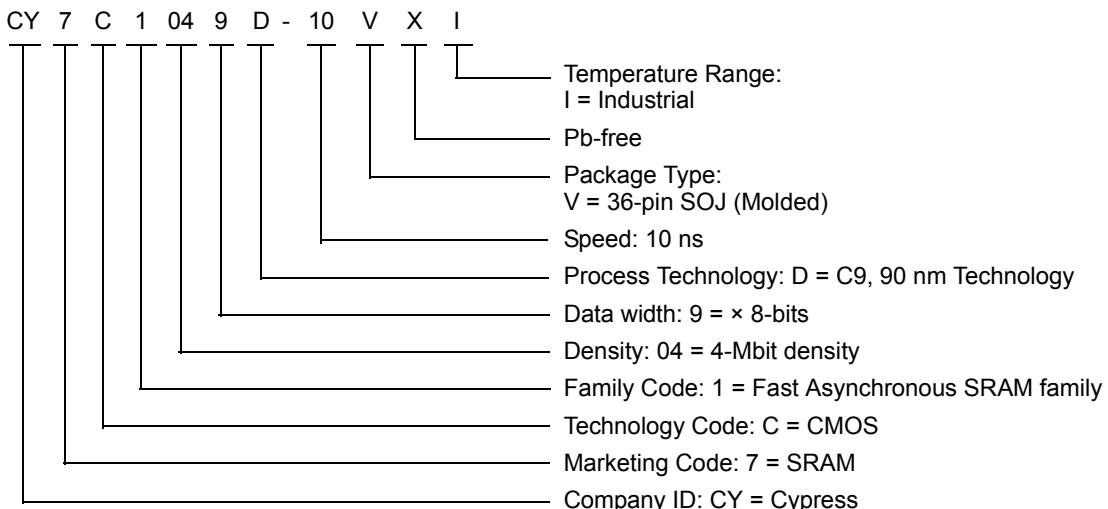
<b><math>\overline{CE}</math></b>	<b><math>\overline{OE}</math></b>	<b><math>\overline{WE}</math></b>	<b><math>I/O_0-I/O_7</math></b>	<b>Mode</b>	<b>Power</b>
H	X	X	High-Z	Power-down	Standby ( $I_{SB}$ )
L	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High-Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

## Ordering Information

<b>Speed (ns)</b>	<b>Ordering Code</b>	<b>Package Diagram</b>	<b>Package Type</b>	<b>Operating Range</b>
10	CY7C1049D-10VXI	51-85090	36-pin SOJ (Molded) Pb-free	Industrial

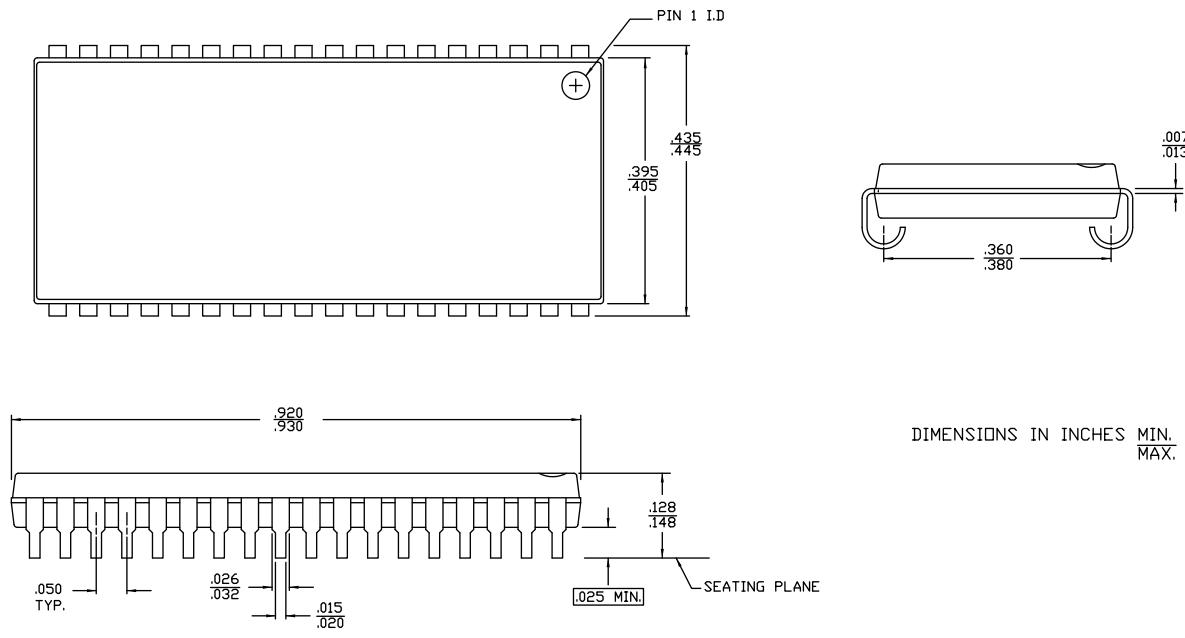
Please contact your local Cypress sales representative for availability of these parts.

## Ordering Code Definitions



## Package Diagram

Figure 9. 36-pin SOJ V36.4 (Molded) Package Outline, 51-85090



51-85090 \*F

## Acronyms

Acronym	Description
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
SOJ	Small Outline J-Lead
VFBGA	Very Fine-Pitch Ball Grid Array

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mV	millivolt
mW	milliwatt
ns	nanosecond
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1049D, 4-Mbit (512 K x 8) Static RAM Document Number: 38-05474				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	201560	SWI	See ECN	Advance Datasheet for C9 IPP
*A	233729	RKF	See ECN	1.AC, DC parameters are modified as per EROS(Spec # 01-2165) 2.Pb-free offering in the 'ordering information'
*B	351096	PCI	See ECN	Changed from Advance to Preliminary Removed 17, 20 ns Speed bin Added footnote # 4 Redefined $I_{CC}$ values for Com'l and Ind'l temperature ranges $I_{CC}$ (Com'l): Changed from 67 and 54 mA to 75 and 70 mA for 12 and 15 ns speed bins respectively $I_{CC}$ (Ind'l): Changed from 80, 67 and 54 mA to 90, 85 and 80 mA for 10, 12 and 15 ns speed bins respectively Added $V_{IH(max)}$ spec in Note# 2 Modified Note# 10 on $t_R$ Changed $t_{SCE}$ from 8 to 7 ns for 10 ns speed bin Changed reference voltage level for measurement of Hi-Z parameters from $\pm 500$ mV to $\pm 200$ mV Added Truth Table on page# 6 Removed L-Version Added 10 ns parts in the Ordering Information Table Added Lead-Free Product Information Shaded Ordering Information Table
*C	446328	NXR	See ECN	Converted from Preliminary to Final Removed -12 and -15 speed bins Removed Commercial Operating Range product information Changed Maximum Rating for supply voltage from 7 V to 6 V Updated Thermal Resistance table Changed $t_{HZWE}$ from 6 ns to 5 ns Updated footnote #7 on High-Z parameter measurement Replaced Package Name column with Package Diagram in the Ordering Information table
*D	3109184	AJU	12/13/2010	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagram</a> .
*E	3235742	PRAS	04/20/2011	Added Acronyms and Units of measure. Updated template.
*F	4040855	MEMJ	06/26/2013	Updated <a href="#">Functional Description</a> . Updated <a href="#">Electrical Characteristics</a> : Added one more Test Condition " $V_{CC} = \text{Max}$ , $I_{OH} = -0.1\text{mA}$ " for $V_{OH}$ parameter and added maximum value corresponding to that Test Condition. Added Note 3 and referred the same note in maximum value for $V_{OH}$ parameter corresponding to Test Condition " $V_{CC} = \text{Max}$ , $I_{OH} = -0.1\text{mA}$ ". Updated <a href="#">Package Diagram</a> : spec 51-85090 – Changed revision from *E to *F. Updated in new template.
*G	4391976	MEMJ	05/28/2014	Updated <a href="#">Switching Waveforms</a> : Added Note 22 and referred the same note in <a href="#">Figure 8</a> . Completing Sunset Review.
*H	4578500	MEMJ	11/24/2014	Added related documentation hyperlink in page 1.

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