

8-Stage Shift/Store Register with Three-State Outputs

The MC14094B combines an 8-stage shift register with a data latch for each stage and a three-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q_S output data is for use in high-speed cascaded systems. The Q'_S output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by three-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

- Three-State Outputs
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Pin-for-Pin Compatible with CD4094B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	- 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

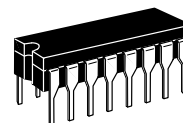
Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q_1	Q_N	Q_S^*	Q'_S
	0	X	X	Z	Z	Q_7	No Chg.
	0	X	X	Z	Z	No Chg.	Q_7
	1	0	X	No Chg.	No Chg.	Q_7	No Chg.
	1	1	0	0	Q_N-1	Q_7	No Chg.
	1	1	1	1	Q_N-1	Q_7	No Chg.
	1	1	1	No Chg.	No Chg.	No Chg.	Q_7

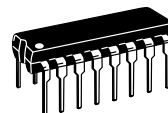
Z = High Impedance X = Don't Care

* At the positive clock edge, information in the 7th shift register stage is transferred to Q_8 and Q_S .

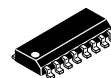
MC14094B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.

PIN ASSIGNMENT

STROBE	1	16	V_{DD}
DATA	2	15	OUTPUT ENABLE
CLOCK	3	14	Q_5
Q_1	4	13	Q_6
Q_2	5	12	Q_7
Q_3	6	11	Q_8
Q_4	7	10	Q'_S
V_{SS}	8	9	Q_S

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V _{in} = 0 or V _{DD}	V _{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	I _{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I _{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (4.1 μA/kHz) f + I _{DD} I _T = (14 μA/kHz) f + I _{DD} I _T = (140 μA/kHz) f + I _{DD}							μAdc
3–State Output Leakage Current	I _{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	μA

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

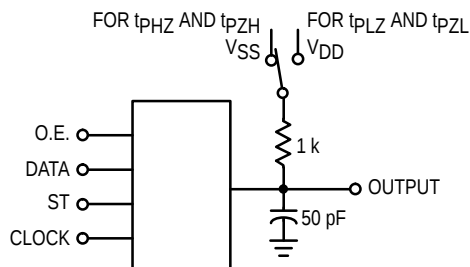
where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

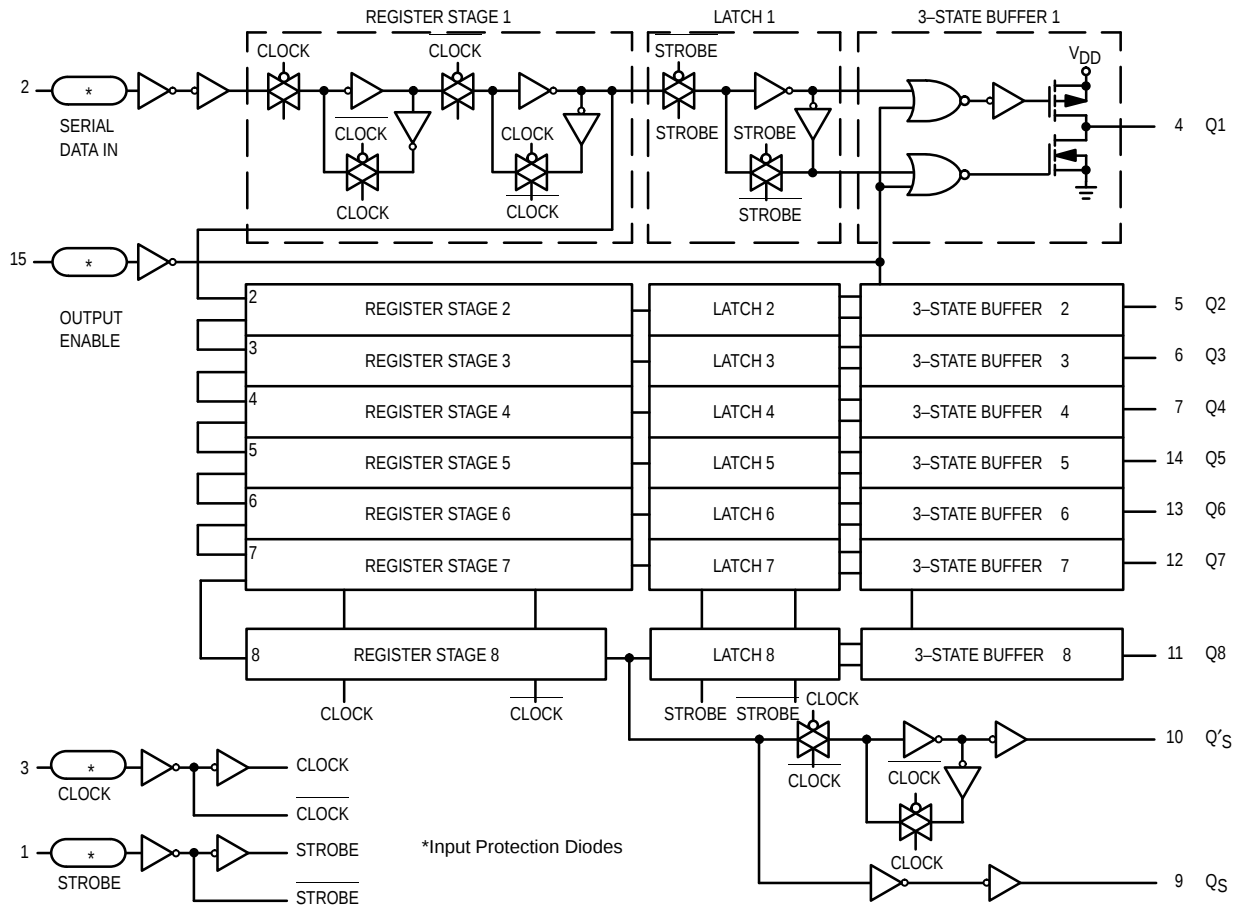
Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH}, t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}, t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH},$ t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Serial out QS $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 305 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 82 \text{ ns}$ Clock to Serial out Q'S $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 350 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 149 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 62 \text{ ns}$ Clock to Parallel out $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 375 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.35 \text{ ns/pF}) C_L + 177 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 122 \text{ ns}$ Strobe to Parallel out $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 245 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 127 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	— — —	350 125 95	600 250 190	ns
Output Enable to Output $t_{PHZ}, t_{PZL} = (0.90 \text{ ns/pF}) C_L + 95 \text{ ns}$ $t_{PHZ}, t_{PZL} = (0.36 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PHZ}, t_{PZL} = (0.26 \text{ ns/pF}) C_L + 42 \text{ ns}$	$t_{PHZ},$ t_{PZL}	5.0 10 15	— — —	140 75 55	280 150 110	
Output Disable to Output $t_{PLZ}, t_{PZH} = (0.90 \text{ ns/pF}) C_L + 180 \text{ ns}$ $t_{PLZ}, t_{PZH} = (0.36 \text{ ns/pF}) C_L + 77 \text{ ns}$ $t_{PLZ}, t_{PZH} = (0.26 \text{ ns/pF}) C_L + 57 \text{ ns}$	$t_{PLZ},$ t_{PZH}	5.0 10 15	— — —	225 95 70	450 190 140	
Setup Time Data in to Clock	t_{su}	5.0 10 15	125 55 35	60 30 20	— — —	ns
Hold Time Clock to Data	t_h	5.0 10 15	0 20 20	– 40 – 10 0	— — —	ns
Clock Pulse Width, High	t_{WH}	5.0 10 15	200 100 83	100 50 40	— — —	ns
Clock Rise and Fall Time	$t_{r(cl)}$ $t_{f(cl)}$	5 10 15	— — —	— — —	15 5.0 4.0	μs
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	2.5 5.0 6.0	1.25 2.5 3.0	MHz
Strobe Pulse Width	t_{WL}	5.0 10 15	200 80 70	100 40 35	— — —	ns

* The formulas given are for the typical characteristics only at 25°C .

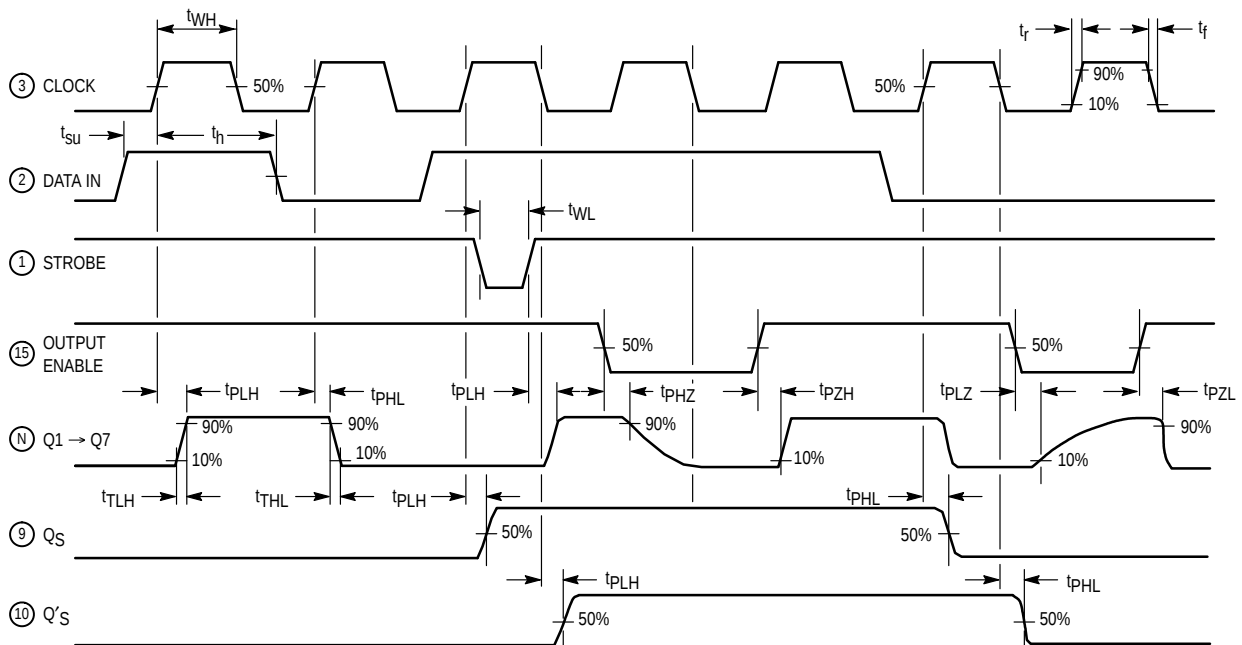
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3-STATE TEST CIRCUIT


BLOCK DIAGRAM

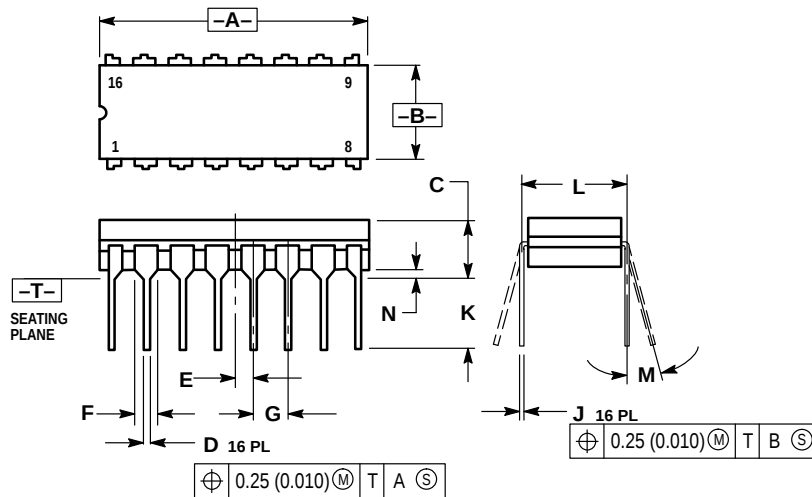


DYNAMIC TIMING DIAGRAM



OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

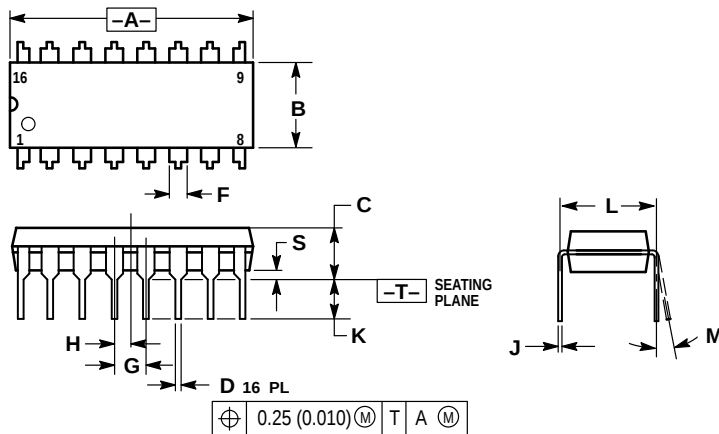


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050	BSC	1.27	BSC
F	0.055	0.065	1.40	1.65
G	0.100	BSC	2.54	BSC
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300	BSC	7.62	BSC
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



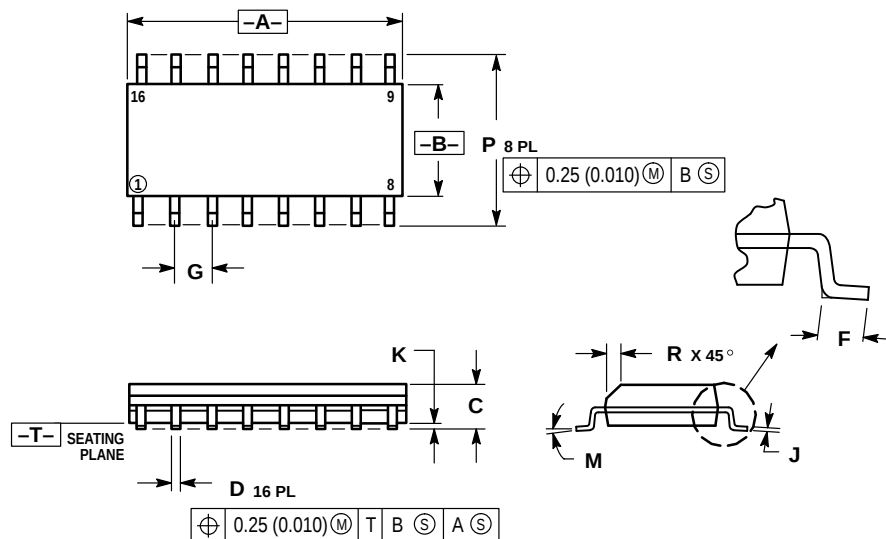
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
H	0.050	BSC	1.27	BSC
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
INTERNET: <http://Design-NET.com>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



MOTOROLA



MC14094B/D

