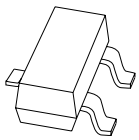


ON5520

N-channel TrenchMOS FET

Rev. 01 — 24 March 2009 Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using TrenchMOS technology.

This type is a selection of the 2N7002 by the parameter $V_{GS(th)}$.

1.2 Features

- Logic level threshold compatible
- Surface-mounted package
- Very fast switching
- TrenchMOS technology

1.3 Applications

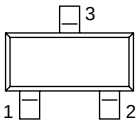
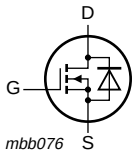
- Logic level translator
- High-speed line driver

1.4 Quick reference data

- $V_{DS} \leq 60$ V
- $R_{DSon} \leq 5\ \Omega$
- $I_D \leq 300$ mA
- $P_{tot} \leq 0.83$ W

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	gate (G)		
2	source (S)		
3	drain (D)		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
ON5520	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

4. Marking

Table 3. Marking codes

Type number	Marking code[1]
ON5520	RN*

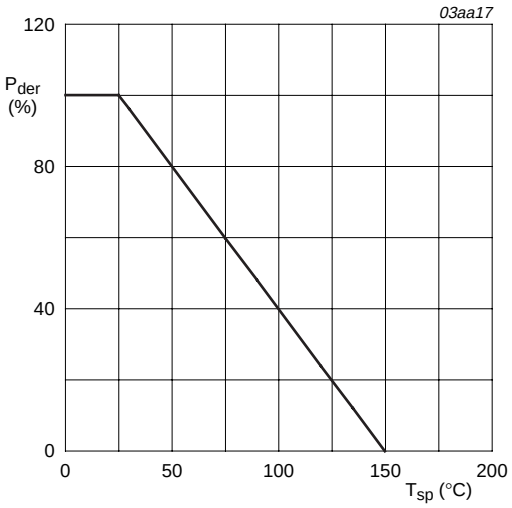
[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 4. Limiting values

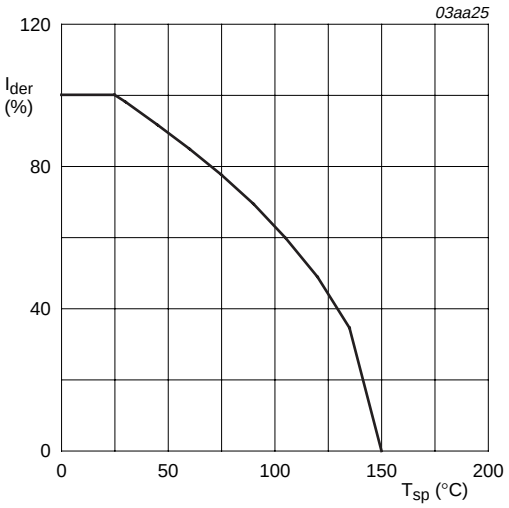
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C	-	60	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	60	V
V_{GS}	gate-source voltage		-	±30	V
V_{GSM}	peak gate-source voltage	t_p ≤ 50 µs; pulsed; duty cycle = 25 %	-	±40	V
I_D	drain current	T_{sp} = 25 °C; V_{GS} = 10 V; see Figure 2 and 3	-	300	mA
		T_{sp} = 100 °C; V_{GS} = 10 V; see Figure 2	-	190	mA
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs; see Figure 3	-	1.2	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; see Figure 1	-	0.83	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current	T_{sp} = 25 °C	-	300	mA
I_{SM}	peak source current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs	-	1.2	A



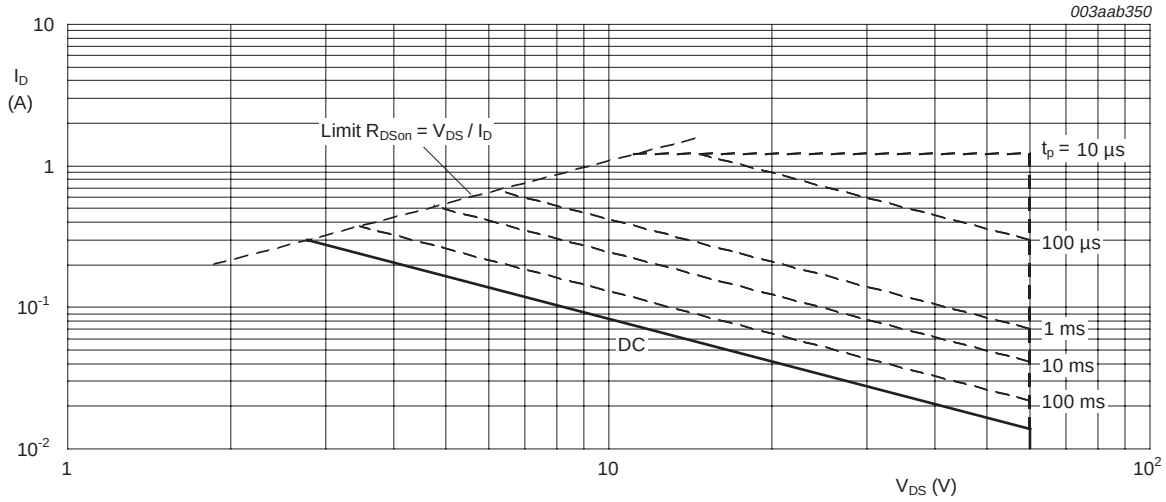
$$P_{der} = \frac{P_{tot}}{P_{tot(25\ ^\circ C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25\ ^\circ C)}} \times 100\ \%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4		-	-	150	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	-	350	K/W

[1] Mounted on a Printed-Circuit Board (PCB); minimum footprint; vertical in still air.

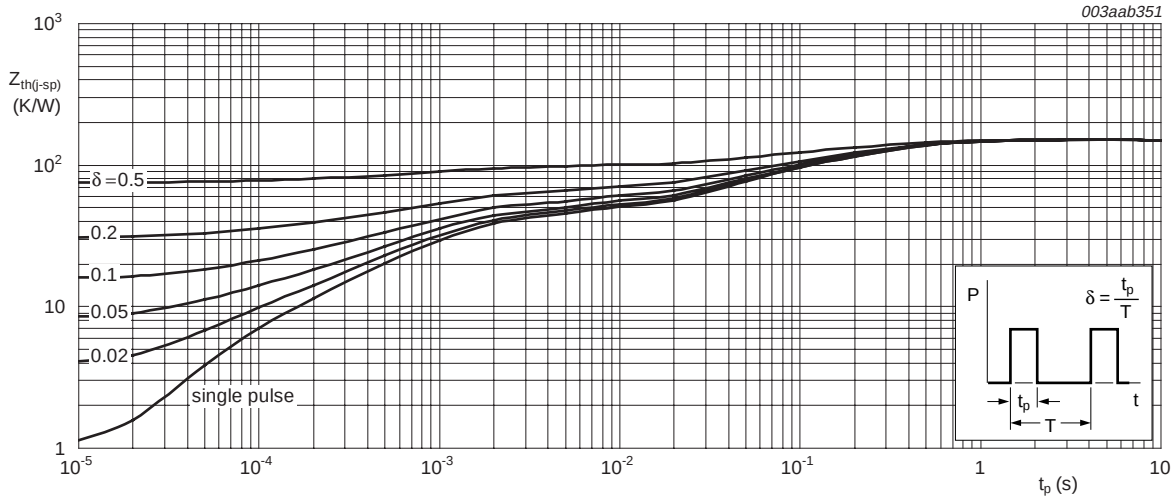


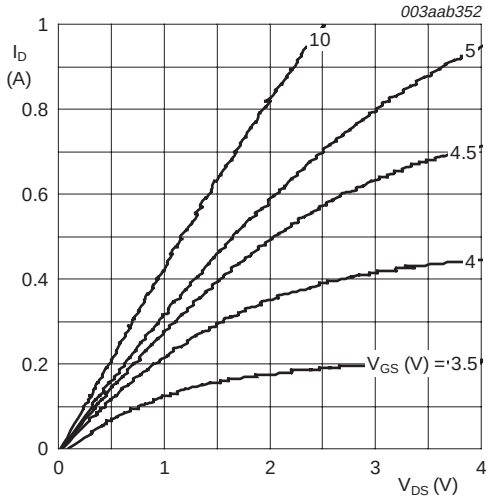
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

7. Characteristics

Table 6. Characteristics

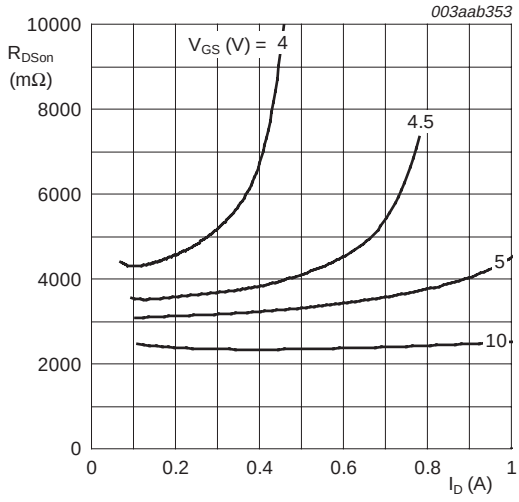
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0 V				
		T_j = 25 °C	60	-	-	V
		T_j = –55 °C	55	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 0.25 mA; V_{DS} = V_{GS}; see Figure 9 and 10				
		T_j = 25 °C	1.6	2	2.1	V
		T_j = 150 °C	0.6	-	-	V
		T_j = –55 °C	-	-	2.75	V
I_{DSS}	drain leakage current	V_{DS} = 48 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.01	1	µA
		T_j = 150 °C	-	-	10	µA
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 500 mA; see Figure 6 and 8				
		T_j = 25 °C	-	2.8	5	Ω
		T_j = 150 °C	-	-	9.25	Ω
		V_{GS} = 4.5 V; I_D = 75 mA; see Figure 6 and 8	-	3.8	5.3	Ω
Dynamic characteristics						
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 10 V; f = 1 MHz; see Figure 12	-	31	50	pF
C_{oss}	output capacitance		-	6.8	30	pF
C_{rss}	reverse transfer capacitance		-	3.5	10	pF
t_{on}	turn-on time	V_{DS} = 50 V; R_L = 250 Ω; V_{GS} = 10 V; R_G = 50 Ω; R_{GS} = 50 Ω	-	2.5	10	ns
t_{off}	turn-off time		-	11	15	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 300 mA; V_{GS} = 0 V; see Figure 11	-	0.85	1.5	V
t_{rr}	reverse recovery time	I_S = 300 mA; dI_S/dt = –100 A/µs; V_{GS} = 0 V	-	30	-	ns
Q_r	recovered charge		-	30	-	nC



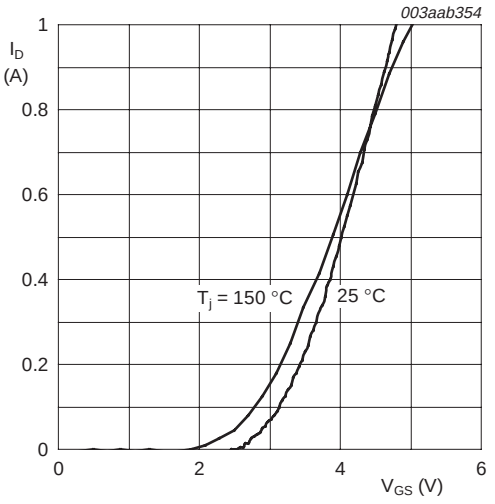
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



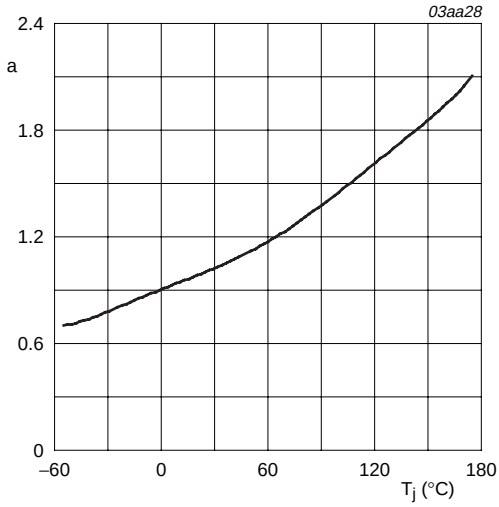
T_j = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



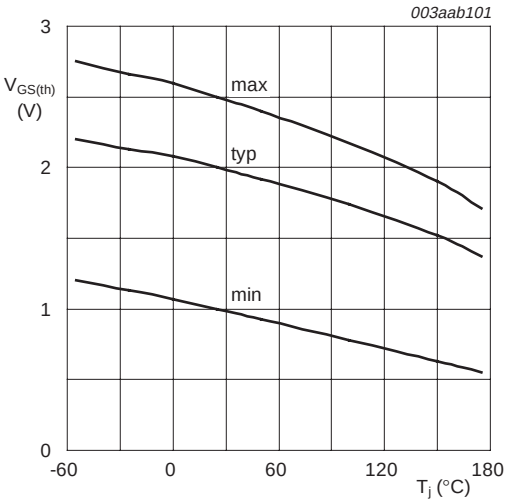
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



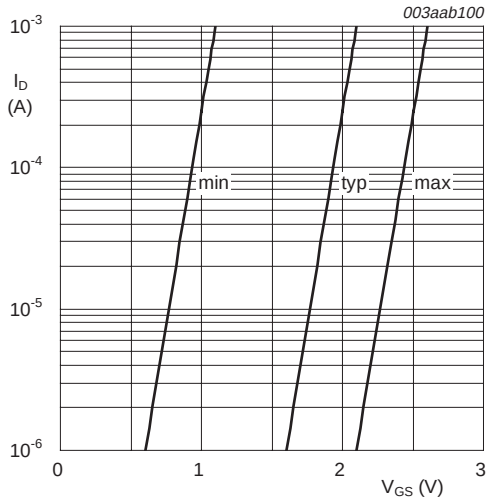
$$a = \frac{R_{DSon}}{R_{DSon(25\ ^\circ C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



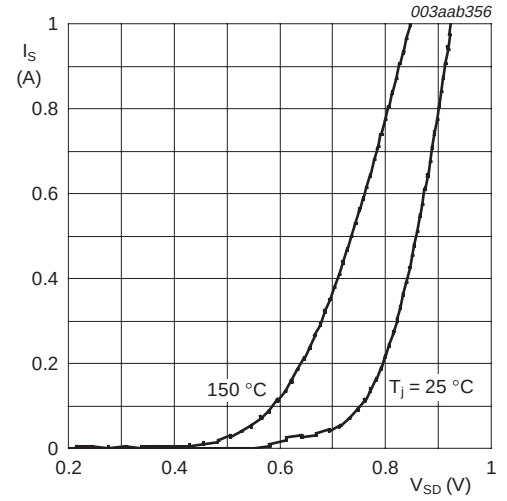
I_D = 0.25 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature



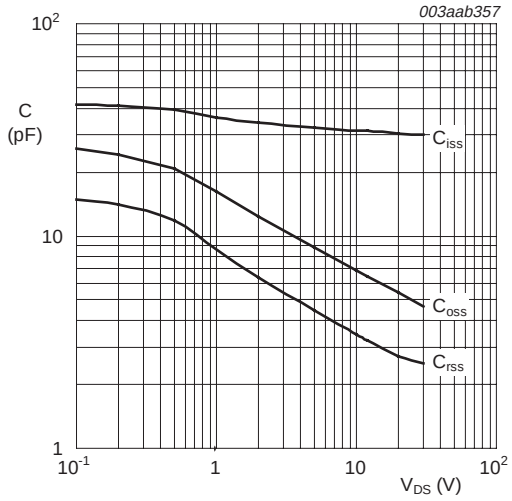
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 11. Source current as a function of source-drain voltage; typical values

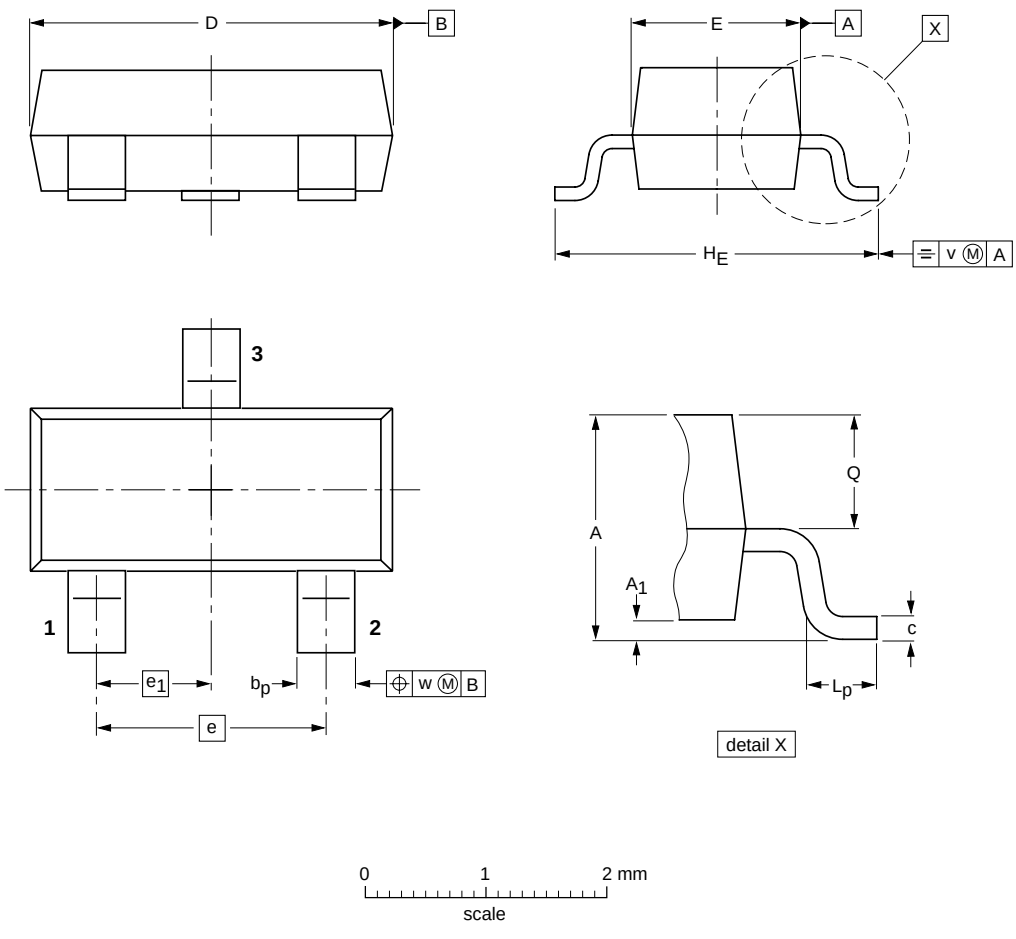


V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

8. Package outline

Plastic surface-mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				~~04-11-04~~ 06-03-16

Fig 13. Package outline SOT23

9. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ON5520_1	20090324	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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12. Contents

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