

## POWER MANAGEMENT

### 3.3V $\mu$ P Power Supply Monitor and Reset Circuit

- Selectable Trip-Point Tolerance and Watchdog Period
- Push-Button Reset
- Push-Pull Reset Outputs

The IMP1832 microprocessor supervisor can halt and restart a “hung-up” or “stalled” microprocessor, restart a microprocessor after a power failure, and debounce a manual push-button microprocessor reset switch. The IMP1832 features over 40% lower supply current than the pin compatible Dallas Semiconductor DS1832.

Precision temperature compensated reference and comparator circuits monitor the 3.3V,  $V_{CC}$  input voltage. During power-up or when the  $V_{CC}$  power supply falls outside selectable tolerance limits, both  $\overline{\text{RESET}}$  and  $\text{RESET}$  become active. When  $V_{CC}$  rises above the threshold voltage, the reset signals remain active for an additional 250ms minimum, allowing the power supply and system microprocessor to stabilize. The trip point tolerance signal, TOL, selects the trip level tolerance to be either 10- or 20-percent.

$\overline{\text{RESET}}$  and  $\text{RESET}$  outputs are push-pull.

A debounced manual reset input,  $\overline{\text{PBRST}}$ , activates the reset outputs for a minimum period of 250ms.

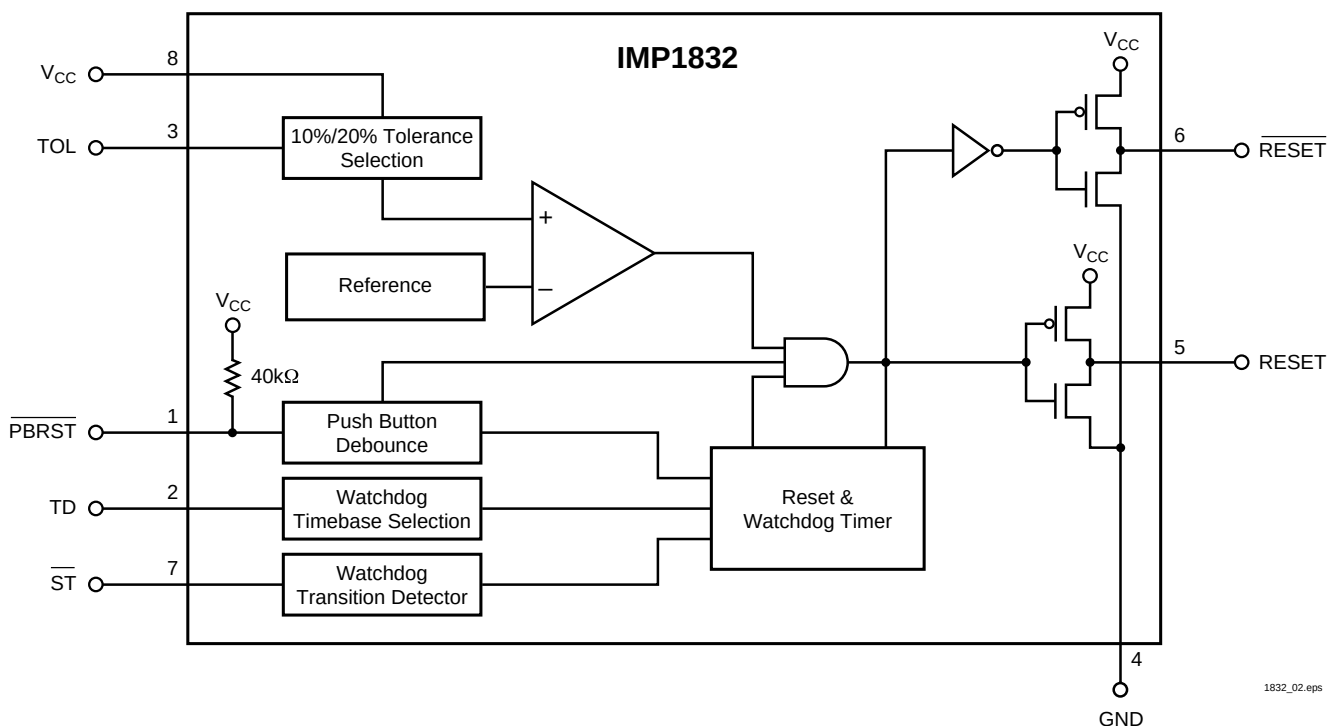
### Key Features

- ◆ Pin compatible with the Dallas Semiconductor DS1832
  - Over 40% lower supply current
- ◆ 3.3V supply monitor
- ◆ Push-pull output
- ◆ Selectable watchdog period
- ◆ Debounce manual push-button reset input
- ◆ Precision temperature-compensated voltage reference and comparator
- ◆ Power-up, power-down and brownout detection
- ◆ 250ms minimum reset time
- ◆ Active LOW and HIGH reset signal
- ◆ Selectable trip point tolerance: 10% or 20%
- ◆ Low-cost 8-pin DIP/SO and 8-pin MicroSO packages
- ◆ Wide operating temperature  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Also included is a watchdog timer to stop and restart a microprocessor that is “hung-up”. Three watchdog time-out periods are selectable: 150ms, 610ms and 1,200ms. If the  $\overline{\text{ST}}$  input is not strobed LOW before the time-out period expires, a reset is issued.

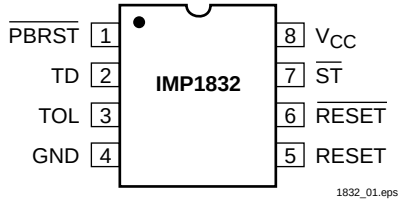
Devices are available in 8-pin DIP, 8-pin SO and compact 8-pin MicroSO packages.

### Block Diagram



## Pin Configuration

### DIP/SO/MicroSO



## Pin Descriptions

| Pin Number<br>8-Pin Package | Name     | Function                                                                                                                                                                                                                                                                                                     |
|-----------------------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                           | PBRST    | Debounced manual pushbutton reset input                                                                                                                                                                                                                                                                      |
| 2                           | TD       | Watchdog time delay selection. ( $t_{TD} = 150ms$ for TD = GND, $t_{TD} = 610ms$ for TD = Open, and $t_{TD} = 1200ms$ for TD = $V_{CC}$ )                                                                                                                                                                    |
| 3                           | TOL      | Selects 10% (TOL connected to GND) or 20% (TOL connected to $V_{CC}$ ) trip point tolerance                                                                                                                                                                                                                  |
| 4                           | GND      | Ground                                                                                                                                                                                                                                                                                                       |
| 5                           | RESET    | Active HIGH reset output. RESET is active: <ul style="list-style-type: none"> <li>1. If <math>V_{CC}</math> falls below the reset voltage trip point.</li> <li>2. If PBRST is LOW.</li> <li>3. If ST is not strobed LOW before the timeout period set by TD expires.</li> <li>4. During power-up.</li> </ul> |
| 6                           | RESET    | Active LOW reset output. (See RESET)                                                                                                                                                                                                                                                                         |
| 7                           | ST       | Strobe Input                                                                                                                                                                                                                                                                                                 |
| 8                           | $V_{CC}$ | 5V power                                                                                                                                                                                                                                                                                                     |

## Ordering Information

| Part Number | Package   | Operating Temperature Range | Maximum Supply Current ( $\mu A$ ) | Voltage Monitoring Application |
|-------------|-----------|-----------------------------|------------------------------------|--------------------------------|
| IMP1832     | 8-DIP     | -40°C to 85°C               | 20                                 | 3.3V                           |
| IMP1832S    | 8-SO      | -40°C to 85°C               | 20                                 | 3.3V                           |
| IMP1832SEMA | 8-MicroSO | -40°C to 85°C               | 20                                 | 3.3V                           |

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## Absolute Maximum Ratings

Voltage on  $\overline{V_{CC}}$  ..... -0.5V to 7V  
 Voltage on  $\overline{ST}$ ,  $\overline{TD}$  ..... -0.5V to  $V_{CC} + 0.5V$   
 Voltage on  $\overline{PBRST}$ ,  $\overline{RESET}$ ,  $\overline{RESET}$  ..... -0.5V to  $V_{CC} + 0.5V$   
 Operating Temperature Range ..... -40°C to 85°C

Soldering Temperature ..... 260°C for 10 seconds  
 Storage Temperature ..... -55°C to 125°C

*Voltages measured with respect to ground.*

*These are stress ratings only and functional operation is not implied.*

## Electrical Characteristics

Unless otherwise stated,  $1.2V \leq V_{CC} \leq 5.5V$  and over the operating temperature range of -40°C to +85°C. All voltages are referenced to ground.

| Parameter                                                                            | Symbol     | Conditions                                                            | Min             | Typ             | Max             | Units      |
|--------------------------------------------------------------------------------------|------------|-----------------------------------------------------------------------|-----------------|-----------------|-----------------|------------|
| Supply Voltage ( $V_{CC}$ )                                                          | $V_{CC}$   |                                                                       | 1.0             |                 | 5.5             | V          |
| $\overline{ST}$ and $\overline{PBRST}$ Input High Level                              | $V_{IH}$   | $V_{CC} \geq 2.7V$                                                    | 2               |                 | $V_{CC} + 0.3V$ | V          |
| $\overline{ST}$ and $\overline{PBRST}$ Input High Level                              | $V_{IH}$   | $V_{CC} < 2.7V$                                                       | $V_{CC} - 0.4V$ |                 |                 | V          |
| $\overline{ST}$ and $\overline{PBRST}$ Input Low Level                               | $V_{IL}$   |                                                                       | -0.3            |                 | 0.5             | V          |
| $V_{CC}$ Trip Point (TOL = GND)                                                      | $V_{CCTP}$ |                                                                       | 2.80            | 2.88            | 2.97            | V          |
| $V_{CC}$ Trip Point (TOL = $V_{CC}$ )                                                | $V_{CCTP}$ |                                                                       | 2.47            | 2.55            | 2.64            | V          |
| Watchdog Time-Out Period                                                             | $t_{TD}$   | $TD = GND$                                                            | 62.5            | 150             | 250             | ms         |
| Watchdog Time-Out Period                                                             | $t_{TD}$   | $TD = V_{CC}$                                                         | 500             | 1200            | 2000            | ms         |
| Watchdog Time-Out Period                                                             | $t_{TD}$   | $TD$ floating                                                         | 250             | 610             | 1000            | ms         |
| Output Voltage                                                                       | $V_{OH}$   | $I = -500\mu A$ , $V_{CC} < 2.7V$                                     | $V_{CC} - 0.3V$ | $V_{CC} - 0.1V$ |                 | V          |
| Output Current                                                                       | $I_{OH}$   | Output = 2.4V, $V_{CC} \geq 2.7V$                                     |                 | 350             |                 | $\mu A$    |
| Output Current                                                                       | $I_{OL}$   | Output = 0.4V, $V_{CC} \geq 2.7V$                                     | 10              |                 |                 | mA         |
| Input Leakage                                                                        | $I_{IL}$   |                                                                       | -1.0            |                 | 1.0             | $\mu A$    |
| $\overline{RESET}$ Low Level                                                         | $V_{OL}$   |                                                                       |                 |                 | 0.4             | V          |
| Internal Pull-Up Resistor                                                            |            | $\overline{PBRST}$ pin                                                |                 | 40              |                 | k $\Omega$ |
| Operating Current                                                                    | $I_{CC1}$  | Outputs open. $V_{CC} \leq 3.6V$<br>and all inputs at $V_{CC}$ or GND |                 |                 | 20              | $\mu A$    |
| Input Capacitance                                                                    | $C_{IN}$   |                                                                       |                 |                 | 5               | pF         |
| Output Capacitance                                                                   | $C_{OUT}$  |                                                                       |                 |                 | 7               | pF         |
| $\overline{PBRST}$ Manual Reset<br>Minimum Low Time                                  | $t_{PB}$   | $\overline{PBRST} = V_{IL}$                                           | 20              |                 |                 | ms         |
| Reset Active Time                                                                    | $t_{RST}$  |                                                                       | 250             | 610             | 1000            | ms         |
| $\overline{ST}$ Pulse Width                                                          | $t_{ST}$   | Must not exceed $t_{RD}$ minimum.<br>Watchdog cannot be disabled.     | 20              |                 |                 | ns         |
| $V_{CC}$ Fail Detect to<br>$\overline{RESET}$ or $\overline{RESET}$                  | $t_{RPD}$  | Pulses < 2 $\mu s$ at $V_{CCTP}$<br>minimum will not cause reset.     |                 | 5               | 8               | $\mu s$    |
| $V_{CC}$ Slew Rate                                                                   | $t_F$      |                                                                       | 20              |                 |                 | $\mu s$    |
| $\overline{PBRST}$ Stable LOW to<br>$\overline{RESET}$ and $\overline{RESET}$ Active | $t_{PDLY}$ |                                                                       |                 |                 | 20              | ms         |
| $V_{CC}$ Detect to $\overline{RESET}$ or<br>$\overline{RESET}$ Inactive              | $t_{RPU}$  | $t_{rise} = 5\mu s$                                                   | 250             | 610             | 1000            | ms         |
| $V_{CC}$ Slew Rate                                                                   | $t_R$      |                                                                       | 0               |                 |                 | ns         |

## Application Information

### Supply Voltage Monitor

The IMP1832 monitors the microprocessor or microcontroller power supply and issues reset signals, both active HIGH and active LOW, that halt processor operation whenever the power supply voltage levels are outside a predetermined tolerance.

Tolerance levels are set with the TOL pin.

RESET and  $\overline{\text{RESET}}$  signals are generated at the last moment of a valid  $V_{CC}$  signal. On power-up, both reset signals are active for a minimum of 250ms after the supply has returned to intolerance level. This allows the power supply and monitored processor to stabilize before instruction execution is allowed to begin.

### Trip Point Tolerance Selection

With TOL connected to  $V_{CC}$ , RESET and  $\overline{\text{RESET}}$  become active whenever  $V_{CC}$  falls below 2.64V. RESET and  $\overline{\text{RESET}}$  become active when  $V_{CC}$  falls below 2.98V if TOL is connected to ground.

After  $V_{CC}$  has risen above the trip point set by TOL, RESET and  $\overline{\text{RESET}}$  remain active for a minimum time period of 250ms.

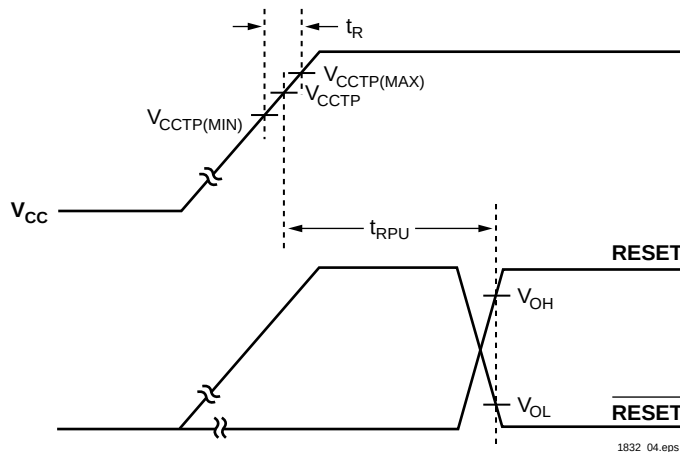


Figure 1. Timing Diagram: Power Up

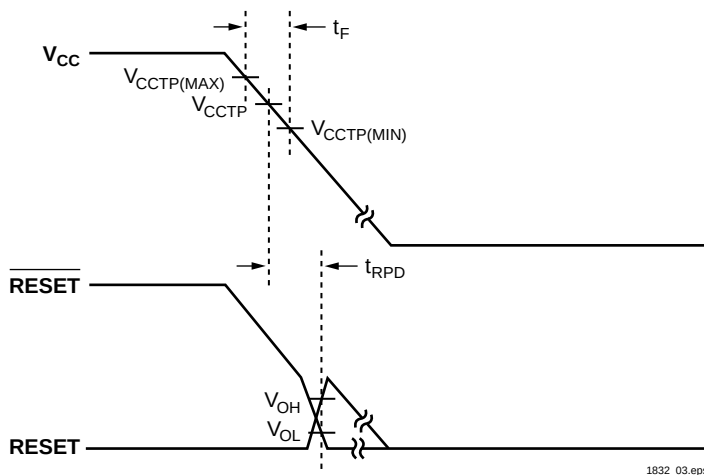


Figure 2. Timing Diagram: Power Down

On power-down, once  $V_{CC}$  falls below the reset threshold RESET stays LOW and is guaranteed to be 0.4V or less until  $V_{CC}$  drops below 1.2V. The active HIGH reset signal is valid down to a  $V_{CC}$  level of 1.2V also.

| Tolerance Select | Tolerance | TRIP Point Voltage (V) |         |      |
|------------------|-----------|------------------------|---------|------|
|                  |           | Min                    | Nominal | Max  |
| TOL = $V_{CC}$   | 20%       | 2.47                   | 2.55    | 2.64 |
| TOL = GND        | 10%       | 2.80                   | 2.88    | 2.97 |

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### Manual Reset Operation

Push-button switch input,  $\overline{\text{PBRST}}$ , allows the user to override the internal trip point detection circuits and issue reset signals. The pushbutton input is debounced and is pulled HIGH through an internal 40k $\Omega$  resistor.

When  $\overline{\text{PBRST}}$  is held LOW for the minimum time  $t_{PB}$ , both resets become active and remain active for a minimum time period of 250ms after  $\overline{\text{PBRST}}$  returns HIGH.

The debounced input is guaranteed to recognize pulses greater than 20ms. No external pull-up resistor is required, since  $\overline{\text{PBRST}}$  is pulled HIGH by an internal 40k $\Omega$  resistor.

The  $\overline{\text{PBRST}}$  can be driven from a TTL or CMOS logic line or shorted to ground with a mechanical switch.

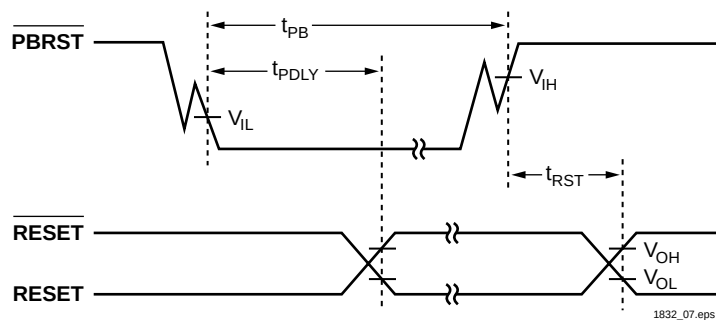


Figure 3. Timing Diagram: Pushbutton Reset

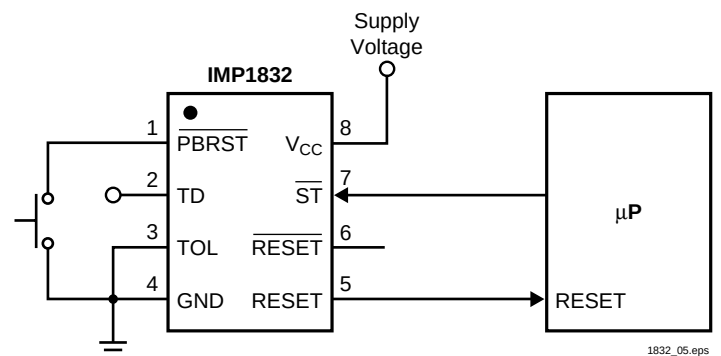


Figure 4. Application Circuit: Pushbutton Reset

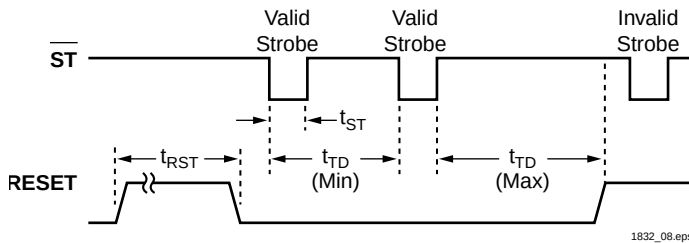
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## Application Information

### Watchdog Timer and $\overline{ST}$ Input

A watchdog timer stops and restarts a microprocessor that is “hung-up”. Through the time delay input, TD, three watchdog time-out periods are selectable: 150ms, 610ms and 1,200ms. If the strobe input,  $\overline{ST}$ , is not strobed LOW prior to timeout, reset signals become active. On power-up or after the supply voltage returns to an in-tolerance condition, the reset signal remains active for 250ms minimum, allowing the power supply and system micro-processor to stabilize.

$\overline{ST}$  Pulses as short as 20ns can be detected.



Note:  $\overline{ST}$  is ignored whenever a reset is active.

**Figure 5. Timing Diagram: Strobe Input**

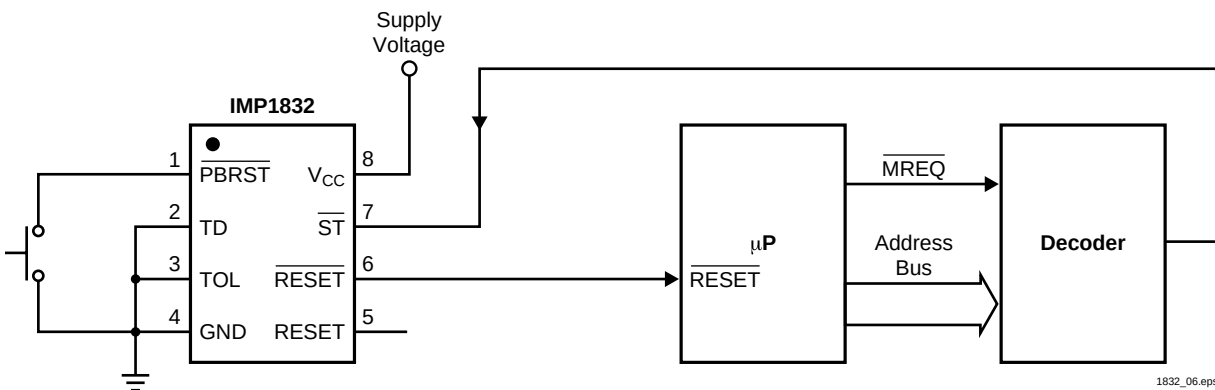
A HIGH-to-LOW  $\overline{ST}$  signal transition must be regularly issued no later than the minimum time-out period defined by the state of the TD signal. This guarantees the watchdog timer does not time-out.

Timeouts periods of approximately 150ms, 610ms or 1,200ms are selected through the TD pin.

| TD Voltage Level | Watchdog Time-Out Period (ms) |         |      |
|------------------|-------------------------------|---------|------|
|                  | Min                           | Nominal | Max  |
| GND              | 62.5                          | 150     | 250  |
| Floating         | 250                           | 610     | 1000 |
| VCC              | 500                           | 1200    | 2000 |

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The watchdog timer can not be disabled. It must be strobed with a high-to-low transition to avoid a watchdog timeout and reset.

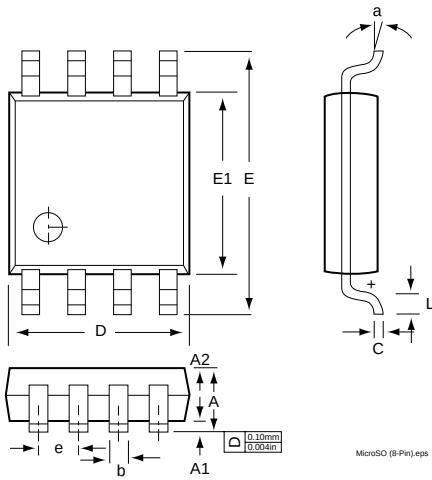


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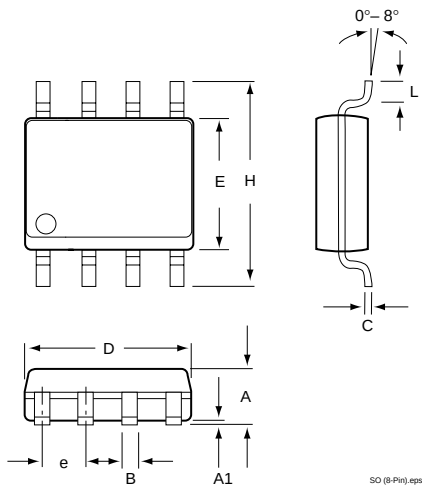
**Figure 6. Application Circuit: Watchdog Timer**

## Package Dimensions

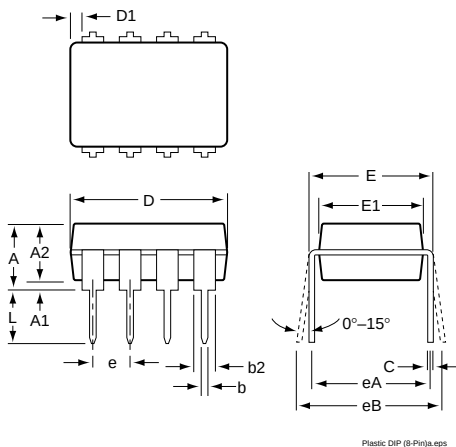
### MicroSO (8-Pin)



### SO (8-Pin)



### Plastic DIP (8-Pin)



| Inches                 |            |        | Millimeters |       |
|------------------------|------------|--------|-------------|-------|
|                        | Min        | Max    | Min         | Max   |
| MicroSO (8-Pin)*       |            |        |             |       |
| A                      | ———        | 0.0433 | ———         | 1.10  |
| A1                     | 0.0020     | 0.0059 | 0.050       | 0.15  |
| A2                     | 0.0295     | 0.0374 | 0.75        | 0.95  |
| b                      | 0.0098     | 0.0157 | 0.25        | 0.40  |
| C                      | 0.0051     | 0.0091 | 0.13        | 0.23  |
| D                      | 0.1142     | 0.1220 | 2.90        | 3.10  |
| e                      | 0.0256 BSC |        | 0.65 BSC    |       |
| E                      | 0.193 BSC  |        | 4.90 BSC    |       |
| E1                     | 0.1142     | 0.1220 | 2.90        | 3.10  |
| L                      | 0.0157     | 0.0276 | 0.40        | 0.70  |
| a                      | 0°         | 6°     | 0°          | 6°    |
| SO (8-Pin)**           |            |        |             |       |
| A                      | 0.053      | 0.069  | 1.35        | 1.75  |
| A1                     | 0.004      | 0.010  | 0.10        | 0.25  |
| B                      | 0.013      | 0.020  | 0.33        | 0.51  |
| C                      | 0.007      | 0.010  | 0.19        | 0.25  |
| e                      | 0.050      |        | 1.27        |       |
| E                      | 0.150      | 0.157  | 3.80        | 4.00  |
| H                      | 0.228      | 0.244  | 5.80        | 6.20  |
| L                      | 0.016      | 0.050  | 0.40        | 1.27  |
| D                      | 0.189      | 0.197  | 4.80        | 2.00  |
| Plastic DIP (8-Pin)*** |            |        |             |       |
| A                      | ———        | 0.210  | ———         | 5.33  |
| A1                     | 0.015      | ———    | 0.38        | ———   |
| A2                     | 0.115      | 0.195  | 2.92        | 4.95  |
| b                      | 0.014      | 0.022  | 0.36        | 0.56  |
| b2                     | 0.045      | 0.070  | 1.14        | 1.78  |
| b3                     | 0.030      | 0.045  | 0.80        | 1.14  |
| D                      | 0.355      | 0.400  | 9.02        | 10.16 |
| D1                     | 0.005      | ———    | 0.13        | ———   |
| E                      | 0.300      | 0.325  | 7.62        | 8.26  |
| E1                     | 0.240      | 0.280  | 6.10        | 7.11  |
| e                      | 0.100      | ———    | 2.54        |       |
| eA                     | 0.300      | ———    | 7.62        |       |
| eB                     | ———        | 0.430  | ———         | 10.92 |
| eC                     | ———        | 0.060  |             |       |
| L                      | 0.115      | 0.150  | 2.92        | 3.81  |

\* JEDEC Drawing MO-187AA

\*\* JEDEC Drawing MS-112AA

\*\*\* JEDEC Drawing MS-001BA

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IMP, Inc.  
Corporate Headquarters  
2830 N. First Street  
San Jose, CA 95134-2071  
Tel: 408-432-9100  
Tel: 800-438-3722  
Fax: 408-434-0335  
e-mail: [info@impinc.com](mailto:info@impinc.com)  
<http://www.impweb.com>