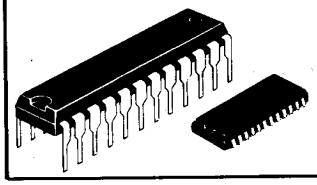
M5M5258AP, AJ-25, -30

262144-BIT(65536-WORD BY 4-BIT)CMOS STATIC RAM



DESCRIPTION

The M5M5258A is a family of 65536 word by 4-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

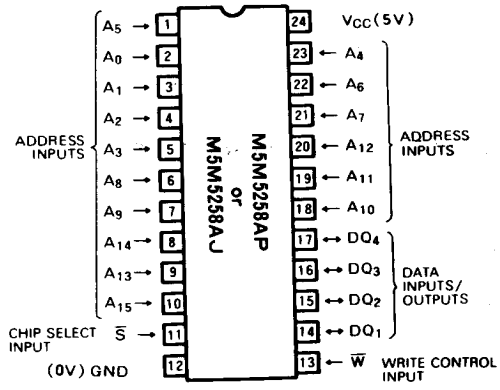
FEATURES

- Fast access time M5M5258AP, AJ-25 . . . 25 ns (max)
  M5M5258AP, AJ-30 . . . 30 ns (max)
- Low power dissipation Active . . . . . 300 mW (typ)
  Stand by . . . . . 5mW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
  Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input

APPLICATION

High-speed memory systems

PIN CONFIGURATION (TOP VIEW)



Outline 24P4Y (DIP)
24P0J (SOJ)

FUNCTION

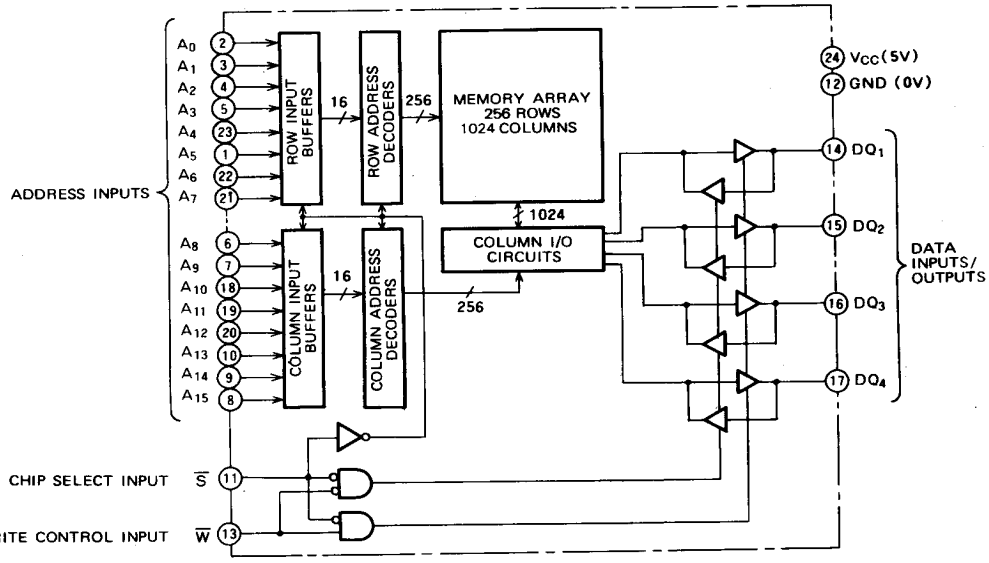
A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data ia available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



MODE SELECTION

$\overline{S}$	$\overline{W}$	Mode	Data I/O	I_{CC}
H	X	Non selection	High-impedance	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

H : V_{IH} L : V_{IL} X : V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		0~70	°C
$T_{stg(bias)}$	Storage temperature (bias)		−10~85	°C
T_{stg}	Storage temperature		−65~150	°C

* Pulse width ≦ 20 ns, In case of DC: −0.5V

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.4		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.5*		0.6	V
V_{OH}	High-level output voltage	I_{OH}=−4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL}=8mA				0.4	V
I_I	Input current	V_I=0~V_{CC}				2	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\overline{S})}$=V_{IH}, V_O=0~V_{CC}				10	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\overline{S})}$=V_{IL} Output open	AC (minimum cycle)			120	mA
			DC		60	75	mA
I_{CC2}	Stand by current	$V_{I(\overline{S})}$=V_{IH}	AC (minimum cycle)			40	mA
			Other V_I≧V_{IH} or ≦V_{IL}			30	mA
I_{CC3}	Stand by current	$V_{I(\overline{S})}$=V_{CC}−0.2V Other V_I≦0.2V or V_I≧V_{CC}−0.2V			1	10	mA

Note 1. Current flow into an IC is positive, out is negative.
* −3.0V in case of AC (Pulse width ≦ 20ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			5	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz			7	pF

AC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ..... V_{IH}=3V, V_{IL}=0V
Input rise and fall time 3ns
Input timing reference level
..... V_{IH}=2.4V, V_{IL}=0.6V
Output timing reference level
..... V_{OH}=2.0V, V_{OL}=0.8V
Output loads ..... Fig. 1, Fig. 2

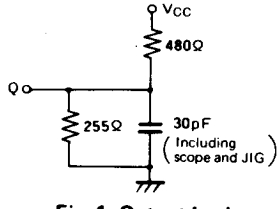


Fig. 1 Output load

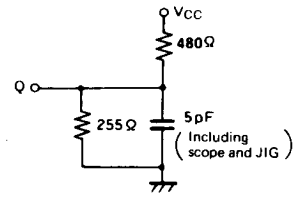


Fig. 2 Output load for t_{en}, t_{dis}

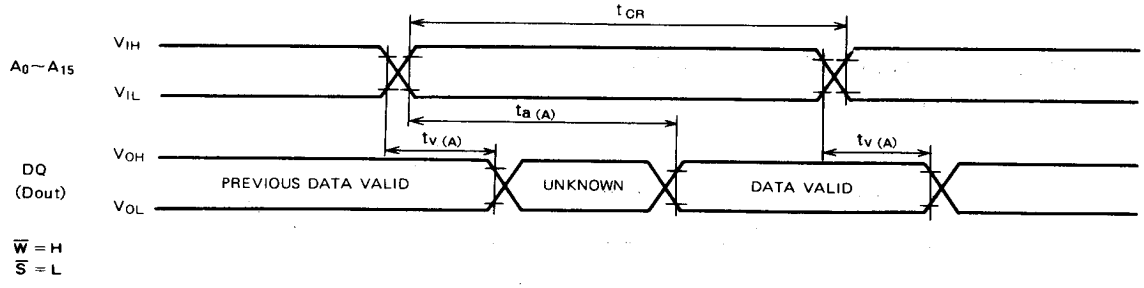
MITSUBISHI ELECTRIC

(2) READ CYCLE

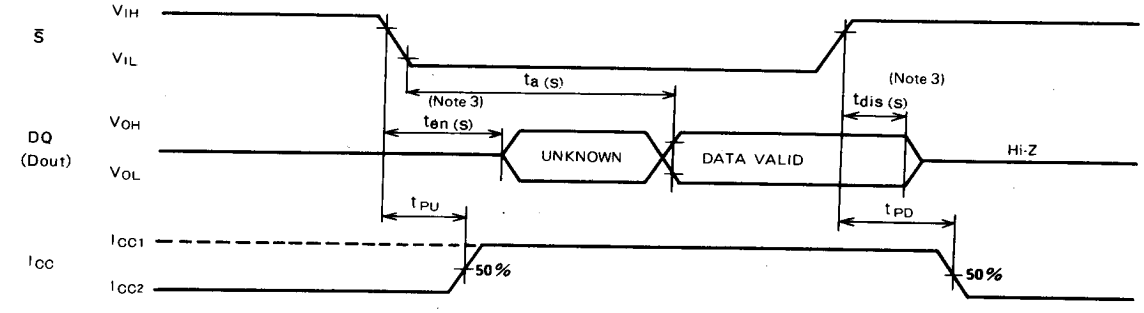
Symbol	Parameter	Limits						Unit
		M5M5258A-25			M5M5258A-30			
		Min	Typ	Max	Min	Typ	Max	
$t_{c(R)}$	Read cycle time	25			30			ns
$t_{a(A)}$	Address access time			25			30	ns
$t_{a(S)}$	Chip select access time			25			30	ns
$t_{v(A)}$	Data valid time after address	5			5			ns
$t_{en(S)}$	Chip selection to output active	5			5			ns
$t_{dis(S)}$	Output disable time from CS	0		15	0		15	ns
t_{PU}	Power-up time after chip selection	0			0			ns
t_{PD}	Power down time after chip deselection			25			30	ns

(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



Read cycle 2 (Note 2)



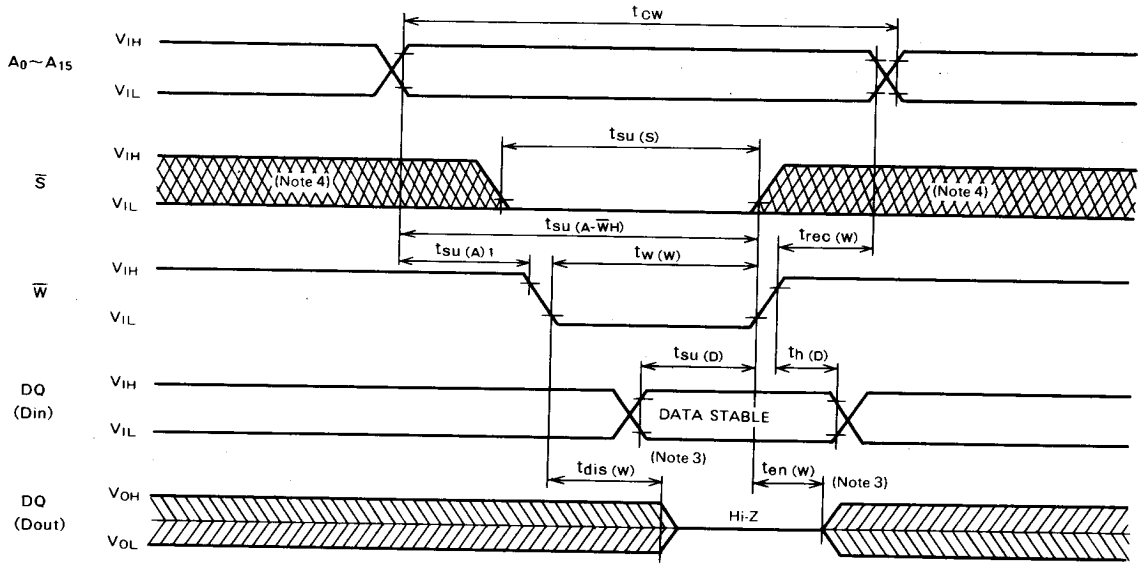
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

(4) WRITE CYCLE

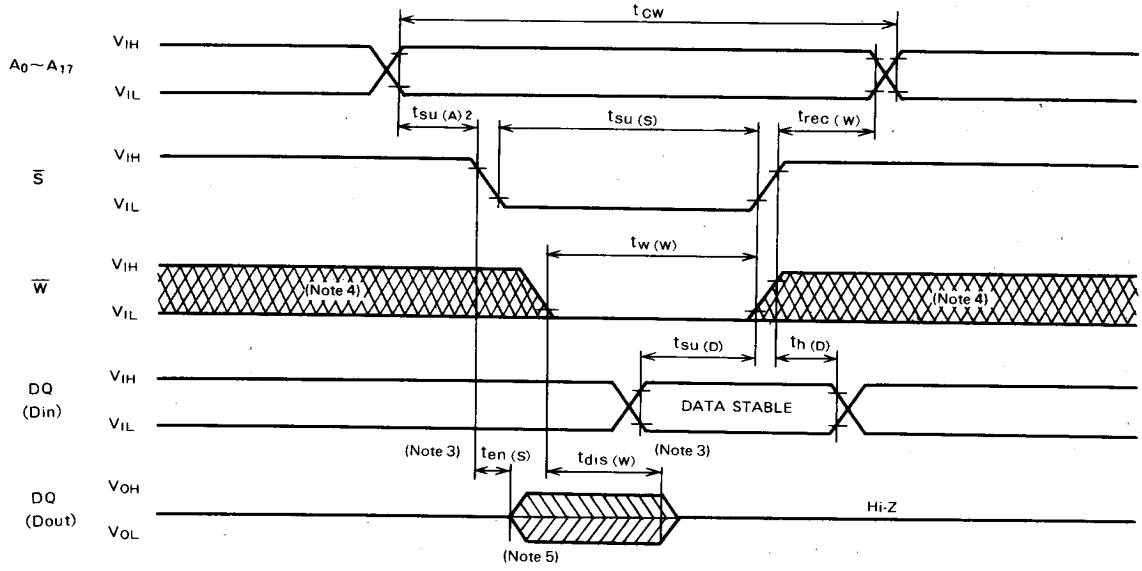
Symbol	Parameter	Limits						Unit
		M5M5258A-25			M5M5258A-30			
		Min	Typ	Max	Min	Typ	Max	
$t_{c(W)}$	Write cycle time	25			30			ns
$t_{su(S)}$	Chip select setup time	20			25			ns
$t_{su(A)1}$	Address setup time (W)	0			0			ns
$t_{su(A)2}$	Address setup time (S)	0			0			ns
$t_{w(W)}$	Write pulse width	20			25			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{su(D)}$	Data setup time	15			20			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{dis(W)}$	Output disable time from W	0		10	0		12	ns
$t_{en(W)}$	Output enable time from W	0			0			ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	20			25			ns

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.
5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.