BTC50010-1TAA

Smart High-Side Power Connector
Single Channel, 1mΩ

Data Sheet

1.3, 2015-02-06

Automotive Power

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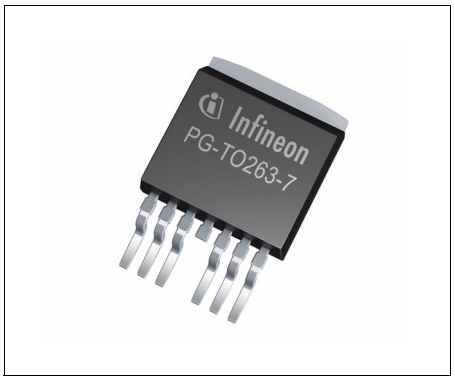
1 Overview



PG-TO-263-7-8

Applications

- Switching resistive, capacitive and inductive loads in conjunction with an effective peripheral free wheeling circuit
- Replaces electromechanical relay
- Most suitable for high current applications, such as Start-Stop, power distribution, main switch, heating systems
- PWM application with low frequencies

Features

- Load or Supply Line switching up to 30 A DC
- Operating temperature up to 150°C
- Current controlled Input pin
- Low Stand-by current
- Single channel 1mOhm power stage device with gate driver output for driving external MOSFET, easily combine with external MOSFET for reverse blocking or to halve the $R_{DS(ON)}$ (with BTC30010-1TAA). Auxiliary gate driver output for driving additional external MOSFET (optimized for BTC30010-1TAA).
- Electrostatic discharge protected (ESD)
- Optimized Electro Magnetic Compatibility (EMC)
- Very low power consumption in ON state
- Compatible to cranking pulse requirement (test pulse 4 in ISO7637 and cold start pulse in LV124)
- Infineon® Reversave™: Reverse battery protection by self turn ON of the power MOSFET
- Inverse operation robustness capability
- Infineon® SMART CLAMPING
- Green Product (RoHS compliant, halogen free package)
- AEC Qualified
- Dustproof

Description

The BTC50010-1TAA is a High-Side Power Connector optimized to replace electromechanical relays. It offers switching without audible noise, low conductive losses, weight reduction and increased switching cycle capability to comply with upcoming requirements on power distribution applications such as load or battery disconnect

Type	Package	Marking
BTC50010-1TAA	PG-TO-263-7-8	C50010A

switch. In addition, it significantly reduces power/current consumption of the device while ON to increase energy efficiency. It offers the possibility to drive an additional power MOSFET or BTC30010-1TAA via its CP pin to support reverse blocking or to halve the $R_{DS(ON)}$. The device can withstand cranking pulses such as test pulse 4 in ISO7637 and cold start pulse in LV124.

Table 1 Product Summary

Parameter	Symbol	Values
Weight (approx.)	G	1.5 g
Nominal operating voltage	$V_{S(OP)}$	8 V … 18 V
Extended operating voltage contains dynamic undervoltage capability	$V_{S(DYN)}$	3.2 V … 28 V
Nominal load current	$I_{L(NOM)}$	30 A
Typical ON-state resistance at T_J = 25 °C (CP pin open)	$R_{DS(ON)}$	0.9 mΩ
Typical input current in ON state	$I_{IN(ON)}$	2 mA
Typical stand-by current at T_J = 25 °C	$I_{S(OFF)}$	3 µA

2 Block Diagram

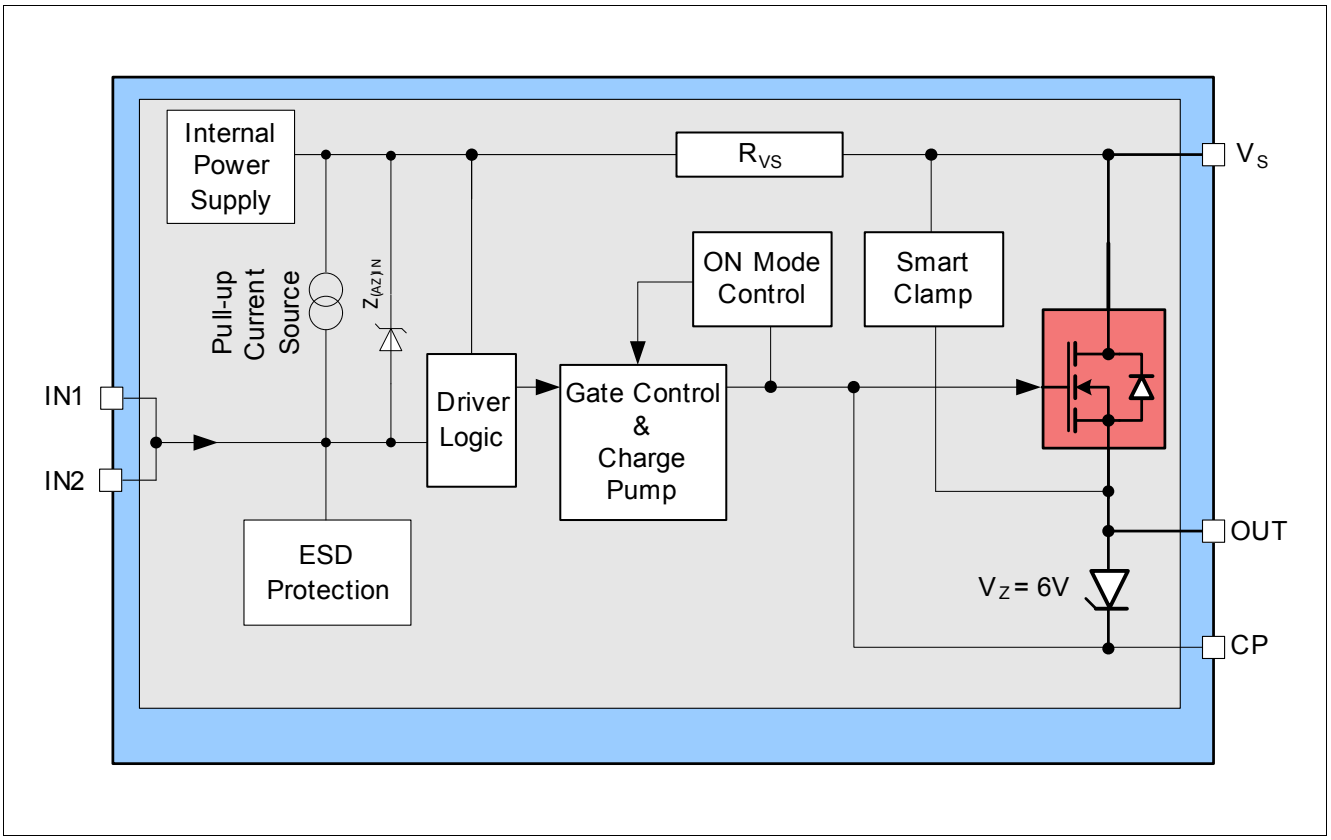


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

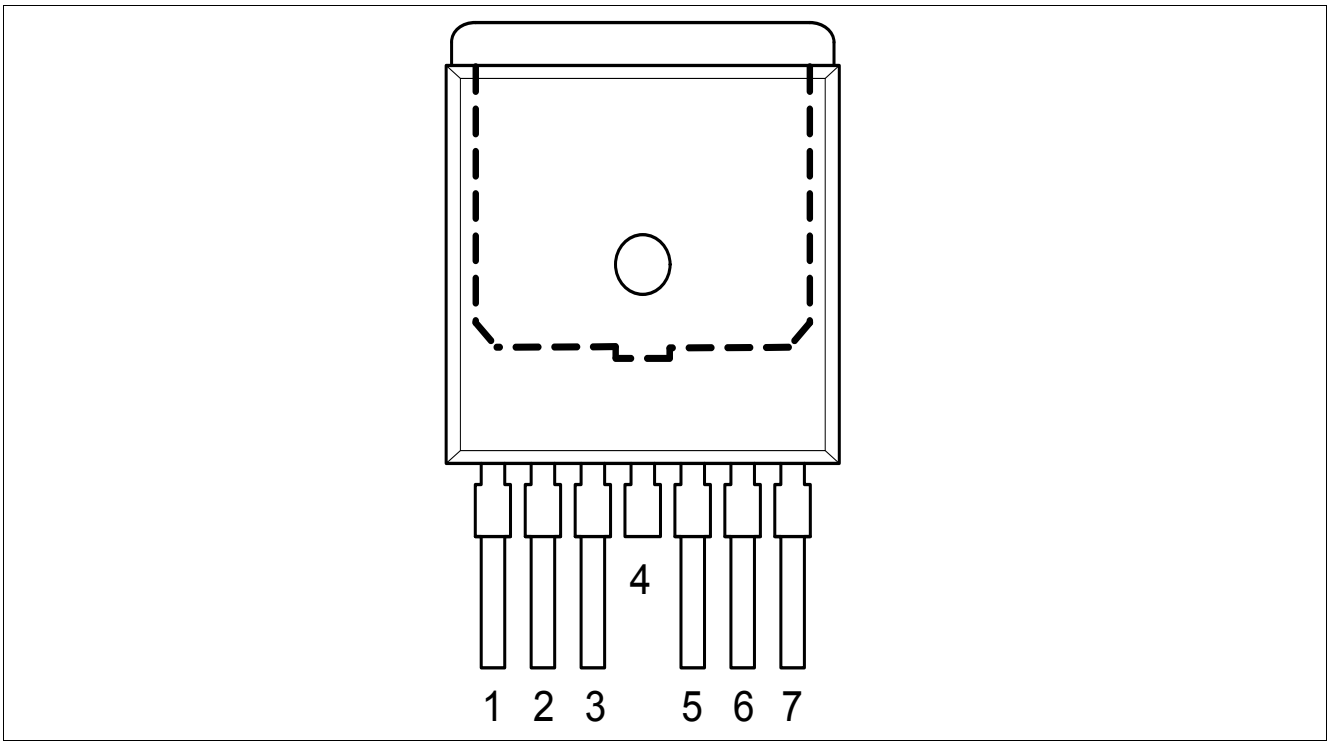


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	IN1	**IN1**; Pull down to module ground for channel activation[1)]
2	IN2	**IN2;** Pull down to module ground for channel activation[1)]
3	CP	**Charge Pump Output;** Output pin of internal charge pump voltage
4, Cooling Tab	VS	**Supply Voltage;** Connected to battery voltage
5, 6, 7	OUT	**OUTPUT;** High side power output[2)]

1) IN1 and IN2 are internally connected

2) All output pins are connected internally. All output pins have to be connected externally together on PCB. Not shorting all outputs pins will considerably increase the ON-resistance. PCB traces have to be designed to withstand the maximum current which can flow.

3.3 Voltage and Current Definition

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

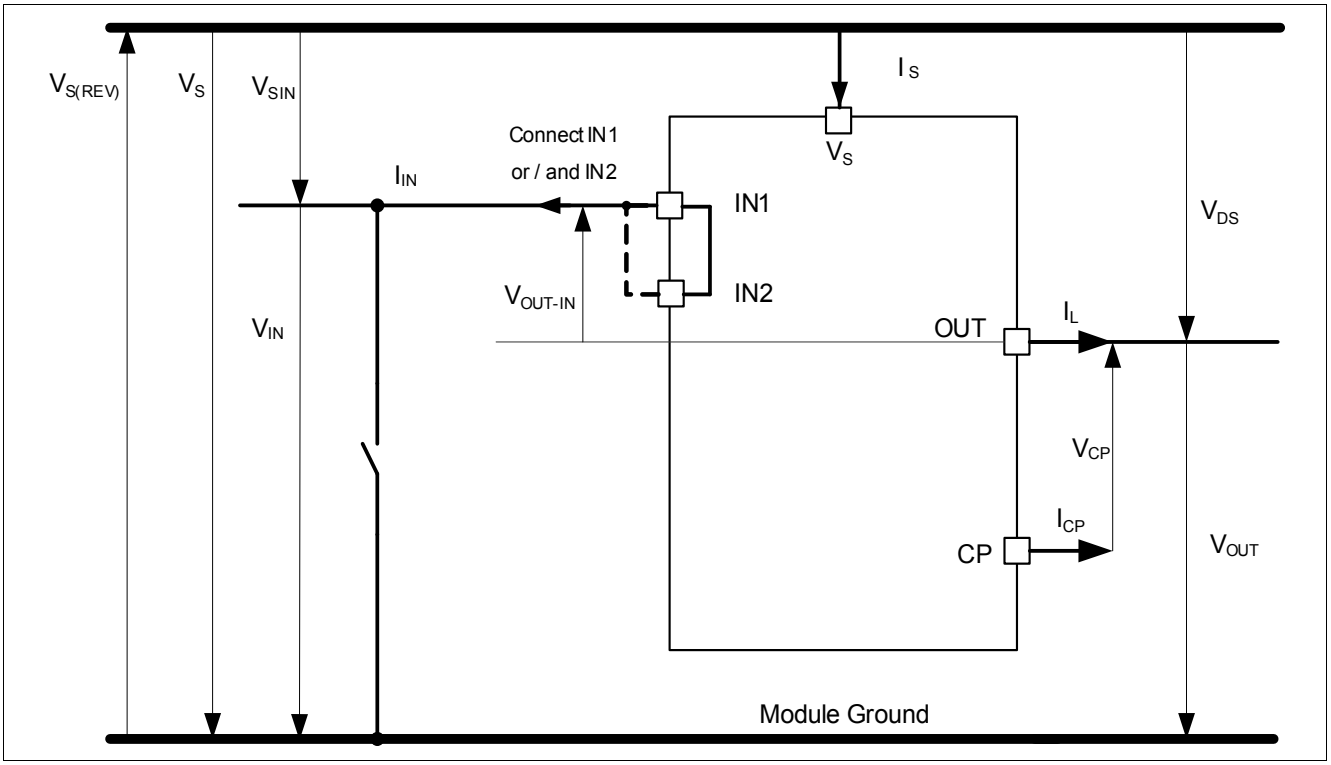


Figure 3 Voltage and Current Definition

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1)]

T_J = -40 °C to +150 °C, all voltages and currents refer to definitions in Figure 3 (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply Voltage	V_S	-0.3	–	28	V	–	P_4.1.1
Voltage from V_S to IN pin	V_{SIN}	-0.3	–	60	V	–	P_4.1.2
Reverse polarity voltage	$V_{S(REV)}$	–	–	16	V	t < 2 min T_A = 25 °C R_L ≥ 0.5Ω V_{IN} = 0 V Figure 18 Figure 19	P_4.1.3
Supply voltage for load dump protection	$V_{S(LD)}$	–	–	45	V	[2)] R_L = 1.0 Ω R_{IN} = 100 Ω	P_4.1.4
Voltage at CP pin	V_{CP}	-0.3	–	V_{CP_ON}	V	V_{CP} = V_{GS_C}	P_4.1.5
Voltage from OUT to IN pin V_{OUTIN} = V_{OUT} -V_{IN}	V_{OUT-IN}	-64	–	–	V	[3)]	P_4.1.6
Currents							
Current through CP pin	I_{CP}	-20	–	20	mA	for t < 0.5 ms during switch ON/OFF	P_4.1.7
Device current vs. time capability at: $I_{6.0\_125°C}$ = 0.85 x 6.0 x I_{RATE} for I_{RATE} = 30A[4)]	t @ $I_{6.0}$	–	–	0.24	s	[5)] BTC50010-1TAA alone or drive BTC30010-1TAA in anti serial, current level: $I_{6.0\_125°C}$ = 153 A, T_A = 125 °C, Figure 4	P_4.1.8
Continuous drain current	I_D	–	–	163	A	T_C = 25 °C V_{IN} = 0 V, I_{CP} ≤ 2µA Current is limited by bondwire	P_4.1.9
Power Stage							
Average power dissipation	P_{TOT}	–	–	160	W	[6)] For $T_{J(0)}$ ≤ 105 °C	P_4.1.13
Temperatures							
Junction Temperature	T_J	-40	–	150	°C	–	P_4.1.14
Dynamic Temperature increase while switching	ΔT_J	–	–	60	K	–	P_4.1.15

Table 2 Absolute Maximum Ratings (cont'd)[1)]

T_J = -40 °C to +150 °C, all voltages and currents refer to definitions in **Figure 3** (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Storage Temperature	T_{STG}	-55	–	150	°C	–	P_4.1.16
ESD Susceptibility							
ESD Susceptibility (all pins)	V_{ESD}	-2	–	2	kV	HBM[7)]	P_4.1.17
ESD Susceptibility OUT pin vs. V_S	V_{ESD_out}	-4	–	4	kV	HBM[7)]	P_4.1.18

1) Not subject to production test, specified by design.

2) $V_{S(LD)}$ is setup without DUT connected to the generator per ISO 7637-1.

3) Relevant to application case such as loss of load, loss of battery (also negative ISO pulse).

4) $I_{Q\_b\_125°C}$ = a x b x I_{RATE}. "a" is the temperature re-rating factor from the fuse curve for 125°C refer to 25°C. "b" is the factor of load current to I_{RATE} at 25°C.

5) Use test PCB with 2 x 70 µm Cu layers and size of 54 x 48 x 1.5 mm. Where applicable, thermal via array is placed under the device footprint on this PCB. BTC50010-1TAA on PCB has $R_{thJA(2P)}$ = 19.6 K/W (referring to 1W power dissipation). PCB is vertical, keep constant environment temperature by indirect airflow of 6L/s.

6) P_{TOT} = ($T_{J(0)}$ - T_C) / R_{thJC}. P_{TOT_max} = (105°C - 25°C) / 0.5 K/W = 160 W.

7) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001-2010.

BTC50010-1TAA current robustness:

Below diagram present the current robustness of BTC50010-1TAA. Generally, module thermal characteristic is more depending on the module construction (e.g. PCB size, metal layer thickness and numbers, module connectors) than the thermal characteristic of BTC50010-1TAA alone. When current pulse is longer than 0.3s, influence of module thermal characteristic is dominant. When current pulse is shorter than 0.3s, influence of thermal characteristic of BTC50010-1TAA is getting significant.

Combining BTC50010-1TAA together with a fuse in application, the total I/t curve of the module (incl. BTC50010-1TAA) has to be above the fuse I/t curve. With specified test setup [1] BTC50010-1TAA can withstand minimum 10 fuse blows of a 30A ATO FUSE.

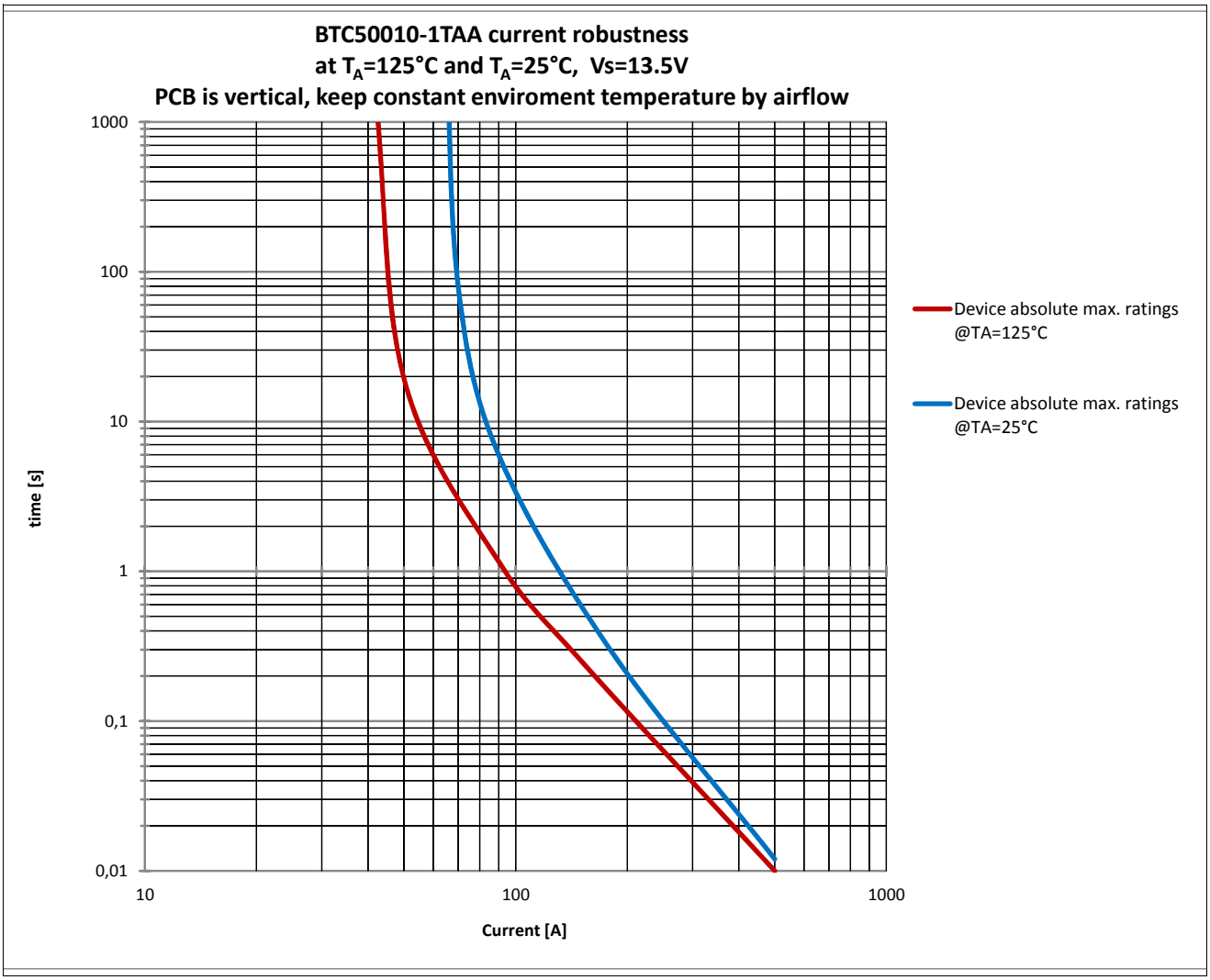


Figure 4 BTC50010-1TAA Current Robustness at T_A = 25°C and T_A = 125°C; V_S = 13.5V [1]

Notes

1. *Stresses above the ones described in **Chapter 4.1** may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

1) Use test PCB with 2 x 70 µm Cu layers and size of 54 x 48 x 1.5 mm. Where applicable, thermal via array is placed under the device footprint on this PCB. BTC50010-1TAA on PCB has RthJA(2P) = 19.6 K/W (referring to with 1 W power dissipation). PCB is vertical, keep constant environment temperature by indirect airflow of 6l/s.

2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 3 Functional Range

T_J = 25 °C, all voltages and currents refer to definitions in **Figure 4** (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating voltage	V_{S_OP}	8	–	18	V	–	P_4.2.1
Extended static operating voltage	$V_{S\_OP\_EXT}$	5	–	28	V	1) 2) $I_L \le I_{L(NOM)}$	P_4.2.2
Extended operating voltage contain dynamic undervoltage capability	V_{S_DYN}	3.2	–	28	V	1) V_S decreasing according to ISO7637 according to LV124	P_4.2.3
Static undervoltage level (start of loss of functionality)	V_{S_UV}	–	–	4.5	V	R_L=270 Ω V_S decreasing V_{DS} ≤ 0.5 V I_{CP_ON} = 0 µA **Figure 5**	P_4.2.4
Undervoltage restart level static	$V_{S\_UV\_Restart}$	–	–	5	V	R_L=270 Ω V_S increasing V_{DS} ≤ 0.5 V I_{CP_ON} = 0 µA **Figure 5**	P_4.2.5
Charge pump current in ON state (maximum allowed leakage current at CP pin)	I_{CP_ON}		0	2	µA	V_{IN} = 0 V, $t > t_{ON}$	P_4.2.6
Maximum allowed Current in OFF state IN pins High	I_{IN_OFF}	–	–	30	µA	Pull-up current flow through internal current source	P_4.2.7

1) Not subject to production test, specified by design.

2) Within the range of $V_{S\_OP\_EXT}$ and out of the range of V_{S_OP}, device parameter deviation is possible.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

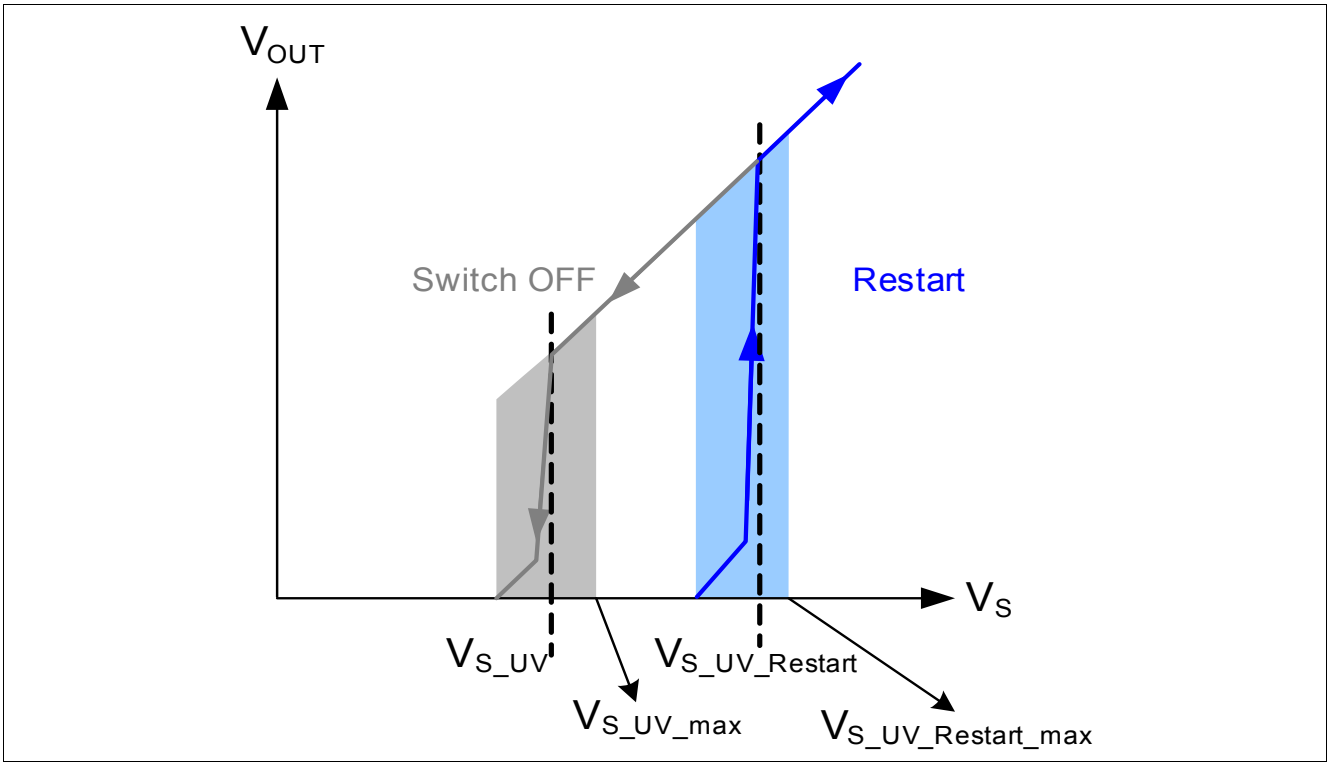


Figure 5 Undervoltage Behavior of BTC50010-1TAA

4.3 Thermal Resistance

Table 4 Thermal Resistance[1] at T_J = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	–	0.5	K/W	2)	P_4.3.1
Junction to Ambient	$R_{thJA(2S2P)}$	–	20	–	K/W	2) 3)	P_4.3.2
Junction to Ambient	$R_{thJA(1S0p)}$	–	70	–	K/W	2) 4)	P_4.3.3

1) Not subject to production test, specified by design.

2) Device is dissipating 1W power.

3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a 76,4 x 114,3 x 1,5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer.

4) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76,4 x 114,3 x 1,5 mm board with 1 copper layer (1 x 70 µm Cu).

Figure 6 is showing the typical thermal impedance of BTC50010-1TAA mounted on different PCB setup on FR4 1s0p (single layer) and 2s2p (quad layer) boards at T_J of 25°C and 105°C according to Jedec JESD51-2,-5,-7 at natural convection.

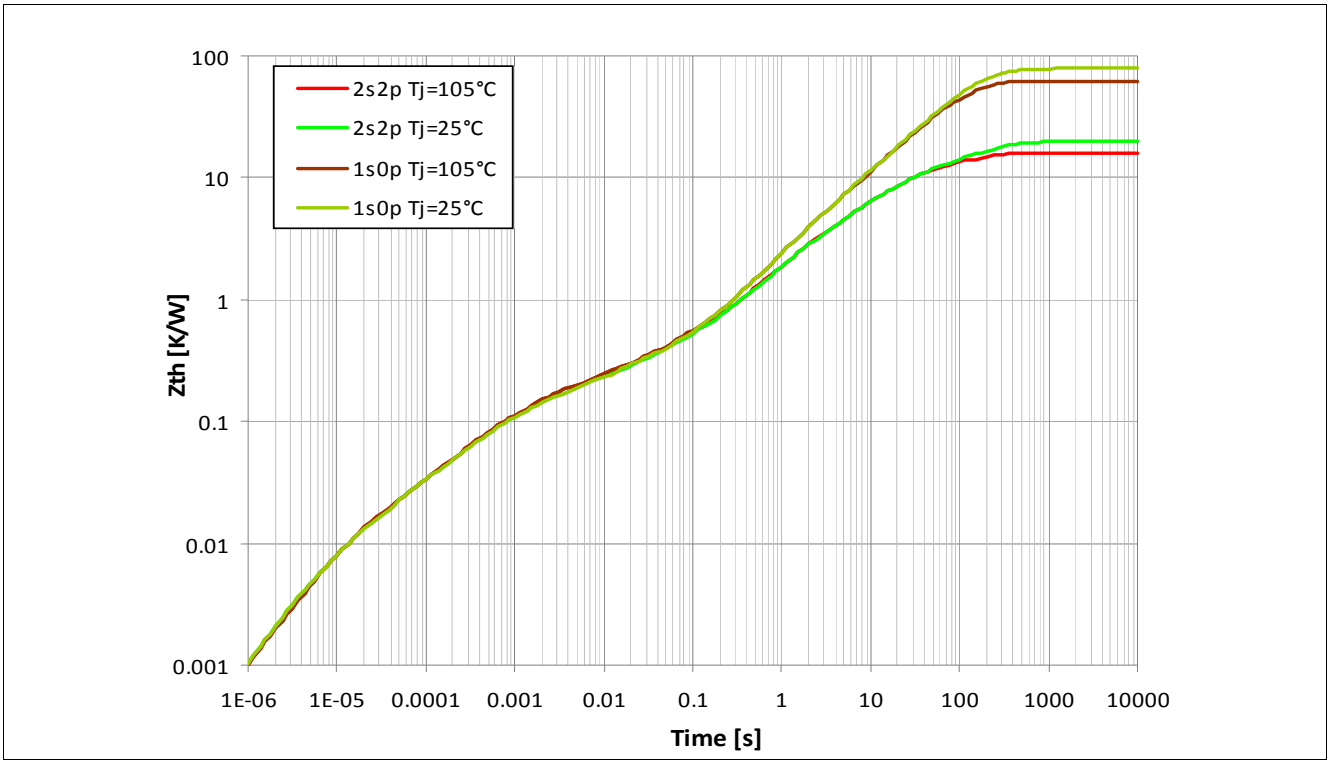


Figure 6 Typical Transient Thermal Impedance $Z_{th(JA)} = f(t)$ for Different Cooling Areas

5 Functional Description

5.1 Power Stage

5.1.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_J. **Figure 16** shows the dependencies in terms of temperature and supply voltage, for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 5.7**.

A LOW signal (see **Chapter 5.2**) at the input pin causes a current I_{IN} flowing internally from the V_S pin out of the IN pin to the module Ground, thus the power DMOS is switched ON with a dedicated slope, which is optimized in terms of EMC emission.

5.1.2 Switching an Inductive Load

When switching OFF inductive loads with high side switches, the voltage V_{OUT} is driven below ground potential, due to the fact that the inductance intends to continue driving the current. To prevent the destruction of the device due to high voltages, the device implements an overvoltage protection, which clamps the voltage between VS and VOUT at $V_{DS(CL)}$ (see **Figure 7**).

Nevertheless it is not recommended to operate the device repetitively under this condition. Therefore, when driving inductive loads, a free wheeling diode must be always placed.

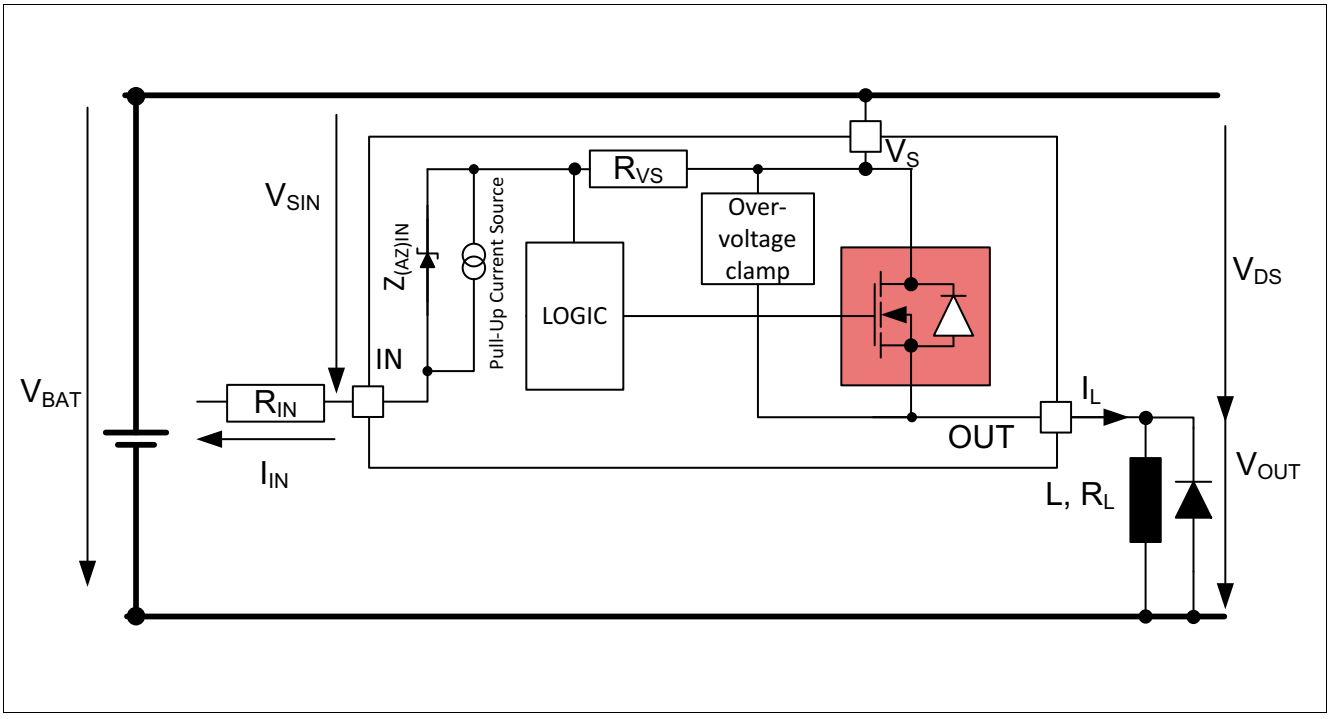


Figure 7 Overvoltage Clamp

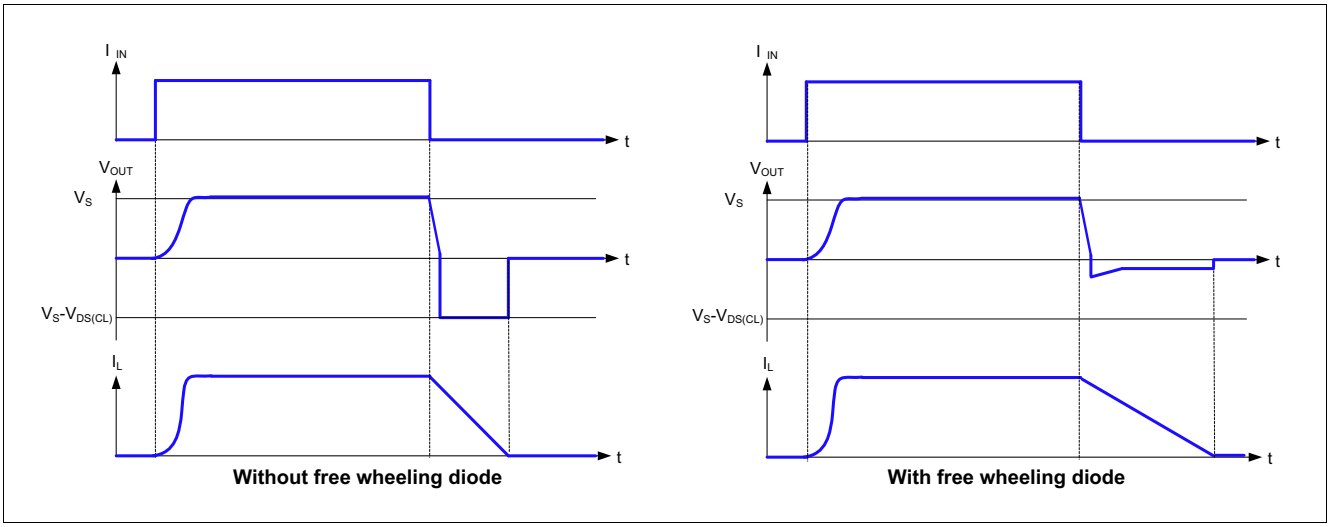


Figure 8 Switching an Inductance with or without free wheeling diode

It is important to verify the effectiveness of the freewheeling solution (see **Figure 8**), which means the selection of the proper diode and of an appropriate free wheeling path. With regard to the choice of the free wheeling diode, low threshold and fast response are key parameter to achieve an effective result.

Moreover the diode should be placed in order to have the shortest wire connection with the load (see **Figure 9**).

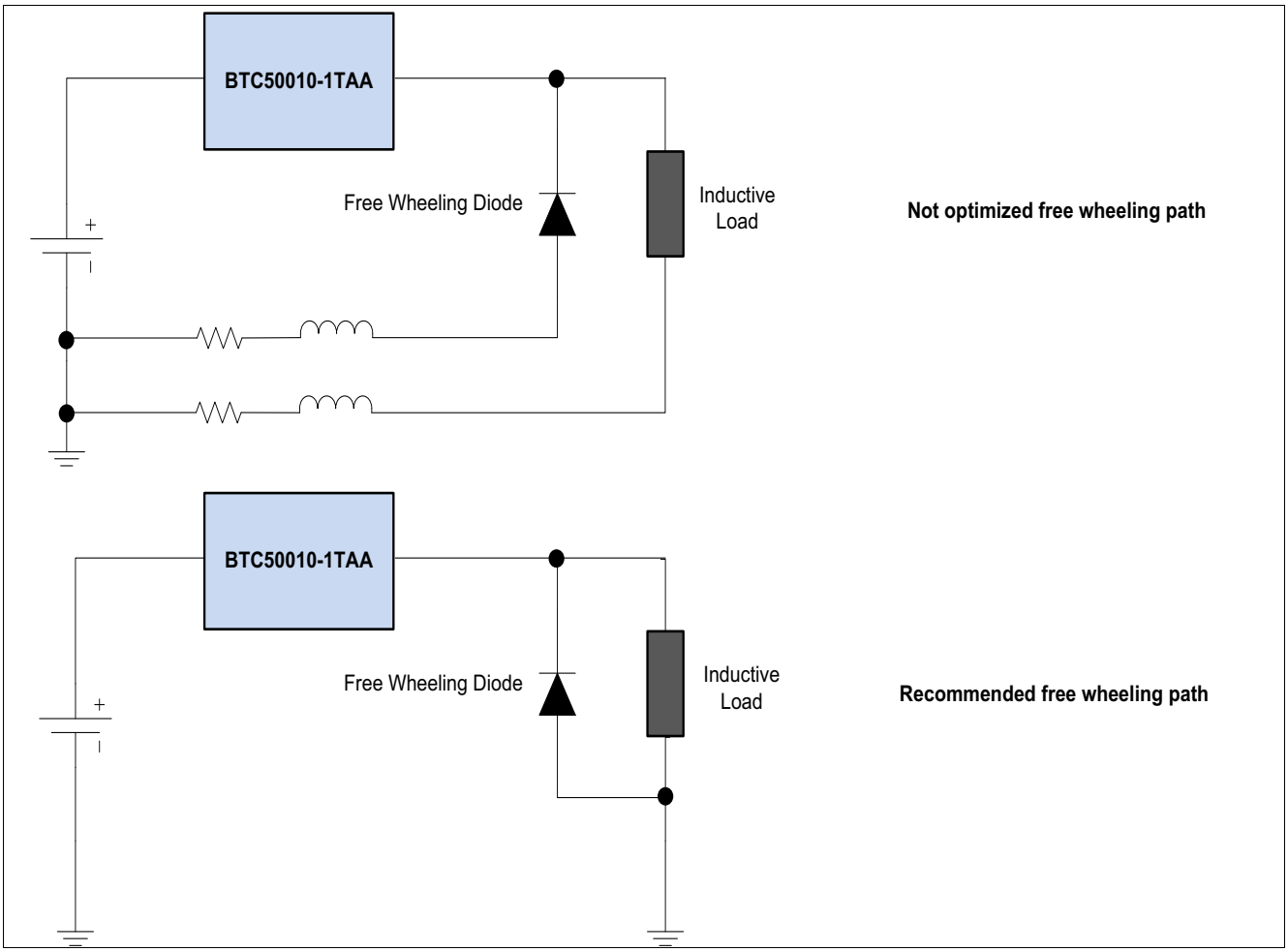


Figure 9 Optimization of the free wheeling path

5.2 Gate Driver Functionality

BTC50010-1TAA has an embedded gate driver. It is used to drive the gate of an integrated power DMOS. The gate driver charges and discharges the gate of the DMOS with current I_{CHARGE} and $I_{DISCHARGE}$. Refer to **Figure 10**, the gate driver is accessible via the CP pin. BTC50010-1TAA is suitable for driving an external MOSFET (e.g. BTC30010-1TAA) in parallel to halve the connect resistance or in anti serial to block the reverse current. It allows also to connect a capacitor C_{CP} to buffer the V_{CP} voltage during cranking time.

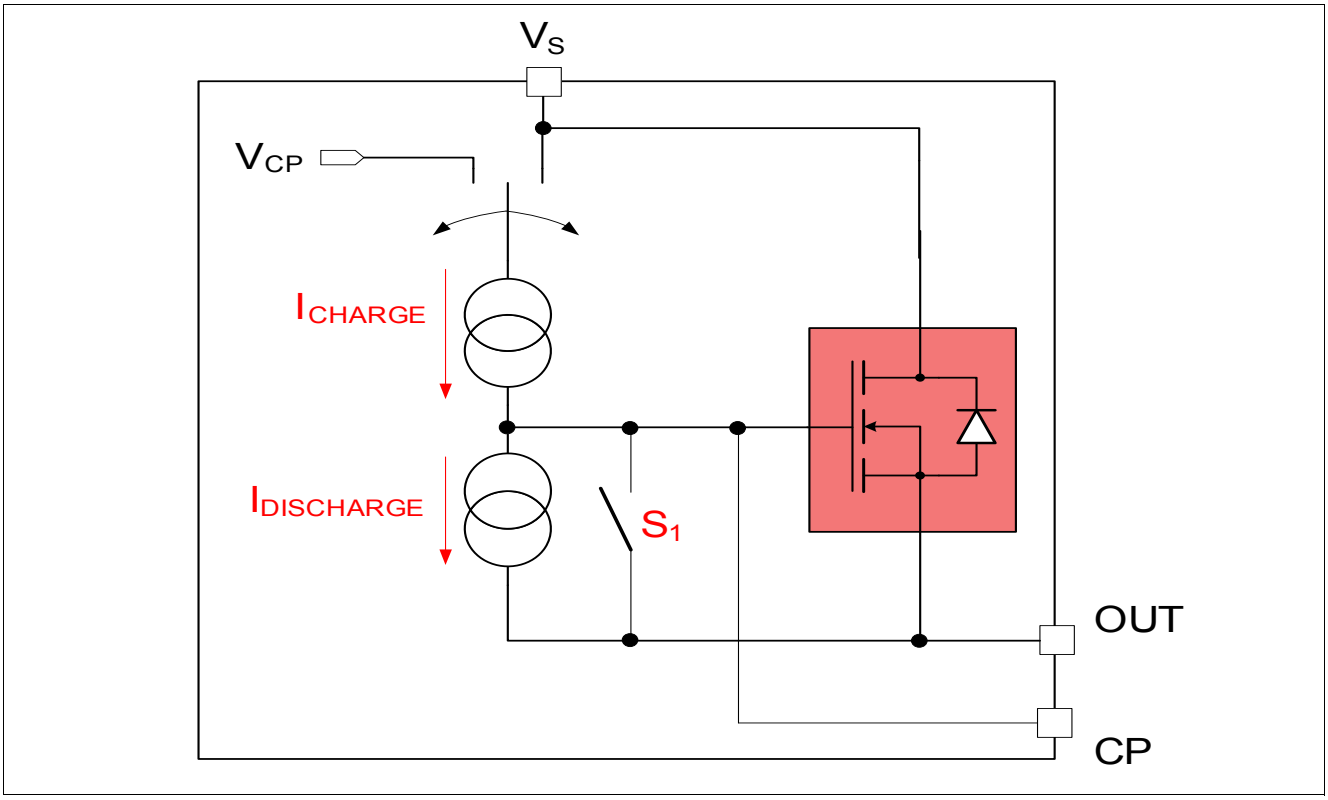


Figure 10 Gate Driver Block Diagram

During Switch ON, BTC50010-1TAA charges the Gate capacitor of an external DMOS or the capacitor C_{CP} which is connected between CP and OUT pin. During switch OFF, when VOUT decreases to around 2.5V below V_S, the internal switch S_1 between gate and source will switch ON to reduce the high energy consuming switch OFF time. Additionally, when S_1 is switched ON, the device is much more robust against electromagnetic disturbance which could come from V_S or output pin to ensure the device doesn't suffer from an unwanted switch ON.

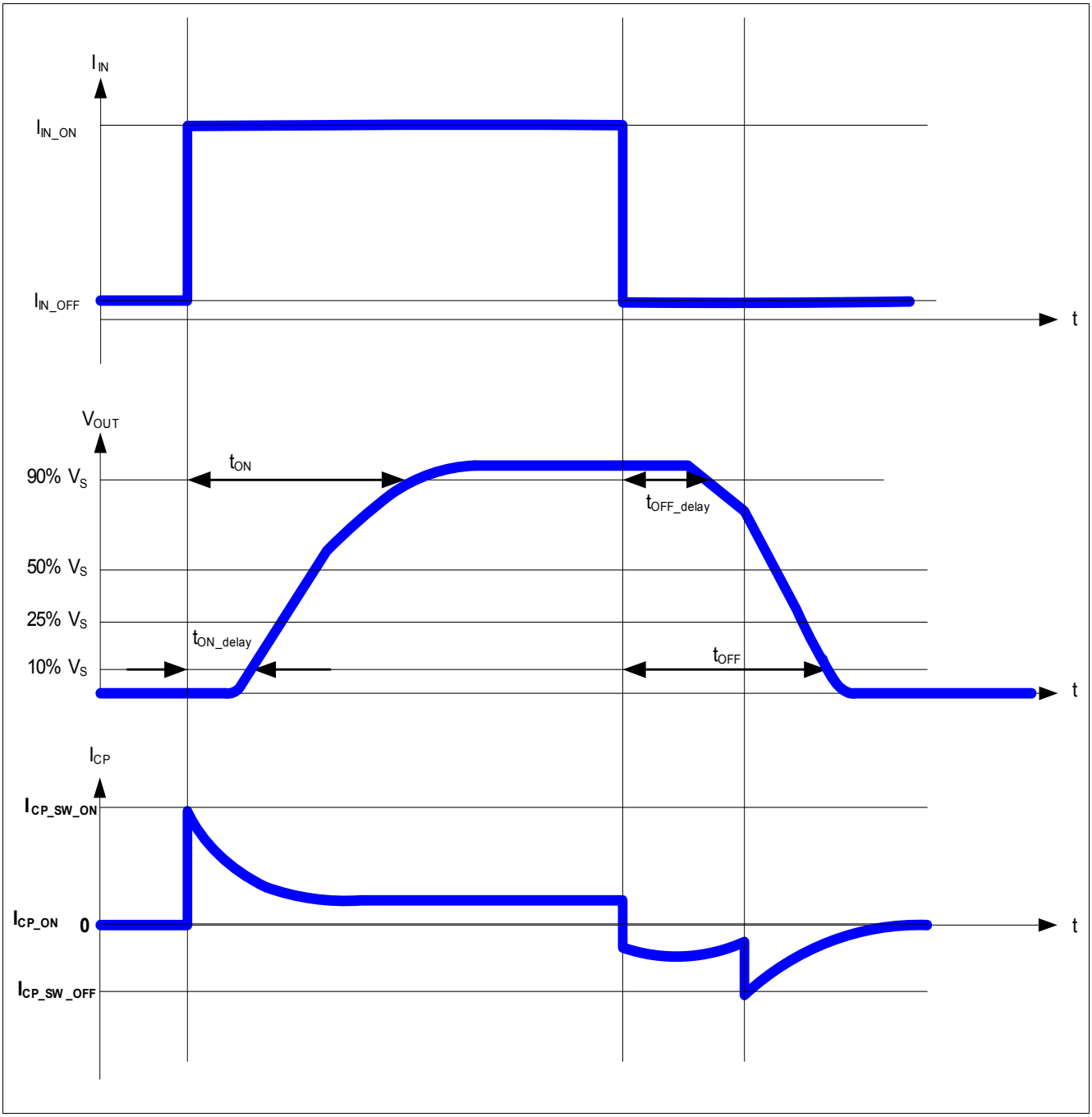


Figure 11 Switch ON and OFF Timing

*Note: **Figure 11** shows the general switching behavior. Under real condition, voltage or current sketch deviation is possible.*

5.3 Undervoltage Protection

Below V_{S_UV} maximum value, the under voltage condition is met. Upon further decrease of V_S, the device will begin to lose functionality, until finally it will turn OFF. During V_S increasing, as soon as the supply voltage is above the static level $V_{S\_UV\_Restart}$, device can be switched ON. **Figure 5** sketches the undervoltage mechanism.

5.4 Overvoltage Protection

The BTC50010-1TAA provides Infineon® SMART CLAMPING functionality, which suppresses over voltages by actively clamping the overvoltage across the power stage and the load. This is achieved by controlling the clamp voltage $V_{DS(CL)}$ depending on the junction temperature T_J and the load current I_L.

5.5 Protection during Loss of Load or Loss of V_S Condition

In case of loss of V_S with charged line inductances, the maximum supply voltage has to be limited. It is recommended to use a diode and a Z-diode (V_{Z1} + V_{D1} < 16V, please refer to **Figure 12**).

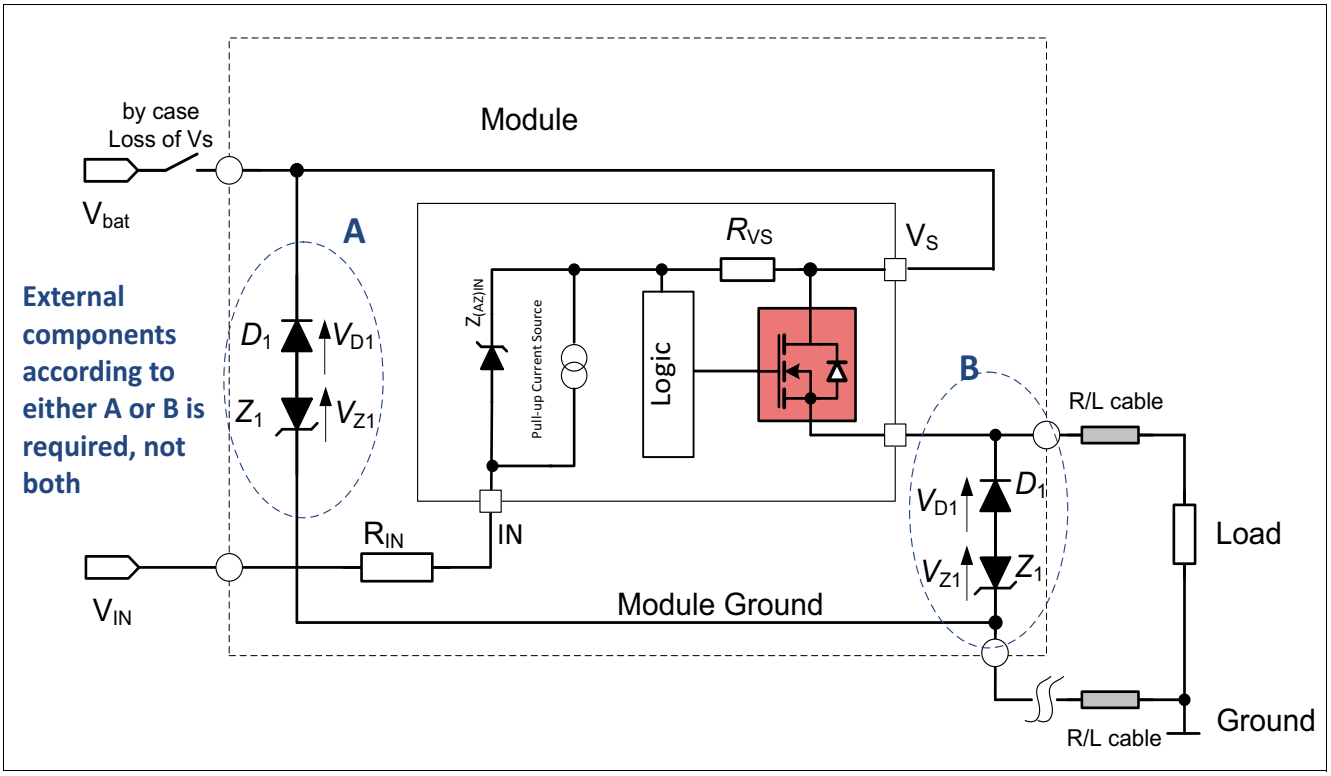


Figure 12 External Component for BTC50010-1TAA Loss of V_S Protection

In case of loss of load with charged primary power line inductances, the maximum supply voltage also has to be limited. It is recommended to use a Z-diode (V_{Z2} < 28V) or V_S clamping power switches between V_S and Module Ground (please refer to **Figure 13**).

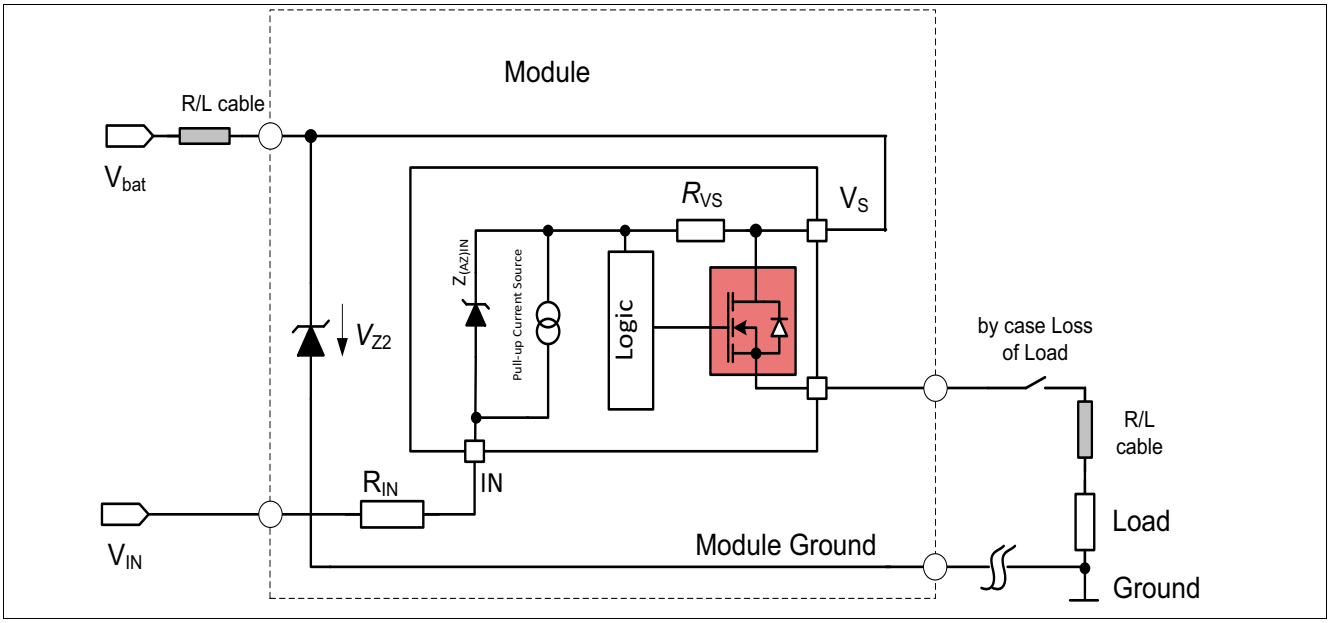


Figure 13 External Component for BTC50010-1TAA Loss of Load Protection

The 16V Z-diode refers to the maximum $V_{S(REV)}$ voltage of the chip. The 28V Z-diode refers to the maximum supply voltage (V_S) of the chip.

5.6 Inverse Current Capability

In case of inverse current, meaning a voltage V_{OUT} at the output higher than the supply voltage V_S (e.g. caused by a load operating as a generator), a current I_L will flow from output to V_S pin via the body diode of the power transistor (please refer to **Figure 14**). In case the IN pin is LOW[1], the power DMOS is already activated and keeps ON. In case, the input goes from “H” to “L”, the DMOS will be activated. Due to the limited speed of INV comparator, the output voltage slope needs to be limited. In case the IN pin is HIGH[2], power DMOS will not be switched ON automatically. Current will flow through the intrinsic body diode. This power dissipation could cause heating effect, which has to be considered.

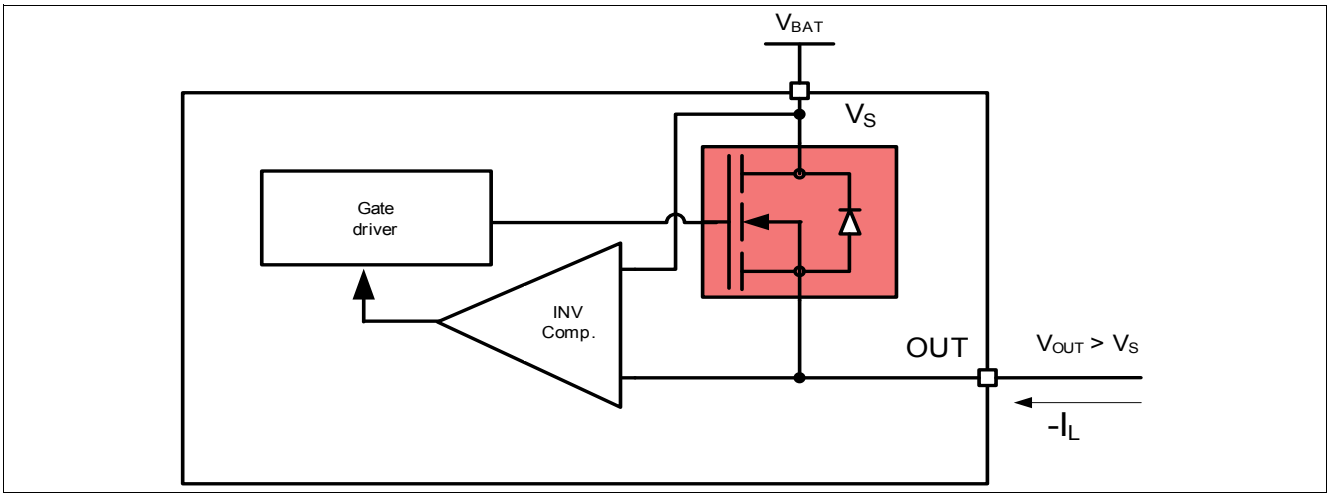


Figure 14 BTC50010-1TAA Inverse Current Circuitry

1) LOW means IN pin is pulled-down by external transistor or $I_{IN} > 0$

2) HIGH (H) means $I_{IN} = 0$

5.7 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode of the power DMOS causes power dissipation. To limit the risk of over temperature, the device provides Infineon® Reversave™ function. The power in this intrinsic body diode is limited by turning the DMOS ON. The DMOS resistance is then equal to $R_{DS(ON)\_REV}$ (please refer to **Figure 18** and **Figure 19**).

Additionally, the current into the logic has to be limited. The device includes a R_{VS} resistor which limits the current in the diodes. To avoid over current in the R_{VS} resistor, it is nevertheless recommended to use a R_{IN} resistor. **Figure 15** shows a typical application. The recommended typical values for R_{IN} is 100Ω.

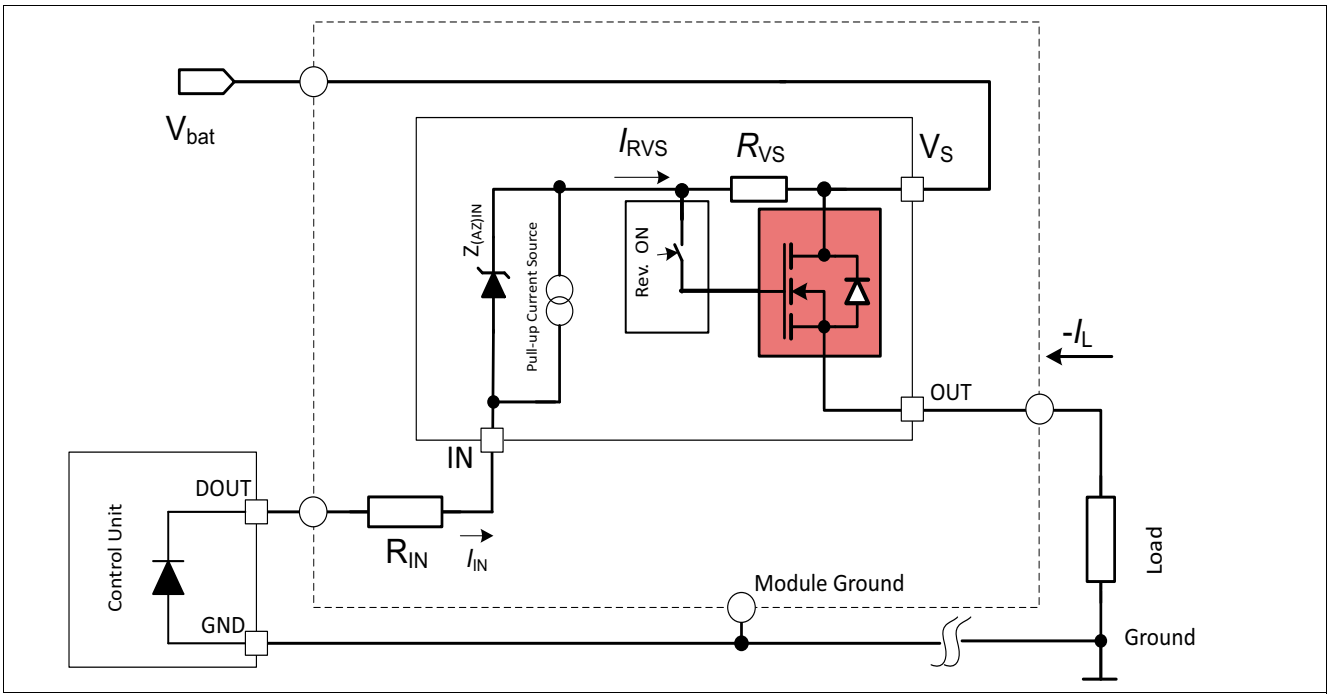


Figure 15 BTC50010-1TAA Reverse Polarity Protection with External Components

*Note: The R_{VS} has a typical value of 80Ω at 25°C. Refer to **Figure 15**, the R_{VS} and R_{IN} build up a voltage divider to split up the supply voltage on BTC50010-1TAA, which protect the device during high voltage pulse (e.g. ISO pulse 3b).*

5.8 Electrical Characteristics

Table 5 Electrical Characteristics: Power Stage

V_S = 13.5 V, T_J = 25 °C, all voltages and currents refer to definitions in **Figure 3** (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltage drop	V_{DROP}	–	27	36	mV	I_L = 30 A	P_5.8.1
ON-state resistance	$R_{DS(ON)}$	–	0.9	1.2	mΩ	CP pin open **Figure 16**	P_5.8.2
ON-state resistance hot	$R_{DS(ON)\_HOT}$	–	–	2.0	mΩ	T_J= 150 °C **Figure 16**	P_5.8.3
ON-state resistance in Infineon® Reversave™	$R_{DS(ON)\_REV}$	–	0.9	–	mΩ	V_{IN} = 0 V	P_5.8.4
ON-state resistance during inverse operation	$R_{DS(ON)\_INV}$	–	0.9	–	mΩ	V_{IN} = 0 V	P_5.8.5
Supply current stand-by IN pins floating	I_{S_OFF}	–	3	12	µA	Leakage current flow through OUT pin	P_5.8.6
Drain to source smart clamp voltage $V_{DS(CL)} = V_S - V_{OUT}$	$V_{DS(CL)}$	28	–	60	V	I_{DS} = 50 mA T_J= 25 °C to 150°C	P_5.8.7

Table 6 Electrical Characteristics: Input Stage

V_S = 13.5 V, T_J = 25 °C, all voltages and currents refer to definitions in **Figure 3** (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input current in ON state IN pins Low	I_{IN_ON}	–	2	3	mA	V_S = 18 V	P_5.8.8

Table 7 Electrical Characteristics: Charge Pump

V_S = 13.5 V, T_J = 25 °C, all voltages and currents refer to definitions in **Figure 3** (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Charge pump current during SWITCH ON	$I_{CP\_SW\_ON}$	0.7	2.2	–	mA	V_{IN} = 0 V V_{CP} = 0 V	P_5.8.9
Charge pump current during SWITCH OFF	$I_{CP\_SW\_OFF}$	350	850	–	µA	$V_{IN} = V_S$ = 8 V $V_{CP} = V_{CP\_ON}$ $V_{OUT} = V_S$	P_5.8.10
Charge pump voltage	V_{CP_ON}	5	–	7	V	V_{IN} = 0 V **Figure 22**	P_5.8.11

Table 8 Electrical Characteristics: Timing

V_S = 13.5 V, T_J = 25 °C, all voltages and currents refer to definitions in **Figure 3** (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Turn ON time	t_{ON}	–	200	500	µs	See timing **Figure 11** CP pin open	P_5.8.12
Turn OFF time	t_{OFF}	–	200	500	µs	See timing **Figure 11** CP pin open	P_5.8.13
Turn ON delay time	t_{ON_delay}	–	80	150	µs	**Figure 11** CP pin open	P_5.8.14
Turn OFF delay time	t_{OFF_delay}	–	180	300	µs	**Figure 11** CP pin open	P_5.8.15

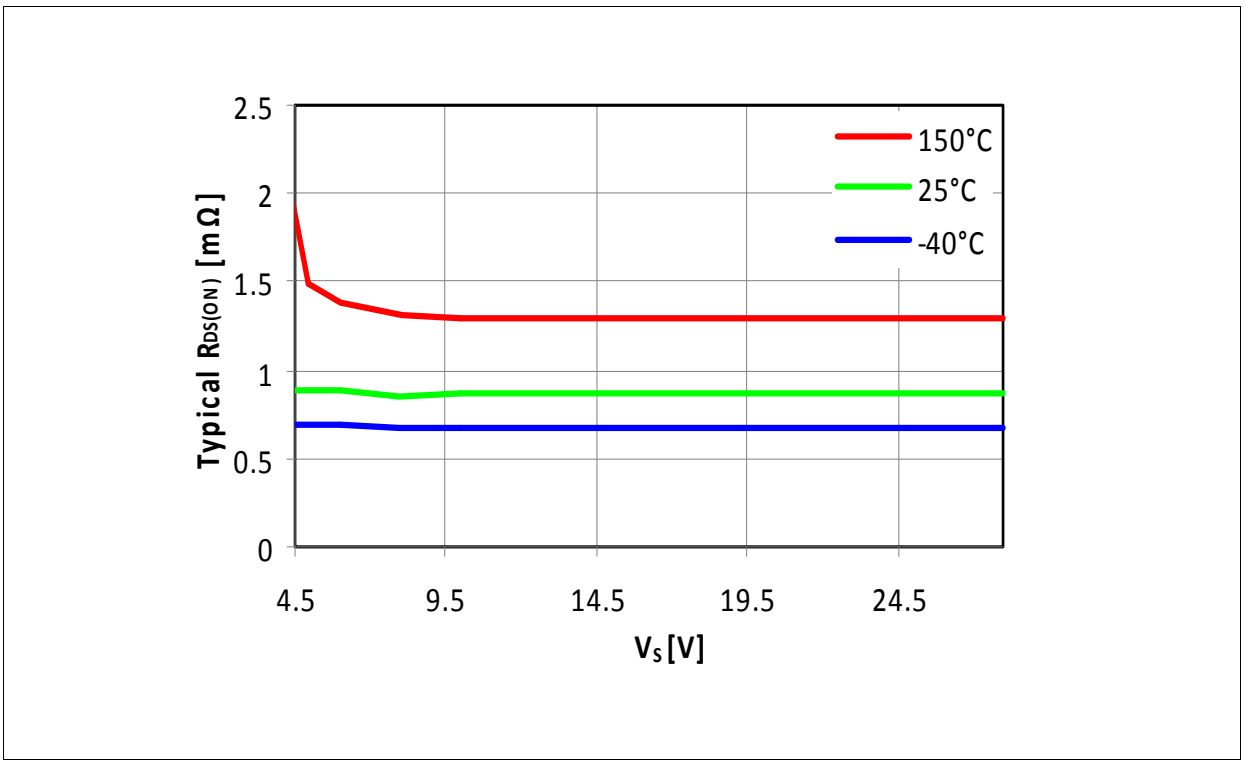


Figure 16 Typical $R_{DS(ON)}$ of BTC50010-1TAA vs. V_S

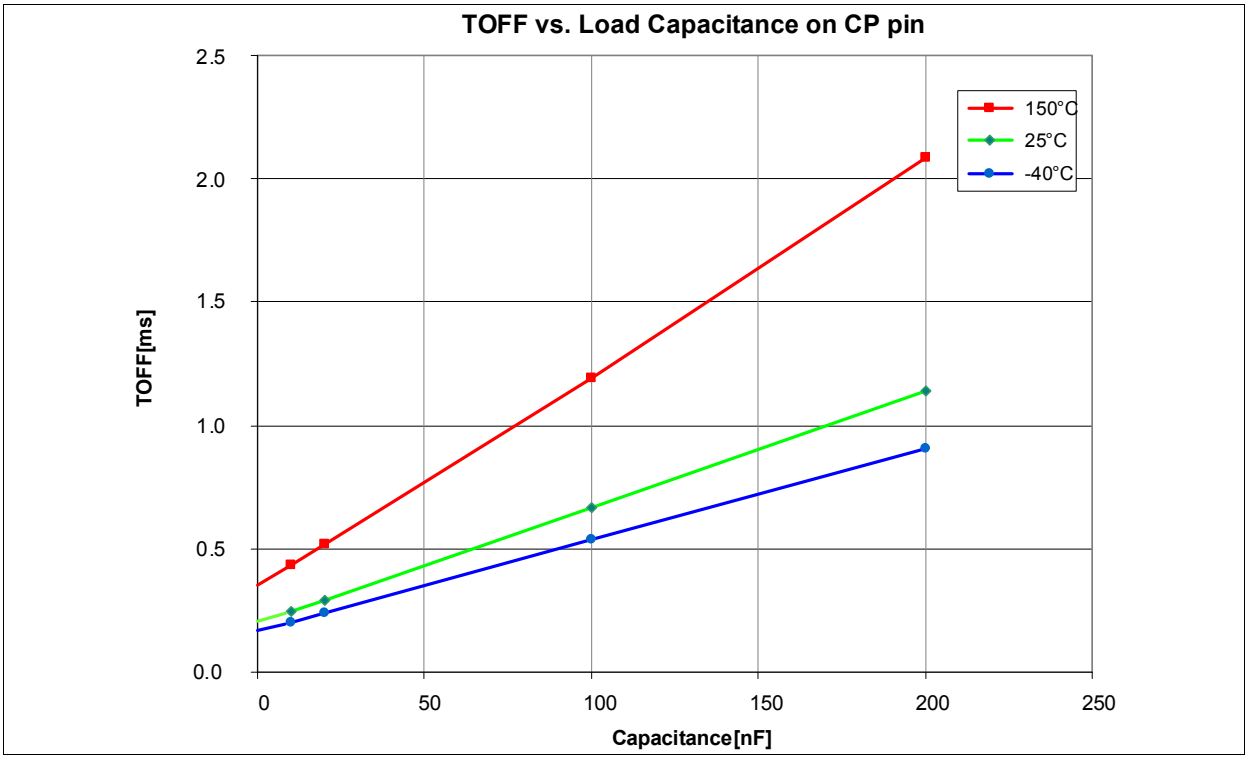


Figure 17 Typical t_{OFF} of BTC50010-1TAA by Driving External Capacitance on CP Pin

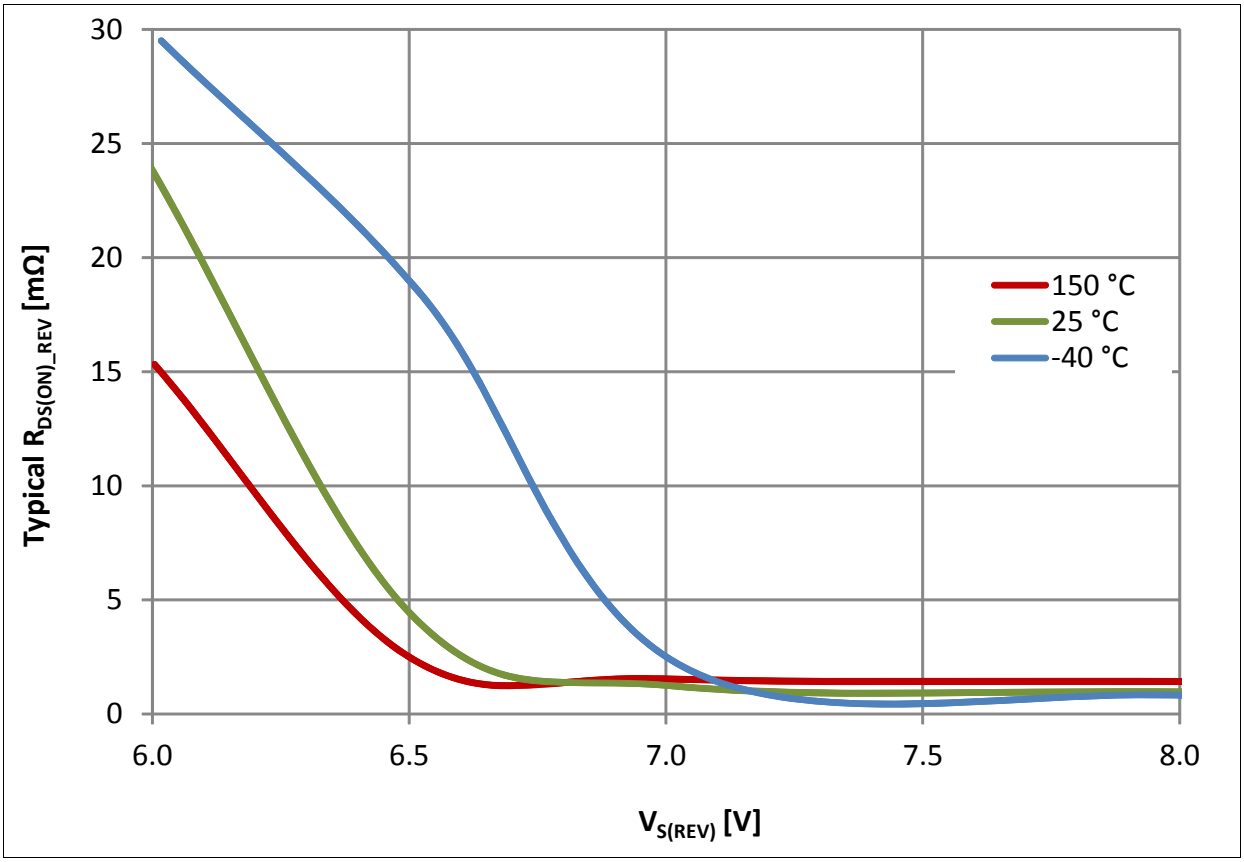


Figure 18 Typical $R_{DS(ON)\_REV}$ of BTC50010-1TAA vs. $V_{S(REV)}$ with V_{IN} = 0V in Reverse Mode for lower values of $V_{S(REV)}$

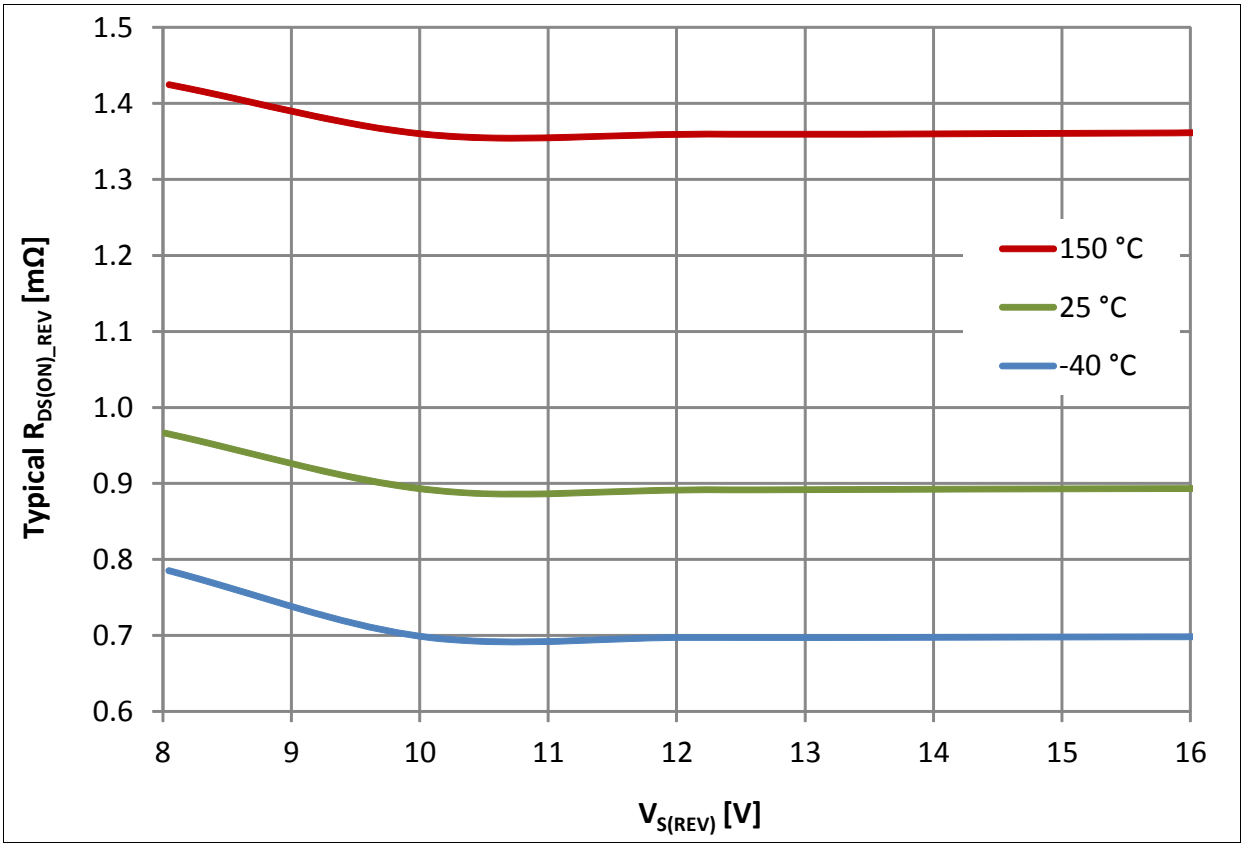


Figure 19 Typical $R_{DS(ON)\_REV}$ of BTC50010-1TAA vs. $V_{S(REV)}$ with V_{IN} = 0V in Reverse Mode for higher values of $V_{S(REV)}$

6 Application Information

This chapter describes how the IC can be used in the application environment.

Note: The following application information is only given as a hint for the implementation of the device in the application and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

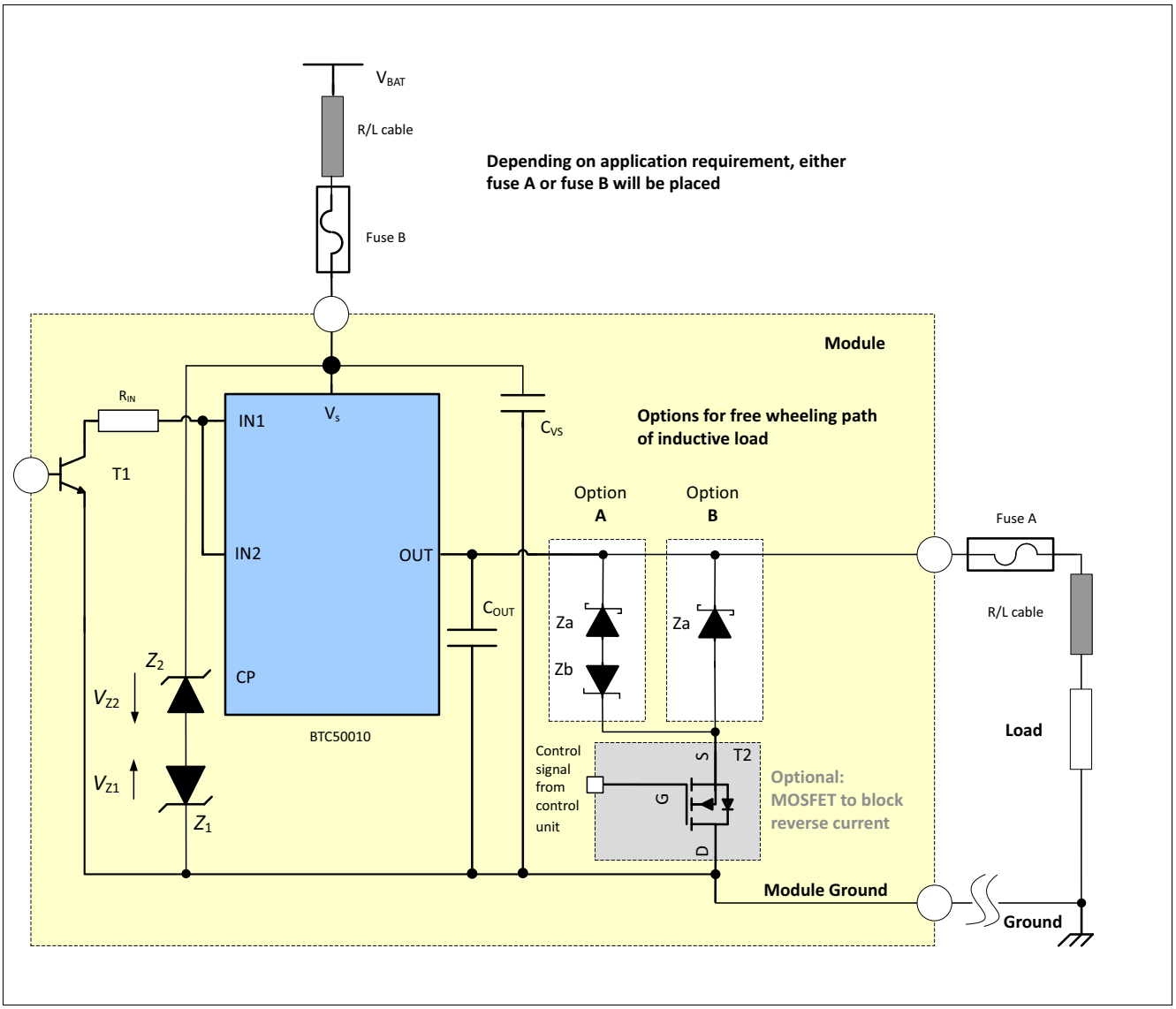


Figure 20 Application Diagram with BTC50010-1TAA

Table 9 Bill of material

Reference	Value	Purpose
T_1	NPN or MOSFET transistor	NPN (e.g. BCR133) or MOSFET (e.g. BSS123) transistor suitable for 5V voltage range controlled by control unit for driving the BTC50010-1TAA
R_{IN}	100 Ω	Protection of BTC50010-1TAA and the microcontroller or control unit during over voltage and reverse polarity, which could be created by huge negative pulse (like ISO pulse 1)

Table 9 Bill of material (cont'd)

Reference	Value	Purpose
Z_1 and Z_2	Zener diodes	Protection of the BTC50010-1TAA during loss of load (correspond to fuse blow on fuse A) or loss of battery (correspond to fuse blow on fuse B) or against huge negative pulse (like ISO pulse 1), please refer to **Figure 12** and **Figure 13**.
Z_a and/or Z_b	Schottky diode Zener transient suppressor	Protection of BTC50010-1TAA when driving an inductive load, stand alone (option B) or together with Z_b (option A). Protection of BTC50010-1TAA when driving an inductive load, to be used together with Z_a in option A to accelerate the demagnetization process.
T_2	MOSFET transistor	Added optionally only for blocking the reverse current in free wheeling path, needed only for option A or B.
FUSE	e.g. 30A ATO FUSE	Protection of the BTC50010-1TAA , wire harness and the load during short circuit. Depending on application requirement, either fuse A or fuse B will be placed.
C_{VS}	100 nF	Improve EMC behavior (in layout, please place it close to the pin)
C_{OUT}	10 nF	Improve EMC behavior (in layout, please place it close to the pins)

6.1 Information for Application Combining PWM Mode with Fuse

The maximum of average power dissipation [1)]P_{loss} is not allowed to be exceeded. Above all, the condition of t_{DC} > $t_{fuseblow\_max}$ must be fulfilled. The $t_{fuseblow\_max}$ is the maximum fuse blow time at certain fuse blow current on the I/t curve of the selected fuse for certain application. During short circuit, the load current could rise up to multiple of the nominal current value until fuse blow. The t_{DC} is defined in **Figure 21**.

P_{loss} = (switching_ON_energy + switching_OFF_energy + I_L^2 * $R_{DS(ON)}$ * t_{DC}) / t_{period}

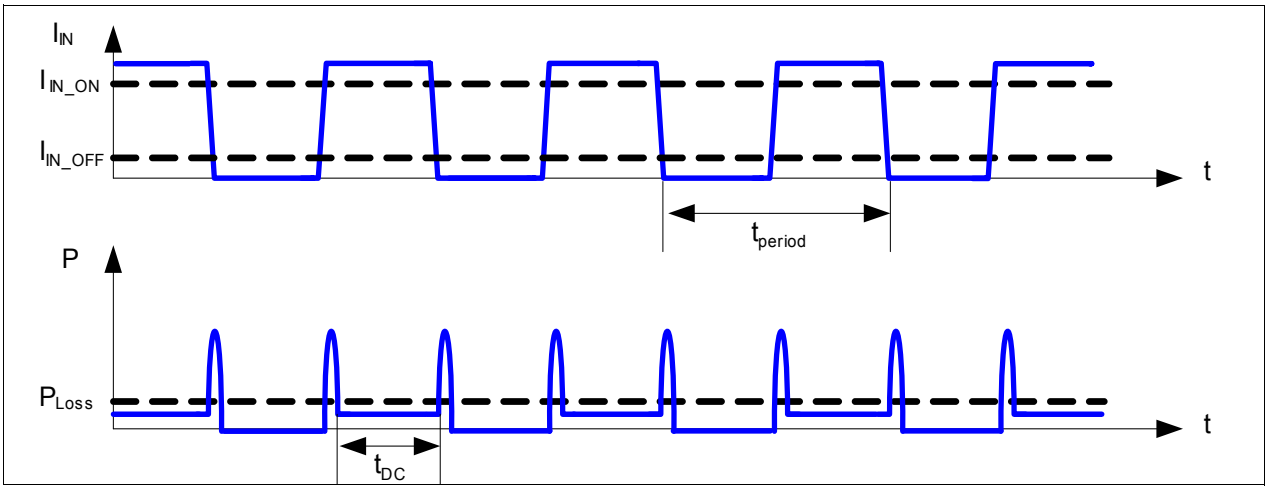


Figure 21 Definition of Average Power Dissipation of BTC50010-1TAA

1) In real application with $R_{thj,a}$ and T_{amb} the maximum allowed average power dissipation is defined: P_{loss}=(150°C - T_{amb}) / $R_{thj,a}$

6.2 Information for Driving Capability of Charge Pump Pin after Switch ON

Curve below shows typical driving capability of the charge pump, which has a dependency on gate voltage and battery voltage. It defines the relevant range of charge pump current for driving the gate capacity of the external MOSFET device and/or an external capacity C_{CP}.

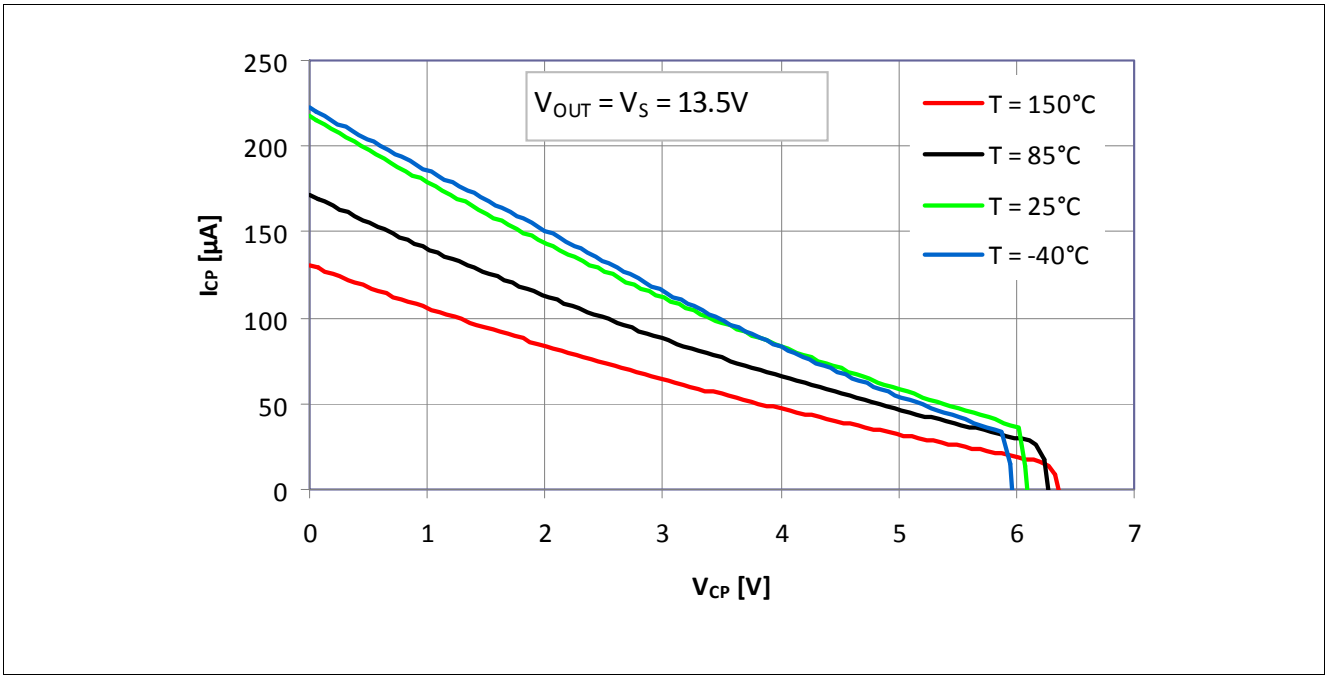


Figure 22 Typical Charge Pump Current Driving Capability vs. Gate-Source Voltage (V_{CP})

6.3 Further Application Information

- Please contact us for information regarding the pin FMEA
- For further information you may contact **http://www.infineon.com/**

7 Package Outlines

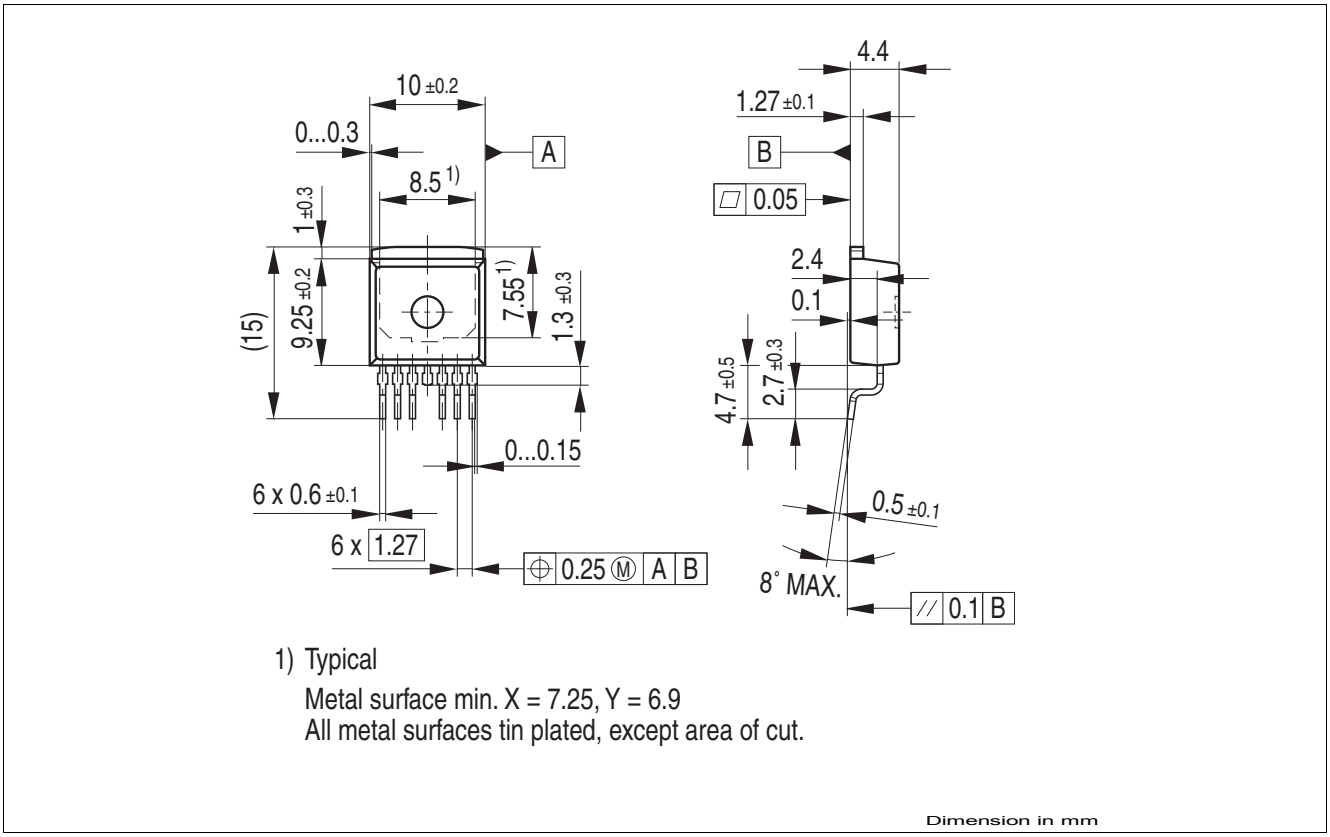


Figure 23 PG-TO-263-7-8 (RoHS compliant)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

BTC50010-1TAA meets the MSL 1 (Moisture Sensitivity Level 1) according to IPC/JEDEC J-STD-020D and can withstand until 245°C peak reflow process.

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

8 Revision History

Revision	Date	Changes
1.0	2011-12-21	Data Sheet released
1.1	2012-06-15	Page 3, Application: in the first bullet point, “inductive” removed Page 8, parameter N_{IND} (P_4.1.10) removed Page 8, parameter N_0 (P_4.1.09) renamed as P_4.1.10 Page 8, parameter I_D (P_4.1.9) added Page 9, parameter E_{AR} (P_4.1.12) removed Page 10, Figure 4 modified, E_{AR} curve removed Page 10, Figure 5 removed Page 15, Chapter 5.1.2 title modified note added Page 19 ~ 20, Chapter 5.5 description modified Page 19, Figure 13 modified Page 20, Figure 14 and Figure 15 modified Page 21, Figure 16 modified Page 25, Figure 20 modified Page 26, Figure 21 modified Page 27, Figure 22 and Figure 23 modified Page 30, Figure 26 modified Page 30, Table 9: third row, first column, Z_2 added; third row, third column, “inductive” removed, “please refer to Figure 13 and Figure 14“added. Page 31, Figure 27 and Table 10 added Page 31, Note “The following application information represents only as a recommendation for switching an inductive load. The function must be verified in the real application” added
1.2	2012-11-16	Page 8, Note “When driving resistive loads with remaining wire or parasitic inductances it must be ensured, that the device will not enter clamping mode during normal operating” added

Revision	Date	Changes
1.3	2015-01-26	Comprehensive rework of rev. 1.2; several figures have been renumbered **Chapter 1**: Overview **Table 1** removed wording “over life time”, updated various symbols **Applications**: first, third and fourth bullet: changed wording **Features**: Change of wording **Description**: Change of wording **Chapter 3.2**: Updated Footnote 2 **Chapter 3.3**:**Figure 3** Change V_{OUTIN} to V_{OUT-IN} **Chapter 4**: Removed Note **Chapter 4.1**: P_4.1.3: changed figure reference P_4.1.6: Change V_{OUTIN} to V_{OUT-IN} P_4.1.8: removed cross reference P_4.1.10: removed from table P_4.1.11: removed from table P_4.1.18: Change symbol name to V_{ESD_out} **Table 2**: Correction within footnote 5 **Page 10**: Footnote 1 modified Removed figure about Total Energy Capability for Switch Off Inductive Loads Reduced figures about Current Robustness **Chapter 4.3 Page 13**: modified text **Chapter 5.1.2**: Completely reworked subchapter **Chapter 5.2**: Change of wording, removed remarks about energy capability. **Chapter 5.5**: modified **Figure 12**, **Figure 13** **Chapter 5.6**: modified text about negative load current, new footnote (1) about definition of LOW and HIGH state **Chapter 5.7**: modified **Figure 15** **Chapter 5.8** P_5.8.11 add max. value P_5.8.12, P_5.8.13, P_5.8.14, P_5.8.15: add typical value **Figure 17** modified **Figure 18**, **Figure 19** new generated out of former figure **Chapter 6**: Reworked text and note; removed figure 20, 21, 22, 23 list of required external components New **Figure 20**, updated **Table 9** Removed former chapter 6.3 (now within **Chapter 6**) **Chapter 6.1**: **Figure 21** and text modified

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