



June 2014

## 74LVX08

### Low Voltage Quad 2-Input AND Gate

#### Features

- Input Voltage Level Translation from 5 V to 3 V
- Ideal for Low-power / Low-Noise 3.3 V Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic threshold Performance

#### Description

The LVX08 contains four 2-input AND gates. The inputs tolerate voltages up to 7 V allowing the interface of 5 V systems to 3 V systems.

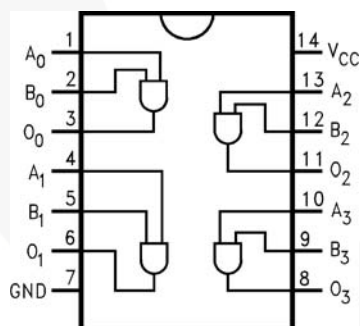
#### Ordering Information

Part Number	Top Mark	Package	Packing Method	Packing Description
74LVX08M	LVX08	SOIC 14L	Rail	14-Lead Small Outline Integrated Circuit, JEDEC MS-012, 0.150 inch Narrow
74LVX08MX	LVX08	SOIC 14L	Tape and Reel	14-Lead Small Outline Integrated Circuit, JEDEC MS-012, 0.150 inch Narrow
74LVX08MTCX	LVX08	TSSOP 14L	Tape and Reel	14-Lead Thin Shrink Small Outline Package, JEDEC MO-153, 4.4 mm Wide

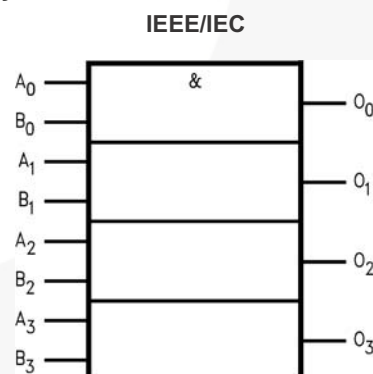


All packages are lead free per JEDEC: J-STD-020B standard.

#### Connection Diagram



#### Logic Symbol



#### Pin Description

Pin Names	Description
A <sub>n</sub> , B <sub>n</sub>	Inputs
O <sub>n</sub>	Outputs

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Rating
$V_{CC}$	Supply Voltage		-0.5 V to 7.0 V
$I_{IK}$	DC Input Diode Current, $V_I = -0.5$ V		-20 mA
$V_I$	DC Input Voltage		-0.5 V to 7.0 V
$I_{OK}$	DC Output Diode Current	$V_O = -0.5$ V	-20 mA
		$V_O = V_{CC} + 0.5$ V	+20 mA
$V_O$	DC Output Voltage		-0.5 V to $V_{CC} + 0.5$ V
$I_O$	DC Output Source or Sink Current		$\pm 25$ mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current		$\pm 50$ mA
$T_{STG}$	Storage Temperature		-65°C to 150°C
$P$	Power Dissipation		180 mW
$T_L$	Lead Temperature (Soldering, 10 seconds)		240°C

## Recommended Operating Conditions<sup>(1)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	2.0 V to 3.6 V
$V_I$	Input Voltage	0 V to 5.5 V
$V_O$	Output Voltage	0 V to $V_{CC}$
$T_A$	Operating Temperature	-40°C to 85°C
$\Delta t / \Delta V$	Input Rise and Fall Time	0 ns/V to 100 ns/V

### Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
V <sub>IH</sub>	HIGH Level Input Voltage	2.0		1.5			1.5		V
		3.0		2.0			2.0		
		3.6		2.4			2.4		
V <sub>IL</sub>	LOW Level Input Voltage	2.0				0.5		0.5	V
		3.0				0.8		0.8	
		3.6				0.8		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	2.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -50 μA	1.9	2.0		1.9		V
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -50 μA	2.9	3.0		2.9		
			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -4 mA	2.58			2.48		
V <sub>OL</sub>	LOW Level Output Voltage	2.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = -50 μA		0.0	0.1		0.1	V
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = -50 μA		0.0	0.1		0.1	
			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = -4 mA			0.36		0.44	
I <sub>IN</sub>	Input Leakage Current	3.6	V <sub>IN</sub> = 5.5 V or GND			±0.1		±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	3.6	V <sub>IN</sub> = V <sub>CC</sub> or GND			2.0		20.0	μA

Noise Characteristics<sup>(2)</sup>

Symbol	Parameter	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	T <sub>A</sub> = 25°C		Unit
				Typ.	Limit	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	50	0.3	0.5	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	50	-0.3	-0.5	V
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	3.3	50		2.0	V
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage	3.3	50		0.8	V

**Note:**2. Input t<sub>r</sub> = t<sub>f</sub> = 3 ns

**AC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time	2.7	15		6.3	11.4	1.0	13.5	ns
			50		8.8	14.9	1.0	17.0	
		3.3 ± 0.3	15		4.8	7.1	1.0	8.5	
			50		7.3	10.6	1.0	12.0	
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew <sup>(3)</sup>	2.7	50			1.5		1.5	ns
		3.3				1.5		1.5	

**Note:**

3. Parameter guaranteed by design t<sub>OSLH</sub> = | t<sub>PLHm</sub> - t<sub>PLHn</sub> |, t<sub>OSHL</sub> = | t<sub>PHLm</sub> - t<sub>PHLn</sub> |.

**Capacitance**

Symbol	Parameter	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Unit
		Min.	Typ.	Max.	Min.	Max.	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance <sup>(4)</sup>		18				pF

**Note:**

4. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}}{4 \text{ (per Gate)}}$

## Physical Dimensions

## SOIC 14L

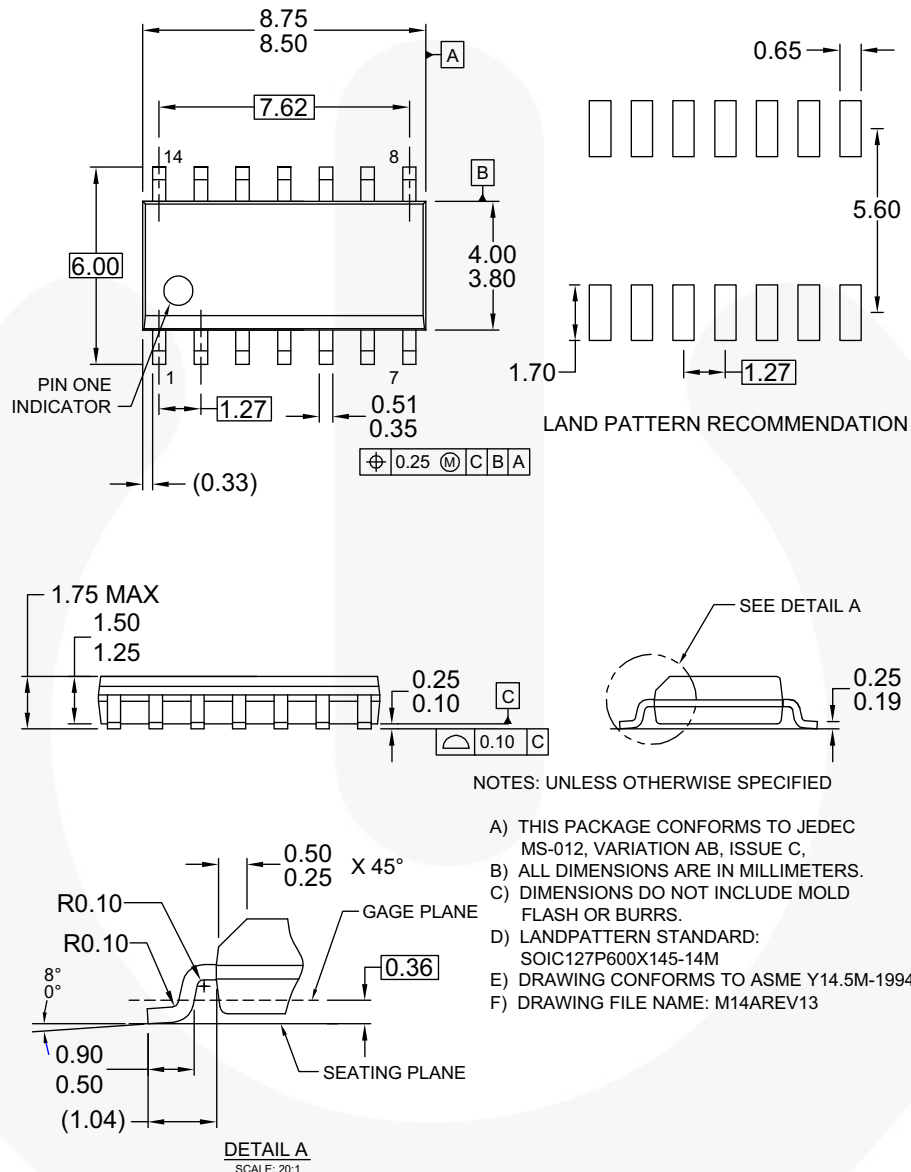


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 inch Narrow

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Technical drawing of a 14-pin micro connector. The drawing includes three views: a top view, a side view, and a detail view of the lead tip.

**Top View Dimensions:**

- Overall width:  $5.0 \pm 0.1$  mm (-A-)
- Pin pitch: 0.43 TYP
- Pin 14 to centerline: 6.4 mm
- Pin 8 to centerline: 3.2 mm
- Overall height:  $4.4 \pm 0.1$  mm (-B-)
- Pin 1 to centerline: 3.2 mm
- Pin 7 to centerline: 3.2 mm

**Side View Dimensions:**

- Overall height: 1.2 MAX
- Pin 14 to centerline: 0.90  $^{+0.15}_{-0.10}$  mm
- Pin 8 to centerline: 0.10  $\pm 0.05$  mm
- Pin 1 to centerline: 0.65 mm
- Pin 7 to centerline: 0.19 - 0.30 mm

**Callouts and Notes:**

- PIN #1 IDENT.
- ALL LEAD TIPS
- 0.2 C B A
- 0.1 C
- 0.13 M A B C
- 0.09-0.20
- SEE DETAIL A
- LAND PATTERN RECOMMENDATION
- DETAIL A
- 12.00° TOP & BOTTOM
- GAGE PLANE
- SEATING PLANE
- 0.25
- 0.6  $\pm 0.1$
- 1.00
- 0°-8°
- R0.09 min

**NOTES:**

- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- DIMENSIONS ARE IN MILLIMETERS

**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-153,  
VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,  
AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI  
Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

**Figure 2. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide**

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