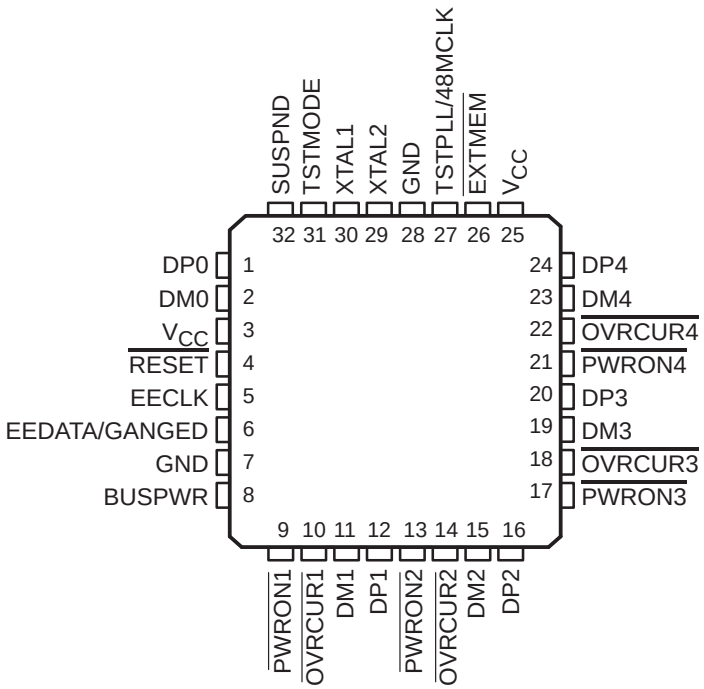
- **Universal Serial Bus (USB) Version 1.1 Compliant**
- **32-Pin LQFP† Package With a 0.8 mm Pin Pitch**
- **3.3-V Low Power ASIC Logic**
- **Integrated USB Transceivers**
- **State Machine Implementation Requires No Firmware Programming**
- **One Upstream Port and Four Downstream Ports**
- **All Downstream Ports Support Full-Speed and Low-Speed Operations**
- **Two Power Source Modes**
  - **Self-Powered Mode**
  - **Bus-Powered Mode**
- **Power Switching and Over-current Reporting Is Provided Ganged or Per Port**
- **Supports Suspend and Resume Operations**
- **Supports Programmable Vendor ID and Product ID With External Serial EEPROM**
- **3-State EEPROM Interface Allows EEPROM Sharing**
- **Push-Pull Outputs for $\overline{\text{PWRON}}$ Eliminate the Need for External Pullup Resistors**
- **Noise Filtering on $\overline{\text{OVRCUR}}$ Provides Immunity to Voltage Spikes**
- **Package Pinout Allows 2-Layer PCB**
- **Low EMI Emission Achieved by a 6-MHz Crystal Input**
- **Migrated From Proven TUSB2040 Hub**
- **Lower Cost Than the TUSB2040 Hub**
- **Enhanced System ESD Performance**
- **Supports 6 MHz Operation Through a Crystal Input or a 48 MHz Input Clock**

**VF PACKAGE**
**(TOP VIEW)**




## description

The TUSB2046B is a 3.3-V CMOS hub device that provides one upstream port and four downstream ports in compliance with the 1.1 Universal Serial Bus (USB) specification. Because this device is implemented with a digital state machine instead of a microcontroller, no firmware programming is required. Fully compliant USB transceivers are integrated into the ASIC for all upstream and downstream ports. The downstream ports support both full-speed and low-speed devices by automatically setting the slew rate according to the speed of the device attached to the ports. The configuration of the BUSPWR pin selects either the bus-powered or the self-powered mode.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

†JEDEC descriptor S-PQFP-G for low profile quad flat pack (LQFP).

## description (continued)

Configuring the GANGED input determines the power switching and over-current detection modes for the downstream ports. External power management devices such as the TPS2044 are required to control the 5-V source to the downstream ports according to the corresponding values of the $\overline{\text{PWRON}}$ pin. Upon detecting any over-current conditions, the power management device sets the corresponding $\overline{\text{OVRCUR}}$ pin of the TUSB2046B to a logic low. If GANGED is high, all $\overline{\text{PWRON}}$ outputs switch together and if any $\overline{\text{OVRCUR}}$ is activated, all ports transition to power off state. If GANGED is low, the $\overline{\text{PWRON}}$ outputs and $\overline{\text{OVRCUR}}$ inputs operate on a per port basis.

The TUSB2046B provides the flexibility of using a 6-MHz or a 48-MHz clock. The logic level of the TSTMODE terminal controls the selection of the clock source. When TSTMODE is low, the output of the internal APLL circuitry is selected to drive the internal core of the chip. When TSTMODE is high, the TSTPLL/48MCLK input is selected as the input clock source and the APLL circuitry is powered down and bypassed. The internal oscillator cell is also powered down while TSTMODE is high.

Low EMI emission is achieved because the TUSB2046B is able to utilize a 6 MHz crystal input. Connect the crystal as shown in Figure 6. An internal PLL then generates the 48 MHz clock used to sample data from the upstream port and to synchronize the 12 MHz used for the USB clock. If low power suspend and resume are desired, a passive crystal or resonator must be used. However, a 6-MHz oscillator may be used by connecting the output to the XTAL1 terminal and leaving the XTAL2 terminal open. The oscillator TTL output must not exceed 3.6 V.

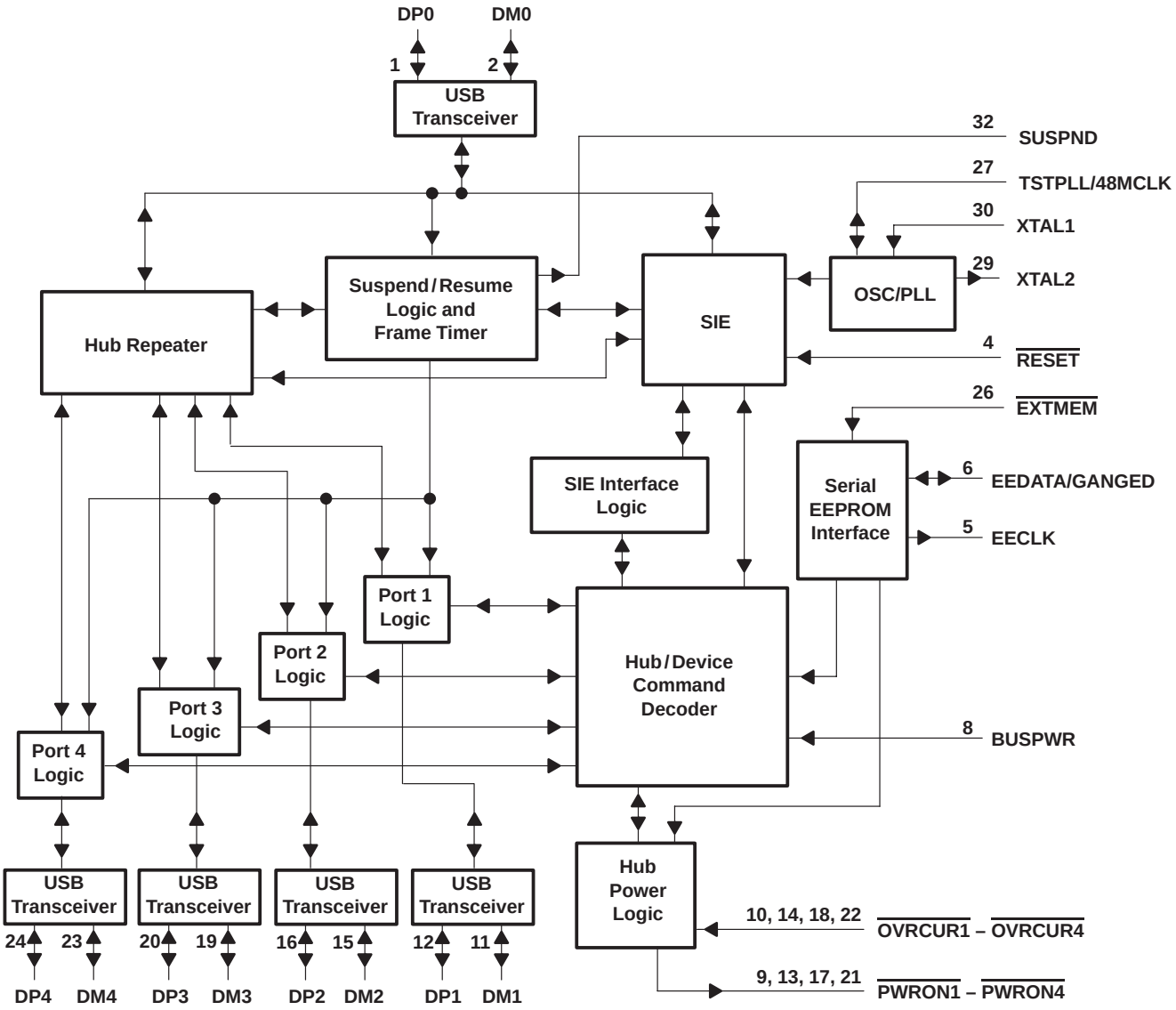
For 48-MHz operation, the clock can not be generated with a crystal, using the XTAL2 output, since the internal oscillator cell only supports fundamental frequency.

Refer to Figure 7 and Figure 8 in the *input clock configuration* section for more detailed information regarding input clock configuration.

The $\overline{\text{EXTMEM}}$ pin enables or disables the optional EEPROM interface. When the $\overline{\text{EXTMEM}}$ pin is high, the product ID (PID) displayed during enumeration is the general-purpose USB hub. For this default, pin 5 is disabled and pin 6 functions as the GANGED input pin. If custom PID and Vendor ID (VID) descriptors are desired, the $\overline{\text{EXTMEM}}$ pin must be low ($\overline{\text{EXTMEM}}$ = 0). For this configuration, pin 5 and pin 6 function as the EEPROM interface with pin 5 and pin 6 functioning as the EECLK and EEDATA, respectively. See Table 1 for a description of the EEPROM memory map.

Other useful features of the TUSB2046B include a package with a 0.8 mm pin pitch for easy PCB routing and assembly, push-pull outputs for the $\overline{\text{PWRON}}$ pins eliminate the need for pullup resistors required by traditional open collector I/Os, and $\overline{\text{OVRCUR}}$ pins have noise filtering for increased immunity to voltage spikes.

## functional block diagram



## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| BUSPWR | 8 | I | Power source indicator. BUSPWR is an active high input that indicates whether the downstream ports source their power from the USB cable or a local power supply. For the bus-power mode, this pin should be pulled to 3.3 V, and for the self-powered mode, this pin should be pulled low. Input must not change dynamically during operation. |
| DM0 | 2 | I/O | Root port USB differential data minus. DM0 paired with DP0 constitutes the upstream USB port. |
| DM1 – DM4 | 11, 15, 19, 23 | I/O | USB differential data minus. DM1 – DM4 paired with DP1 – DP4 support up to four downstream USB ports. |
| DP0 | 1 | I/O | Root port USB differential data plus. DP0 paired with DM0 constitutes the upstream USB port. |
| DP1 – DP4 | 12, 16, 20, 24 | I/O | USB differential data plus. DP1 – DP4 paired with DM1 – DM4 support up to four downstream USB ports. |
| EECLK | 5 | O | EEPROM serial clock. When $\overline{\text{EXTMEM}}$ is high, the EEPROM interface is disabled. The EECLK pin is disabled and should be left floating (unconnected). When $\overline{\text{EXTMEM}}$ is low, EECLK acts as a 3-state serial clock output to the EEPROM with a 100 μA internal pulldown. |
| EEDATA/ GANGED | 6 | I/O | EEPROM serial data/power management mode indicator. When $\overline{\text{EXTMEM}}$ is high, EEDATA/$\overline{\text{GANGED}}$ selects between gang or per-port power over-current detection for the downstream ports. When $\overline{\text{EXTMEM}}$ is low, EEDATA/GANGED acts as a serial data I/O for the EEPROM and is internally pulled down with a 100 μA pulldown. This standard TTL input must not change dynamically during operation. |
| $\overline{\text{EXTMEM}}$ | 26 | I | EEPROM read enable. When $\overline{\text{EXTMEM}}$ is high, the serial EEPROM interface of the device is disabled. When $\overline{\text{EXTMEM}}$ is low, terminals 5 and 6 are configured as the clock and data pins of the serial EEPROM interface, respectively. |
| GND | 7, 28 | | Ground. GND terminals must be tied to ground for proper operation. |
| $\overline{\text{OVRCUR1}}$ – $\overline{\text{OVRCUR4}}$ | 10, 14, 18, 22 | I | Over-current input. $\overline{\text{OVRCUR1}}$ – $\overline{\text{OVRCUR4}}$ are active low. For per-port over current detection, one over-current input is available for each of the four downstream ports. In the ganged mode, any $\overline{\text{OVRCUR}}$ input may be used and all $\overline{\text{OVRCUR}}$ pins should be tied together. $\overline{\text{OVRCUR}}$ pins are active low inputs with noise filtering logic. |
| $\overline{\text{PWRON1}}$ – $\overline{\text{PWRON4}}$ | 9, 13, 17, 21 | O | Power-on/-off control signals. $\overline{\text{PWRON1}}$ – $\overline{\text{PWRON4}}$ are active low, push-pull outputs. Push-pull outputs eliminate the pullup resistors which open-drain outputs require. However, the external power switches that connect to these pins must be able to operate with 3.3-V inputs because these outputs cannot drive 5-V signals. |
| $\overline{\text{RESET}}$ | 4 | I | Reset. $\overline{\text{RESET}}$ is an active low TTL input with hysteresis and must be asserted at power up. When $\overline{\text{RESET}}$ is asserted, all logic is initialized. Generally, a reset with a pulse width between 100 μs and 1 ms is recommended after 3.3 V $V_{CC}$ reaching its 90%. Clock signal has to be active during the last 60 μs of the reset window. |
| SUSPND | 32 | O | Suspend status. SUSPND is an active high output available for external logic power down operations. During the suspend mode, SUSPND is high. SUSPND is low for normal operation. |
| TSTMODE | 31 | I | Test/mode pin. TSTMODE is used as a test pin during production testing. This pin must be tied to ground or 3.3 V $V_{CC}$ for normal 6 MHz or 48 MHz operation, respectively. |
| TSTPLL/48MCLK | 27 | I/O | Test/48MHz clock input. TSTPLL/48MCLK is used as a test pin during production testing. This pin must be tied to ground for normal 6 MHz operation. If 48 MHz input clock is desired, a 48 MHz clock source (no crystal) can be connected to this input pin. |
| $V_{CC}$ | 3, 25 | | 3.3-V supply voltage |
| XTAL1 | 30 | I | Crystal 1. XTAL1 is a 6-MHz crystal input with 50% duty cycle. An internal PLL generates the 48-MHz and 12-MHz clocks used internally by the ASIC logic. |
| XTAL2 | 29 | O | Crystal 2. XTAL2 is a 6-MHz crystal output. This terminal should be left open when using an oscillator. |

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . –0.5 V to 3.6 V
Input voltage range, $V_I$ . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$, ($V_I$ < 0 V or $V_I$ > $V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$, ($V_O$ < 0 V or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Operating free-air temperature range, $T_A$, TUSB2046B . . . . . 0°C to 70°C
TUSB2046BI . . . . . –40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to GND.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | TUSB2046B | 3 | 3.3 | 3.6 | V |
| | TUSB2046BI | 3.3 | | 3.6 | |
| Input voltage, TTL/LVCMOS, $V_I$ | | 0 | | $V_{CC}$ | V |
| Output voltage, TTL/LVCMOS, $V_O$ | | 0 | | $V_{CC}$ | V |
| High-level input voltage, signal-ended receiver, $V_{IH(REC)}$ | | 2 | | $V_{CC}$ | V |
| Low-level input voltage, signal-ended receiver, $V_{IL(REC)}$ | | | | 0.8 | V |
| High-level input voltage, TTL/LVCMOS, $V_{IH(TTL)}$ | | 2 | | $V_{CC}$ | V |
| Low-level input voltage, TTL/LVCMOS, $V_{IL(TTL)}$ | | 0 | | 0.8 | V |
| Operating free-air temperature, $T_A$ | TUSB2046B | 0 | | 70 | °C |
| | TUSB2046BI | –40 | | 85 | |
| External series, differential driver resistor, $R_{(DRV)}$ | | 22 (–5%) | | 22 (5%) | Ω |
| Operating (dc differential driver) high speed mode, $f_{(OPRH)}$ | | | | 12 | Mb/s |
| Operating (dc differential driver) low speed mode, $f_{(OPRL)}$ | | | | 1.5 | Mb/s |
| Common mode, input range, differential receiver, $V_{(ICR)}$ | | 0.8 | | 2.5 | V |
| Input transition times, $t_t$, TTL/LVCMOS | | 0 | | 25 | ns |
| Junction temperature range, $T_J$ | | 0 | | 115 | °C |

### electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | TTL/LVCMOS | $I_{OH}$ = –4 mA | $V_{CC}$ – 0.5 | | V |
| | | USB data lines | $R_{(DRV)}$ = 15 kΩ, to GND | 2.8 | | |
| | | | $I_{OH}$ = –12 mA (without $R_{(DRV)}$) | $V_{CC}$ – 0.5 | | |
| $V_{OL}$ | Low-level output voltage | TTL/LVCMOS | $I_{OL}$ = 4 mA | | 0.5 | V |
| | | USB data lines | $R_{(DRV)}$ = 1.5 kΩ to 3.6 V | | 0.3 | |
| | | | $I_{OL}$ = 12 mA (without $R_{(DRV)}$) | | 0.5 | |
| $V_{IT+}$ | Positive input threshold voltage | TTL/LVCMOS | | | 1.8 | V |
| | | Single-ended | 0.8 V ≤ $V_{ICR}$ ≤ 2.5 V | | 1.8 | V |
| $V_{IT–}$ | Negative-input threshold voltage | TTL/LVCMOS | | 0.8 | | V |
| | | Single-ended | 0.8 V ≤ $V_{ICR}$ ≤ 2.5 V | 1 | | V |
| $V_{hys}$ | Input hysteresis† ($V_{T+}$ – $V_{T–}$) | TTL/LVCMOS | | 0.3 | 0.7 | V |
| | | Single-ended | 0.8 V ≤ $V_{ICR}$ ≤ 2.5 V | 300 | 500 | mV |
| $I_{OZ}$ | High-impedance output current | TTL/LVCMOS | V = $V_{CC}$ or GND‡ | | ±10 | μA |
| | | USB data lines | 0 V ≤ $V_O$ ≤ $V_{CC}$ | | ±10 | μA |
| $I_{IL}$ | Low-level input current | TTL/LVCMOS | $V_I$ = GND | | –1 | μA |
| $I_{IH}$ | High-level input current | TTL/LVCMOS | $V_I$ = $V_{CC}$ | | 1 | μA |
| $z_{o(DRV)}$ | Driver output impedance | USB data lines | Static $V_{OH}$ or $V_{OL}$ | 7.1 | 19.9 | Ω |
| $V_{ID}$ | Differential input voltage | USB data lines | 0.8 V ≤ $V_{ICR}$ ≤ 2.5 V | 0.2 | | V |
| $I_{CC}$ | Input supply current | | Normal operation | | 40 | mA |
| | | | Suspend mode | | 1 | μA |

† Applies for input buffers with hysteresis
‡ Applies for open drain buffers

### differential driver switching characteristics over recommended ranges of operating free-air temperature and supply voltage, $C_L$ = 50 pF (unless otherwise noted)

#### full speed mode

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_r$ | Transition rise time for DP or DM | See Figure 1 and Figure 2 | 4 | 20 | ns |
| $t_f$ | Transition fall time for DP or DM | See Figure 1 and Figure 2 | 4 | 20 | ns |
| $t_{(RFM)}$ | Rise/fall time matching§ | ($t_r$/$t_f$) × 100 | 90% | 110% | |
| $V_{O(CRS)}$ | Signal crossover output voltage§ | | 1.3 | 2.0 | V |

§ Characterized only. Limits are approved by design and are not production tested.

#### low speed mode

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_r$ | Transition rise time for DP or DM§ | $C_L$ = 200 pF to 600 pF, | See Figure 1 and Figure 2 | 75 | 300 | ns |
| $t_f$ | Transition fall time for DP or DM§ | $C_L$ = 200 pF to 600 pF, | See Figure 1 and Figure 2 | 75 | 300 | ns |
| $t_{(RFM)}$ | Rise/fall time matching§ | ($t_r$/$t_f$) × 100 | | 80% | 120% | |
| $V_{O(CRS)}$ | Signal crossover output voltage§ | $C_L$ = 200 pF to 600 pF | | 1.3 | 2.0 | V |

§ Characterized only. Limits are approved by design and are not production tested.

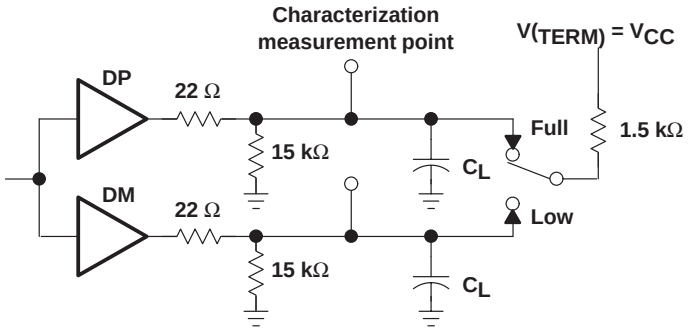
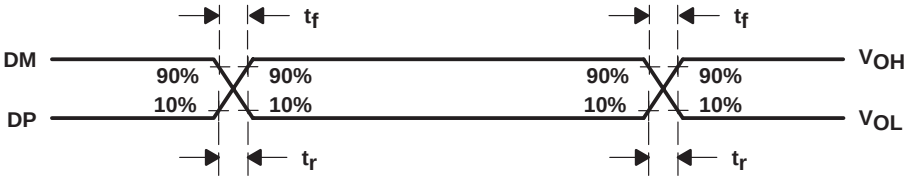



**Figure 1. Differential Driver Switching Load**




NOTE: The $t_r/t_f$ ratio is measured as $t_{r(DP)}/t_{f(DM)}$ and $t_{r(DM)}/t_{f(DP)}$ at each crossover point.

**Figure 2. Differential Driver Timing Waveforms**

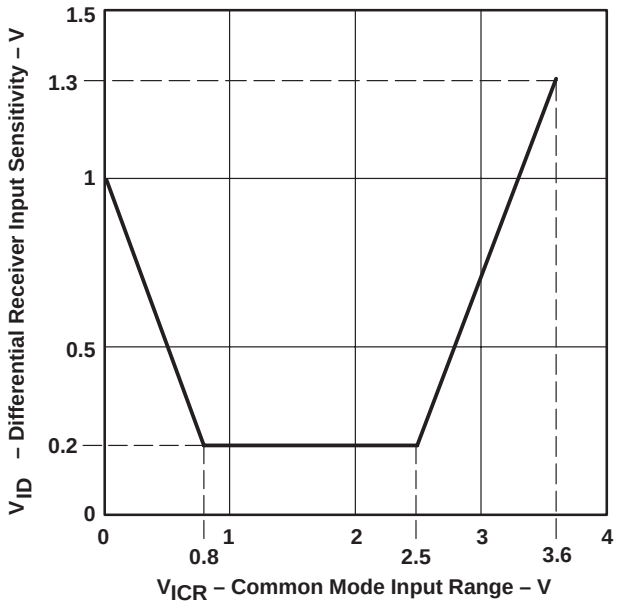



**Figure 3. Differential Receiver Input Sensitivity vs Common Mode Input Range**

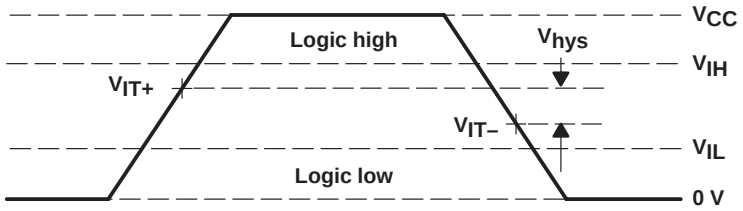



**Figure 4. Single-Ended Receiver Input Signal Parameter Definitions**

## APPLICATION INFORMATION

A major advantage of USB is the ability to connect 127 functions configured in up to six logical layers (tiers) to a single personal computer (see Figure 5).

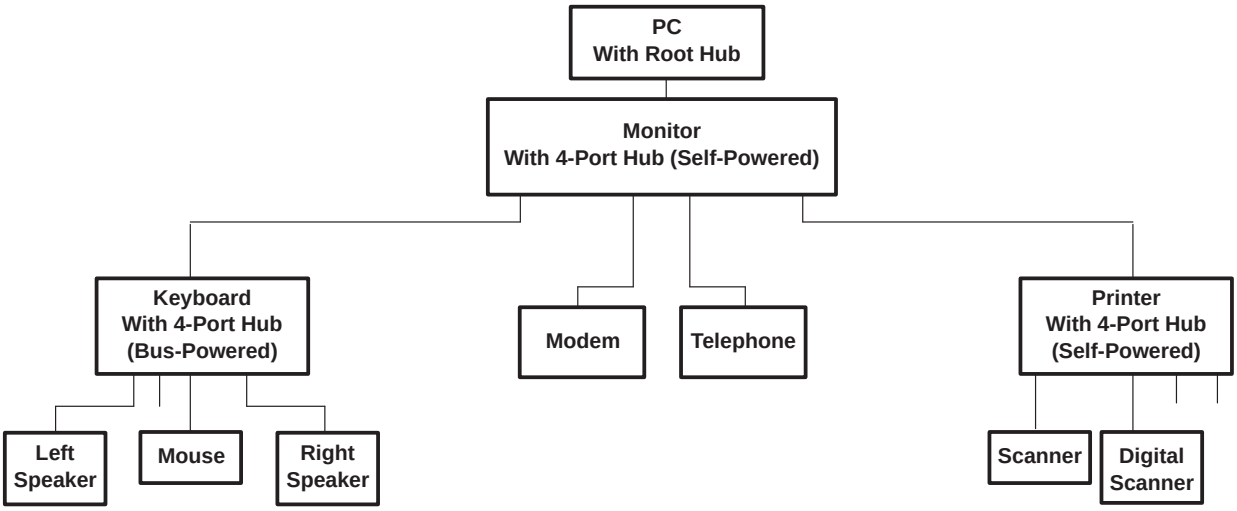



**Figure 5. USB Tiered Configuration Example**

Another advantage of USB is that all peripherals are connected using a standardized four-wire cable that provides both communication and power distribution. The power configurations are bus-powered and self-powered modes. The maximum current that may be drawn from the USB 5-V line during power up is 100 mA. For the bus-powered mode, a hub can draw a maximum of 500 mA from the 5-V line of the USB cable. A bus-powered hub must always be connected downstream to a self-powered hub unless it is the only hub connected to the PC and there are no high-powered functions connected downstream. In the self-powered mode, the hub is connected to an external power supply and can supply up to 500 mA to each downstream port. High-powered functions may draw a maximum of 500 mA from each downstream port and may only be connected downstream to self-powered hubs. Per the USB specification, in the bus-powered mode, each downstream port can provide a maximum of 100 mA of current, and in the self-powered mode, each downstream port can provide a maximum of 500 mA of current.

Both bus-powered and self-powered hubs require over-current protection for all downstream ports. The two types of protection are individual port management (individual port basis) or ganged port management (multiple port basis). Individual port management requires power management devices for each individual downstream port, but adds robustness to the USB system because, in the event of an over-current condition, the USB host only powers down the port that has the condition. The ganged configuration uses fewer power management devices and thus has lower system costs, but in the event of an over-current condition on any of the downstream ports, all the ganged ports are disabled by the USB host.

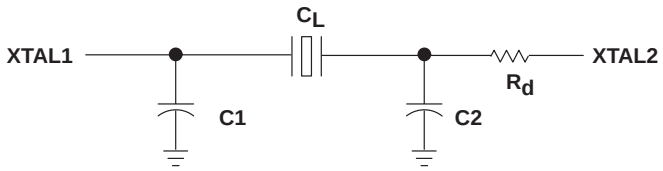
Using a combination of the BUSPWR and EEDATA/GANGED inputs, the TUSB2046B supports four modes of power management: bus-powered hub with either individual port power management or ganged port power management, and the self-powered hub with either individual port power management or ganged port power management. Texas Instruments supplies the complete hub solution because we offer this TUSB2046B, the TUSB2077 (7–port) and the TUSB2140B (4-port with $I^2C$) hubs along with the power management chips needed to implement a fully USB Specification 1.1 compliant system.

## APPLICATION INFORMATION

### USB design notes

The following sections provide block diagram examples of how to implement the TUSB2046B device. Note, even though no resistors are shown, pullup, pulldown and series resistors must be used to properly implement this device.

Figure 6 is an example of how to generate the 6 MHz clock signal.




NOTE A: Figure 6 assumes a 6 MHz fundamental crystal that is parallel loaded. The component values of C1, C2 and $R_d$ are determined using a crystal from Fox Electronics – part number HC49U–6.00MHz30\50\0 ±70\20 which means ±30 ppm at 25°C and 50 ppm from 0°C to 70°C. The characteristics for the crystal include a load capacitance ($C_L$) of 20 pF, maximum shunt capacitance ($C_0$) of 7 pF, and the maximum ESR of 50 Ω. In order to insure enough negative resistance, use C1 = C2 = 27 pF. The resistor $R_d$ is used to trim the gain, and $R_d$ = 1.5 kΩ is recommended.

**Figure 6. Crystal Tuning Circuit**

### input clock configuration

The input clock configuration logic of TUSB2046B is enhanced to accept a 6 MHz crystal or 48 MHz on the board clock source with a simple tie-off change on TSTMODE (pin 31).

- A 6-MHz input clock configuration is shown in Figure 7.
  In this mode, both TSTMODE and TSTPLL/48MCLK terminals must be tied to ground. The hub is configured to use the 6 MHz clock on pin 30 and 29, which are XTAL1 and XTAL2 respectively on TUSB2046B. This is identical to the TUSB2046.

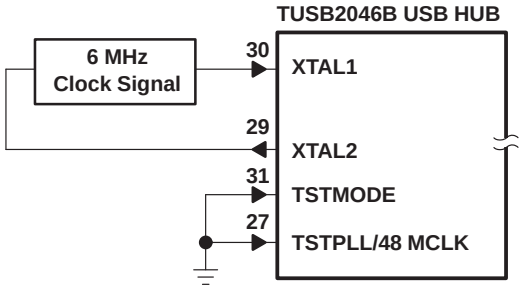



**Figure 7. 6-MHz Input Clock Configuration**

## APPLICATION INFORMATION

### input clock configuration (continued)

- A 48-MHz input clock configuration is shown in Figure 8.
  In this mode, both TSTMODE and XTAL1 terminals must be tied to 3.3 V $V_{CC}$. The hub accepts the 48 MHz clock input on TSTPLL/48MCLK (pin 27). XTAL2 must be left floating (open) for this configuration. Only the oscillator or the onboard clock source is accepted for this mode. A crystal can not be used for this mode, since the chip's internal oscillator cell only supports fundamental frequency.

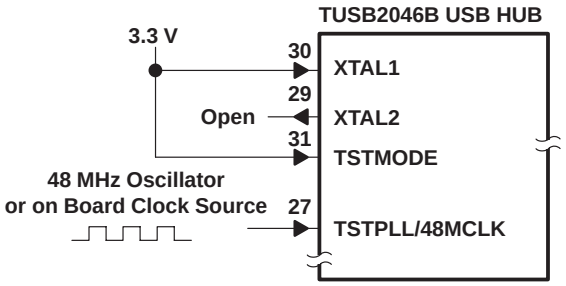



**Figure 8. 48-MHz Input Clock Configuration**

Figure 9 is a block diagram example of how to connect the external EEPROM if a custom product ID and vendor ID are desired.

Figure 10 shows the EEPROM read operation timing diagram. Figures 11, 12, and 13 illustrate how to connect the TUSB2046B device for different power source and port power management combinations.

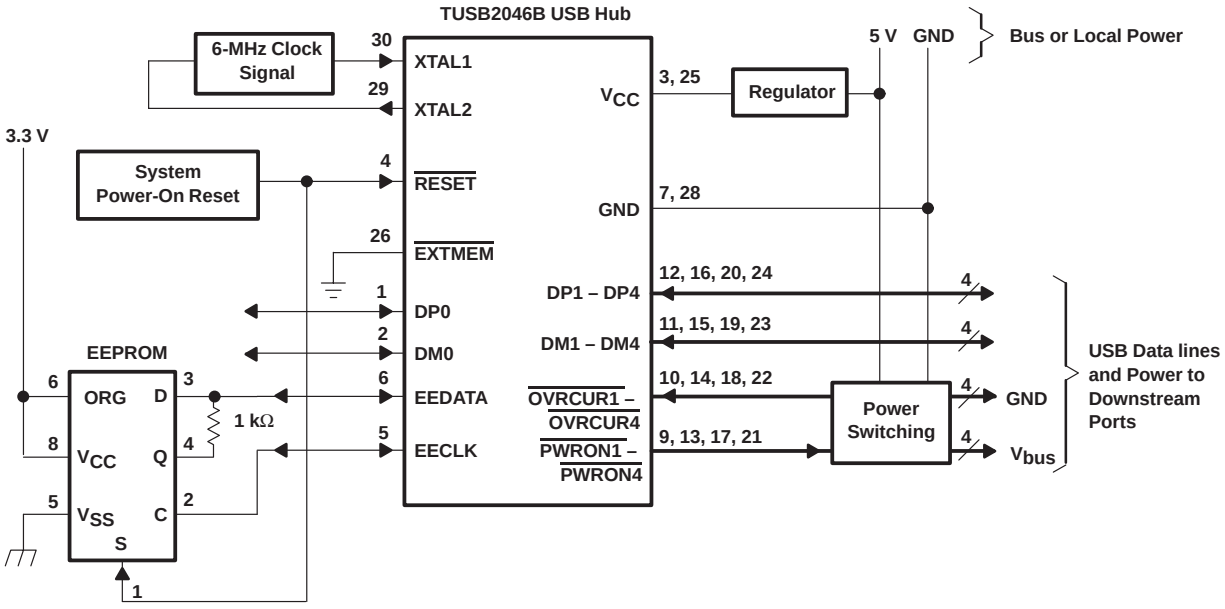



**Figure 9. Typical Application of the TUSB2046B USB Hub**

## APPLICATION INFORMATION

### programming the EEPROM

An SGS Thompson M93C46 EEPROM or equivalent is used for storing the programmable VID and PID. When the EEPROM interface is enabled ($\overline{\text{EXTMEM}}$ = 0), the EECLK and EEDATA are internally pulled down (100 μA) inside the TUSB2046B. The internal pulldowns are disabled when the EEPROM interface is disabled ($\overline{\text{EXTMEM}}$ = 1).

The EEPROM is programmed with the three 16-bit locations as shown in Table 1. Connecting pin 6 of the EEPROM high (ORG = 1) organizes the EEPROM memory into 64×16 bit words.

**Table 1. EEPROM Memory Map**

| ADDRESS | D15 | D14 | D13 | D12–D8 | D7–D0 |
|---|---|---|---|---|---|
| 00000 | 0 | GANGED | 00000 | 00000 | 00000000 |
| 00001 | VID High-byte | | | | VID Low-byte |
| 00010 | PID High-byte | | | | PID Low-byte |
| | XXXXXXXX | | | | |

The D and Q signals of the EEPROM must be tied together using a 1-kΩ resistor with the common I/O operations forming a single-wire bus. After system power-on reset, the TUSB2046B performs a one-time access read operation from the EEPROM if the $\overline{\text{EXTMEM}}$ pin is pulled low and the chip select(s) of the EEPROM is connected to the system power-on reset. Initially, the EEDATA pin will be driven by the TUSB2046B to send a start bit (1) which is followed by the read instruction (10) and the starting-word address (00000). Once the read instruction is received, the instruction and address are decoded by the EEPROM, which then sends the data to the output shift register. At this point, the hub stops driving the EEDATA pin and the EEPROM starts driving. A dummy (0) bit is then output and the first three 16-bit words in the EEPROM are output with the most significant bit (MSB) first.

The output data changes are triggered by the rising edge of the clock provided by the TUSB2046B on the EECLK pin. The *SGS-Thompson M936C46* EEPROM is recommended because it advances to the next memory location by automatically incrementing the address internally. Any EEPROM used must have the automatic internal address advance function. After reading the three words of data from the EEPROM, the TUSB2046B puts the EEPROM interface into a high-impedance condition (pulled down internally) to allow other logic to share the EEPROM. The EEPROM read operation is summarized in Figure 10. For more details on EEPROM operation, refer to *SGS-Thompson Microelectronics M93C46 Serial Microwire Bus EEPROM* data sheet.

## APPLICATION INFORMATION

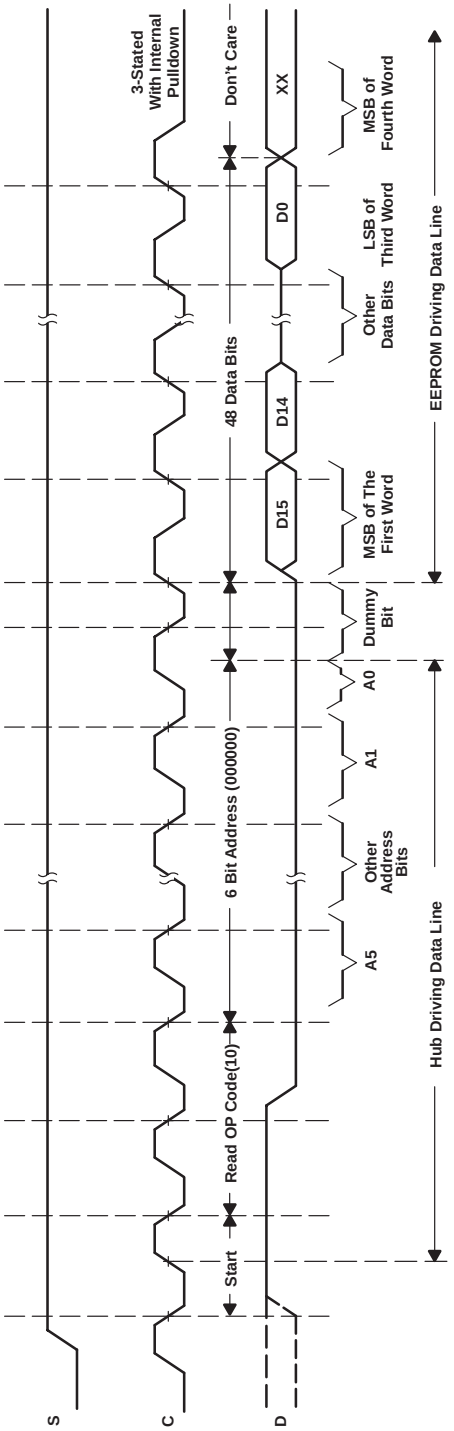
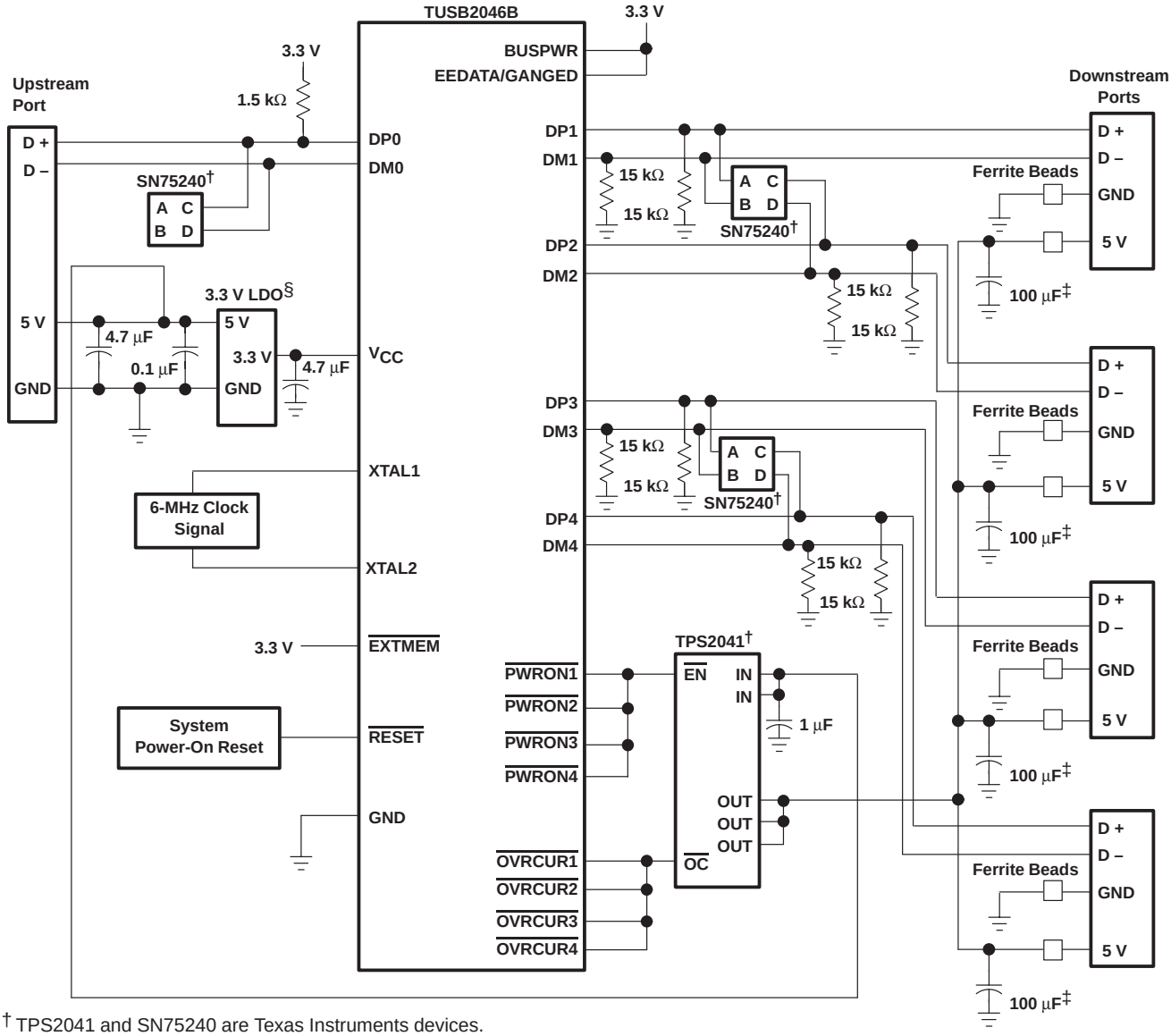



**Figure 10. EEPROM Read Operation Timing Diagram**

## APPLICATION INFORMATION

### bus-powered hub, ganged port power management

When used in bus-powered mode, the TUSB2046B supports up to four downstream ports by controlling a TPS2041 device which is capable of supplying 100 mA of current to each downstream port. Bus-powered hubs must implement power switching to ensure current demand is held below 100 mA when the hub is hot-plugged into the system. Utilizing the TPS2041 for ganged power management provides over-current protection for the downstream ports. The SN75240 transient suppressors reduce inrush current and voltage spikes on the data lines. The $\overline{\text{OVRCUR}}$ signals should be tied together for a ganged operation.



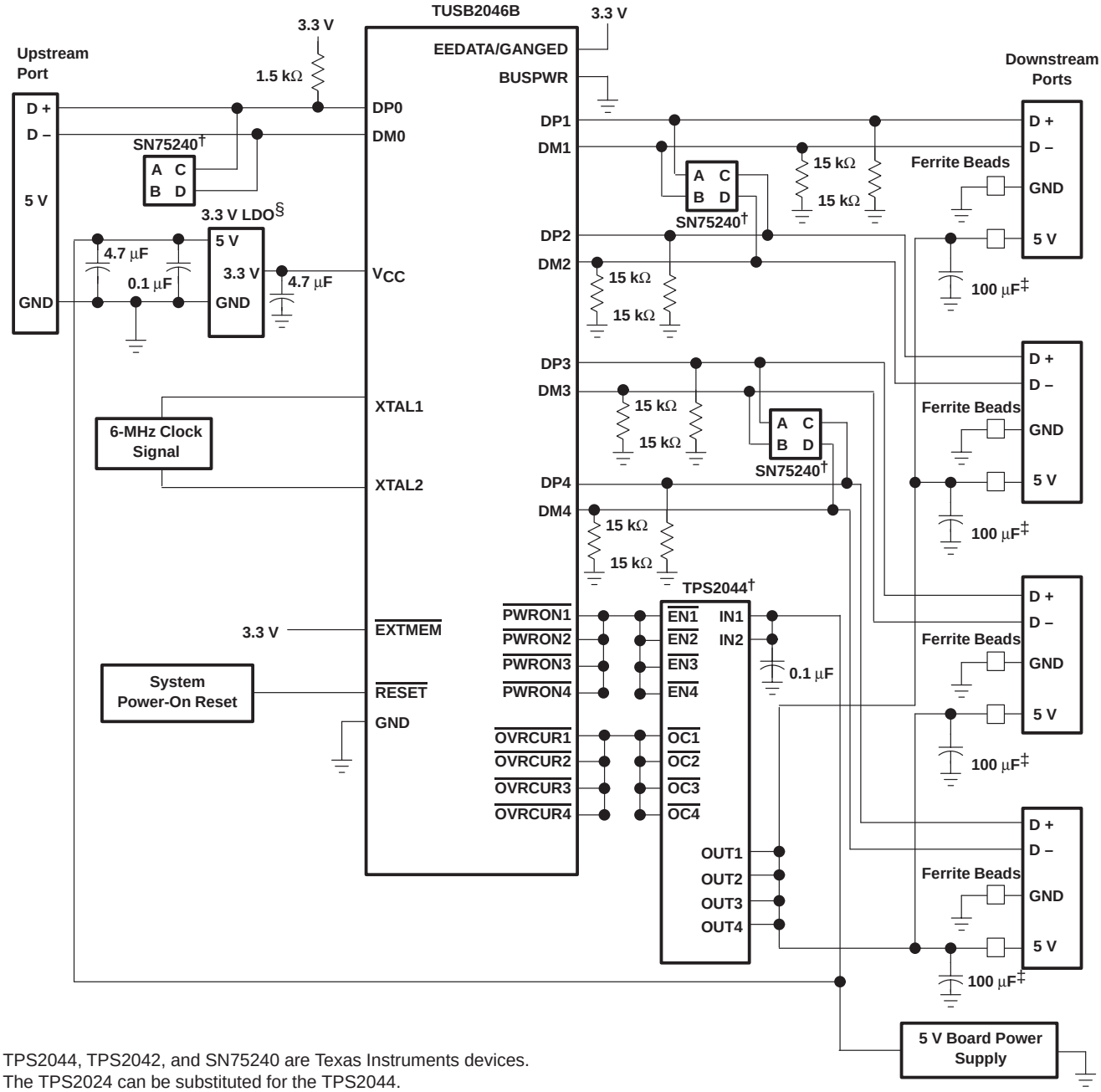

† TPS2041 and SN75240 are Texas Instruments devices.
‡ 120 µF per hub is the minimum required per the USB specification, version 1.1. However, TI recommends a 100 µF low ESR tantalum capacitor per port for immunity to voltage droop.
§ LDO is a 5 V to 3.3 V voltage regulator

**Figure 11. TUSB2046B Bus-Powered Hub, Ganged Port Power Management Application**

## APPLICATION INFORMATION

### self-powered hub, ganged port power management

The TUSB2046B can also be implemented for ganged port power management in a self-powered configuration. The implementation is very similar to the bus-powered example with the exception that a self-powered port supplies 500 mA of current to each downstream port. The over-current protection can be provided by a TPS2044 quad device or a TPS2024 single power switch.




† TPS2044, TPS2042, and SN75240 are Texas Instruments devices. The TPS2024 can be substituted for the TPS2044.

‡ 120 µF per hub is the minimum required per the USB specification, version 1.1. However, TI recommends a 100 µF low ESR tantalum capacitor per port for immunity to voltage droop.

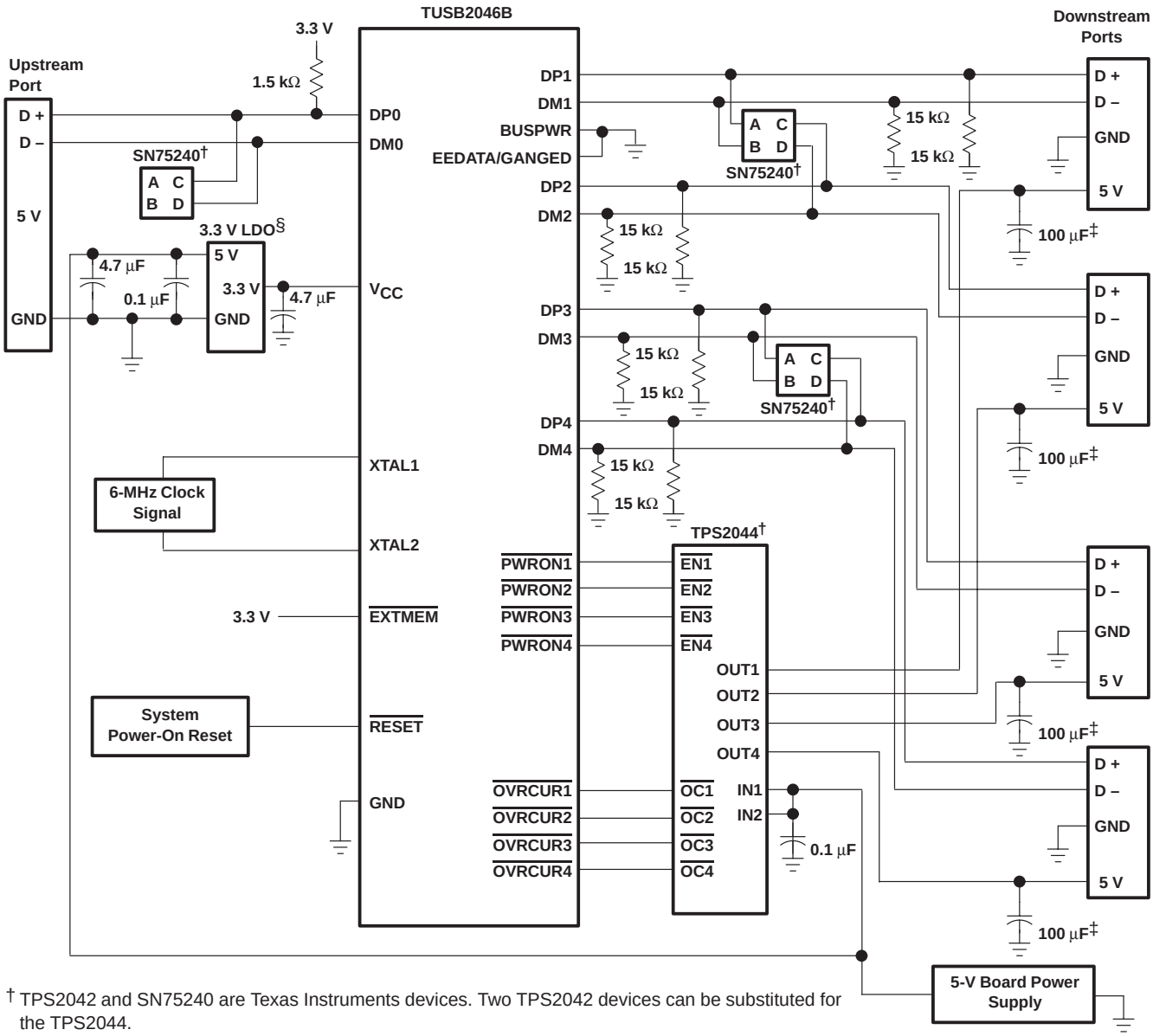
§ LDO is a 5 V to 3.3 V voltage regulator

**Figure 12. TUSB2046B Self-Powered Hub, Ganged Port Power Management Application**

## APPLICATION INFORMATION

### self-powered hub, individual port power management

In a self-powered configuration, the TUSB2046B can be implemented for individual port-power management when used with the TPS2044, because it is capable of supplying 500 mA of current to each downstream port and can provide current limiting on a per port basis. When the hub detects a fault on a downstream port, power is removed from only the port with the fault and the remaining ports continue to operate normally. Self-powered hubs are required to implement over-current protection and report overcurrent conditions. The SN75240 transient suppressors reduce inrush current and voltage spikes on the data lines.




† TPS2042 and SN75240 are Texas Instruments devices. Two TPS2042 devices can be substituted for the TPS2044.

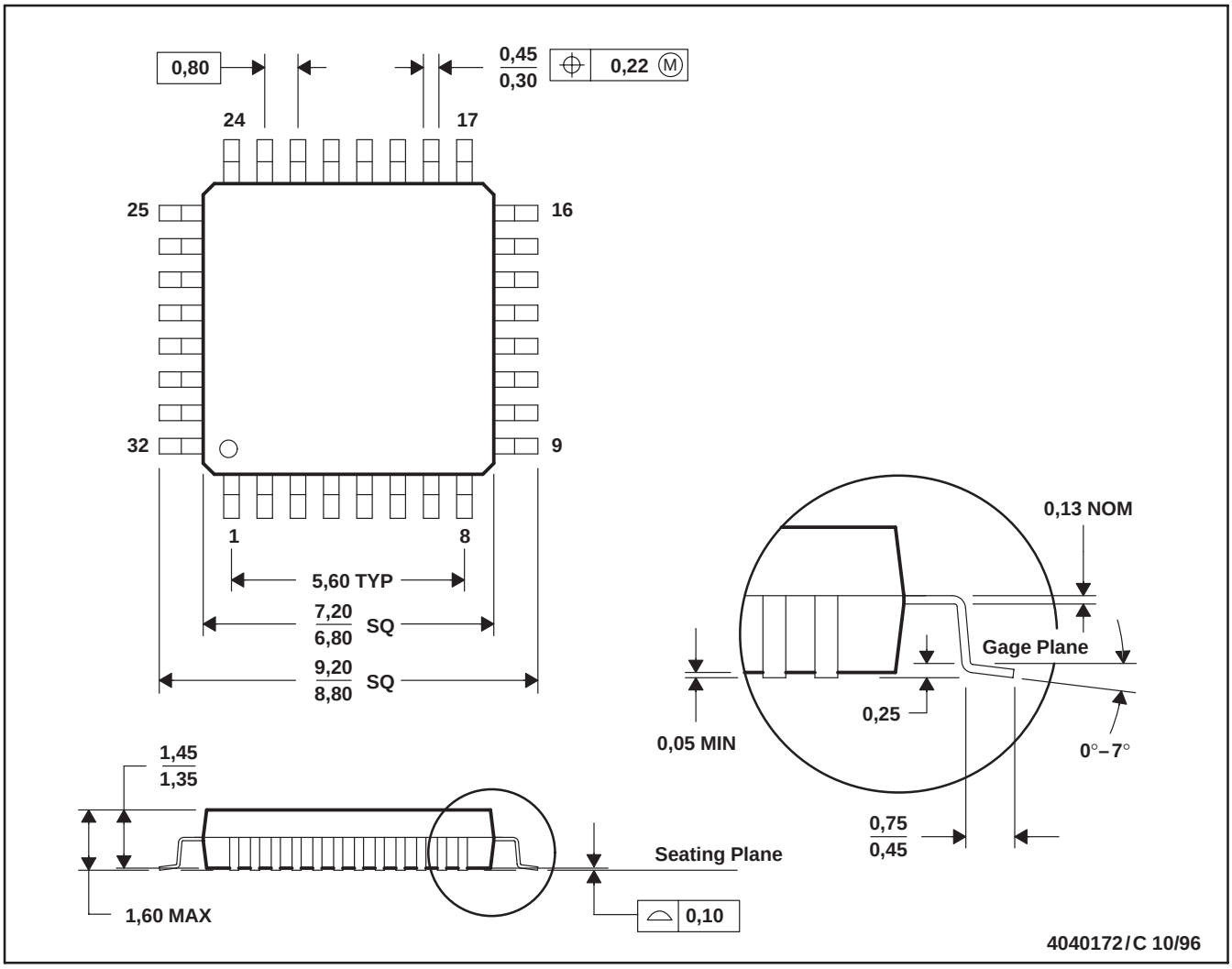
‡ 120 µF per hub is the minimum required per the USB specification, version 1.1. However, TI recommends a 100 µF low ESR tantalum capacitor per port for immunity to voltage droop.

§ LDO is a 5 V to 3.3 V voltage regulator

**Figure 13. TUSB2046B Self-Powered Hub, Individual Port-Power Management Application**

## MECHANICAL DATA

**VF (S-PQFP-G32)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.