

KMB001CEVAL Schematics

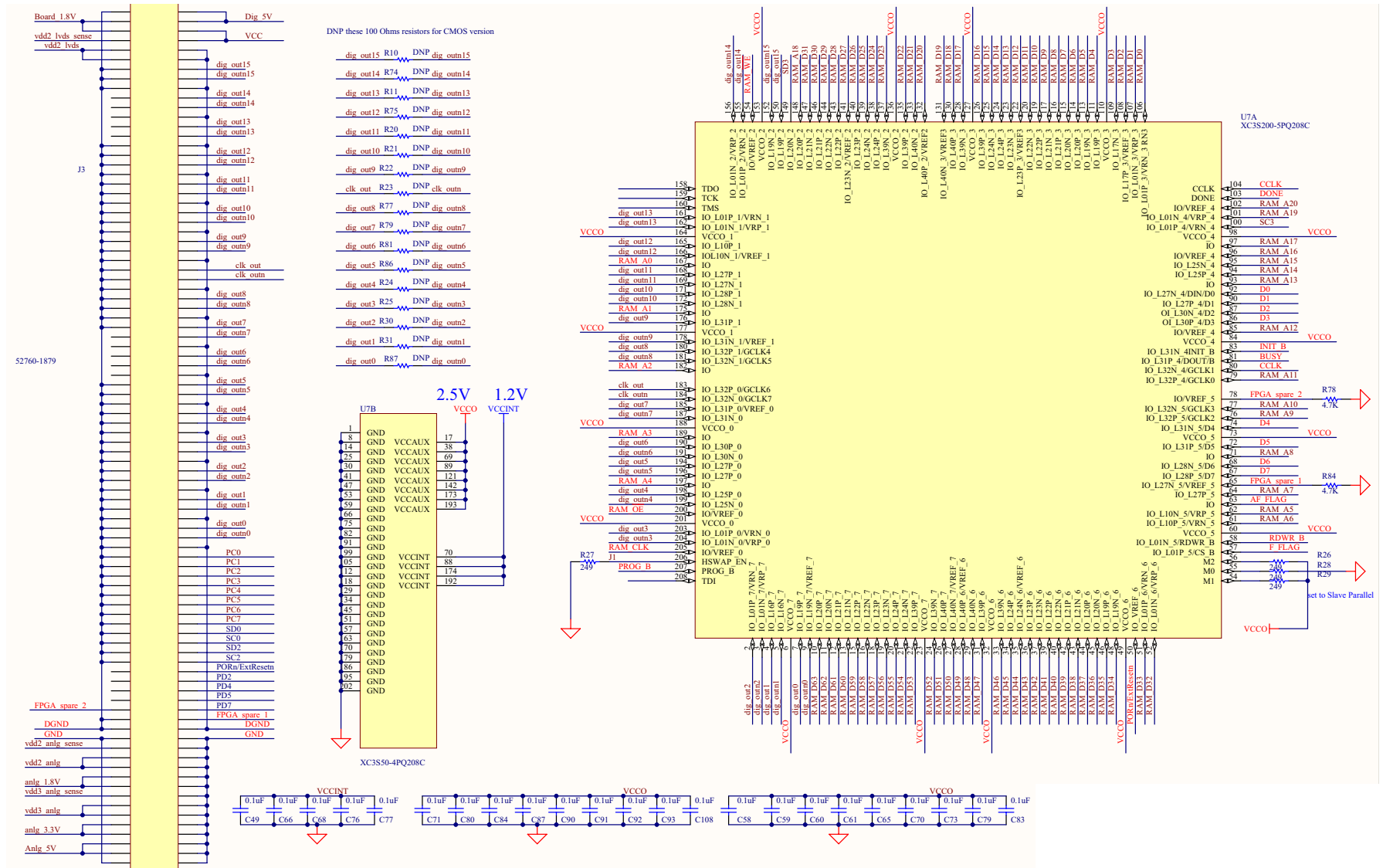
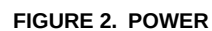


FIGURE 1. FPGA, INPUT/OUTPUT MEZZANINE CONNECTOR



KMB001CEVAL Schematics (Continued)

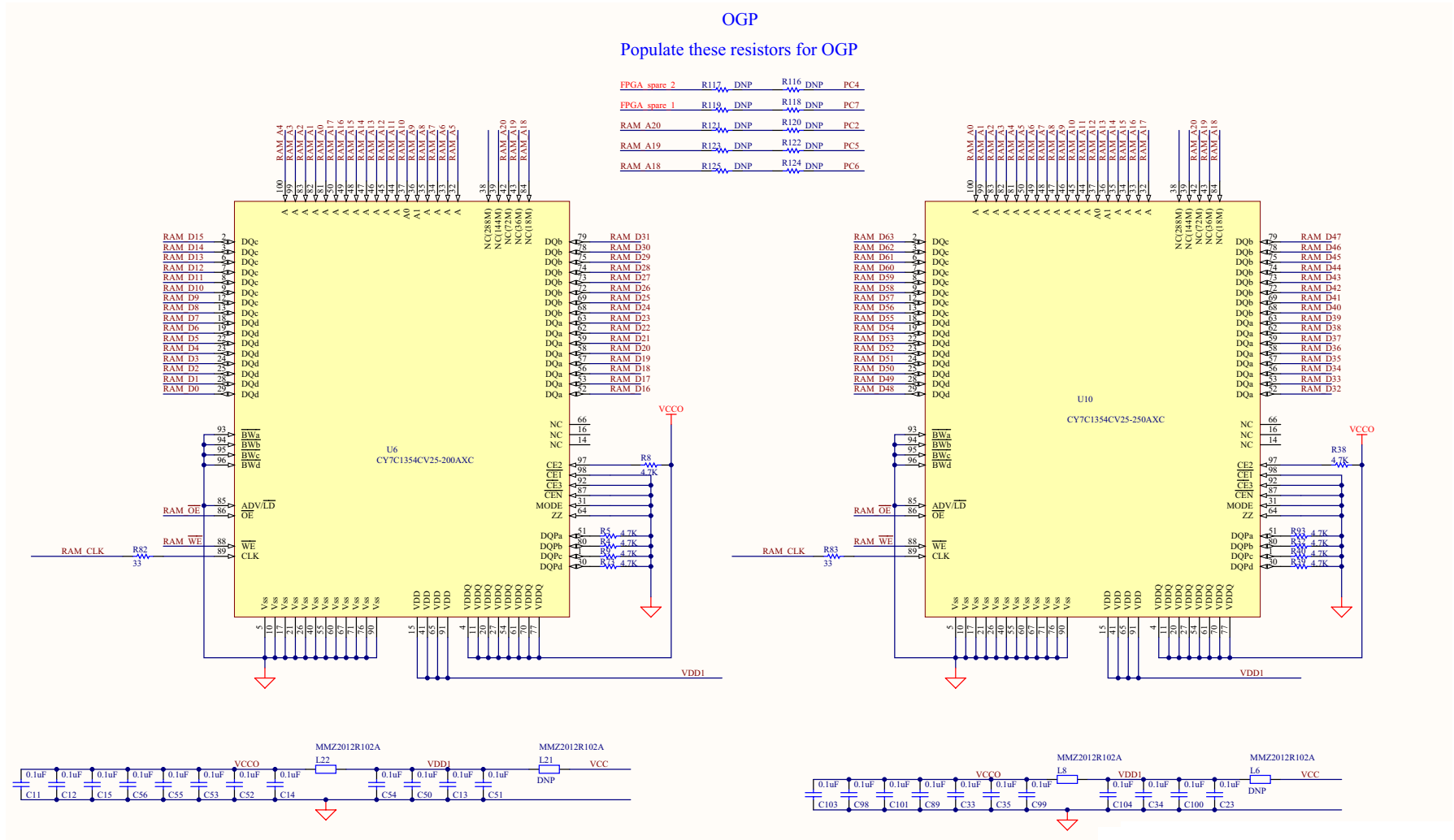
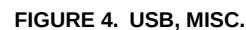


FIGURE 3. MEMORY



KMB001LEVAL Schematics

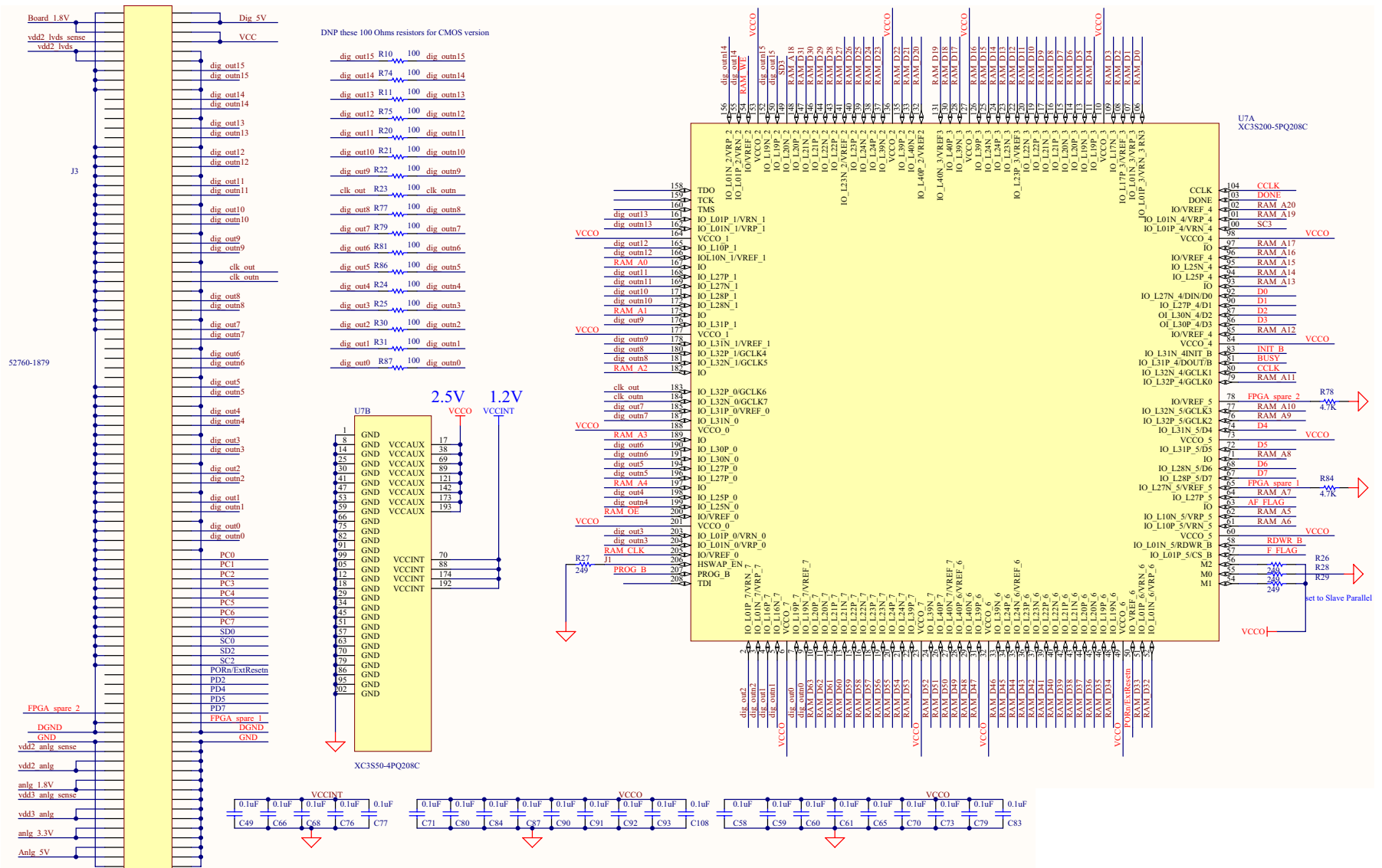


FIGURE 5. FPGA, INPUT/OUTPUT MEZZANINE CONNECTOR

KMB001LEVAL Schematics (Continued)

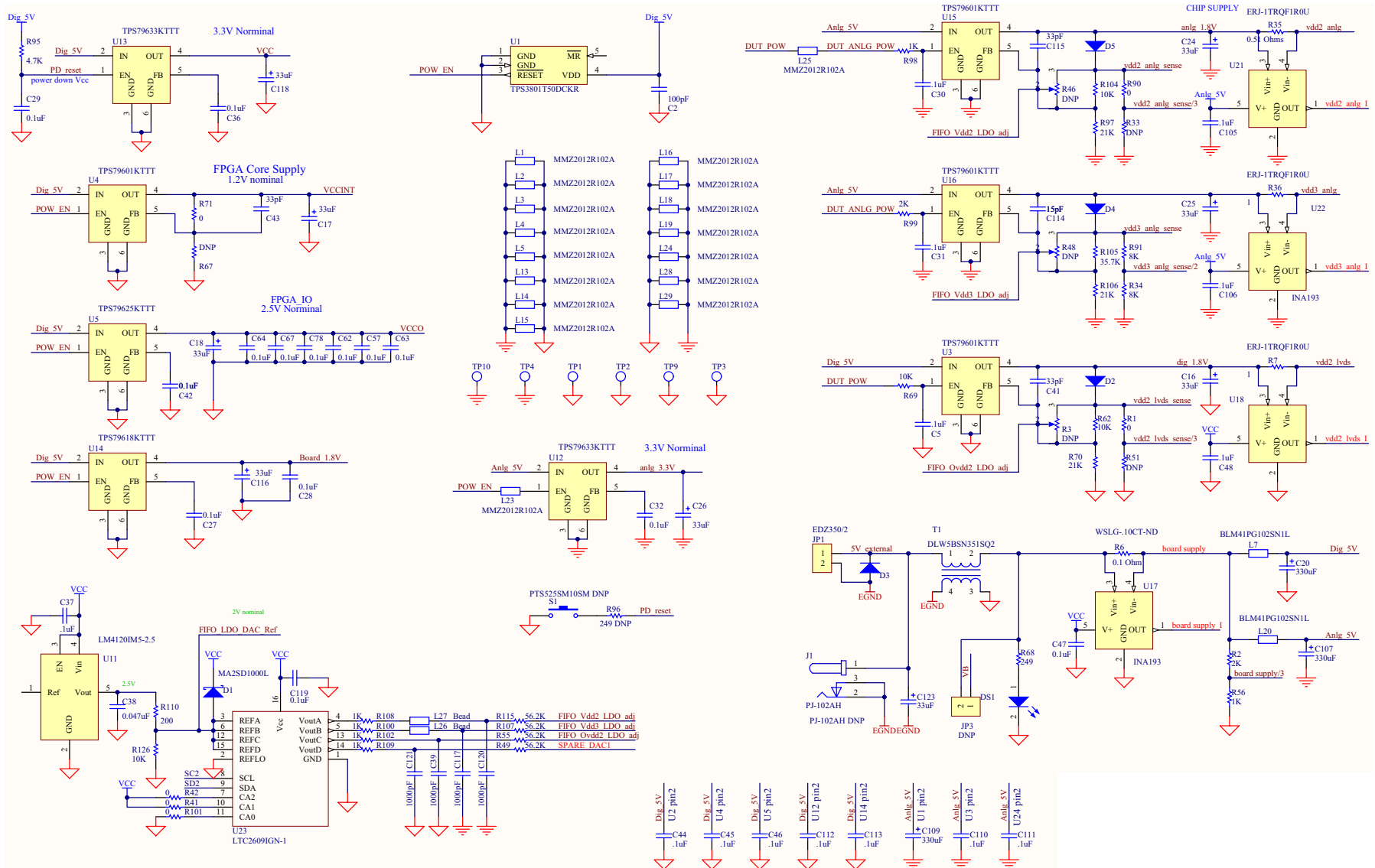
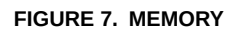


FIGURE 6. POWER



KMB001LEVAL Schematics (Continued)

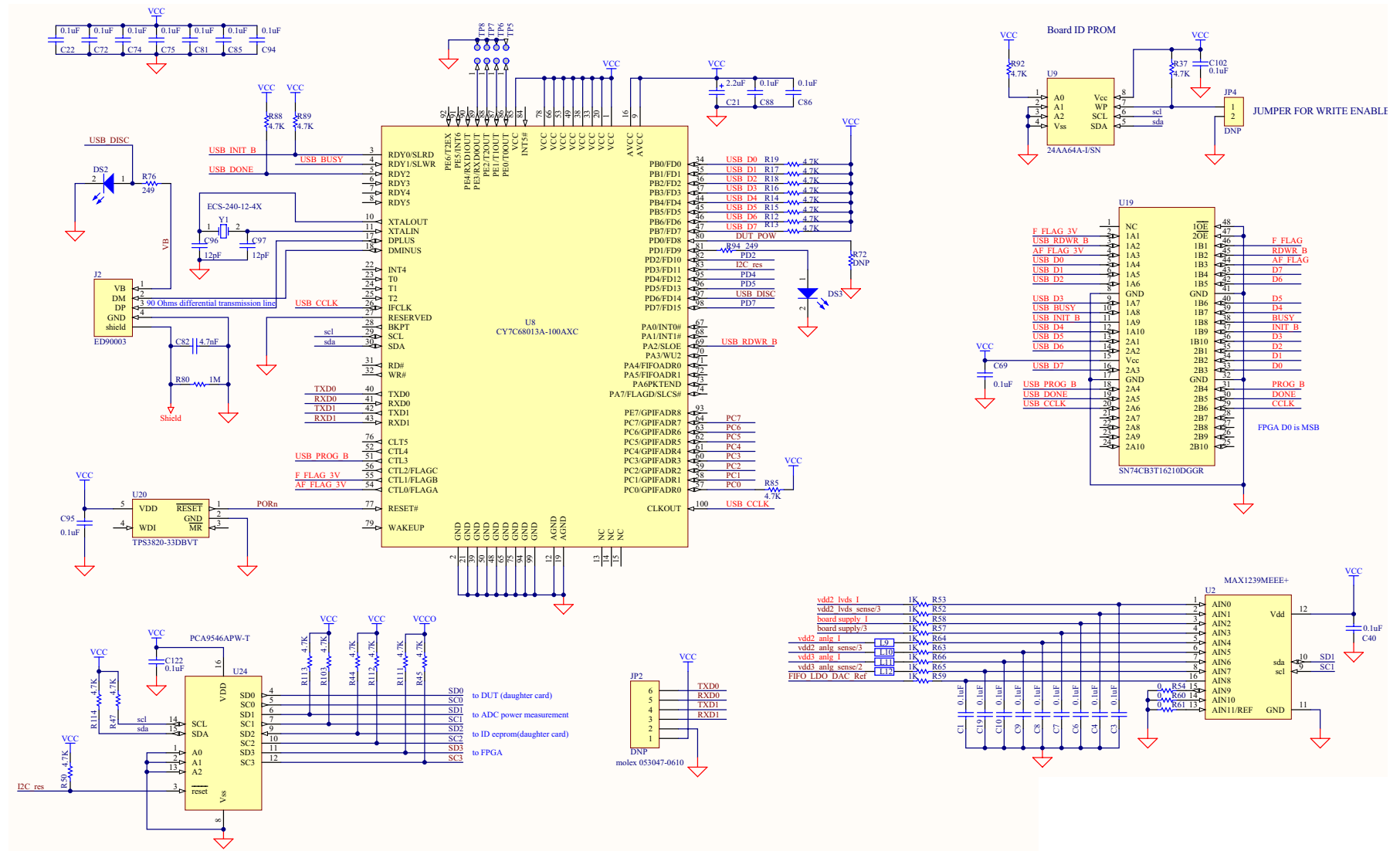


FIGURE 8. USB, MISC.

KMB001CEVAL Layers

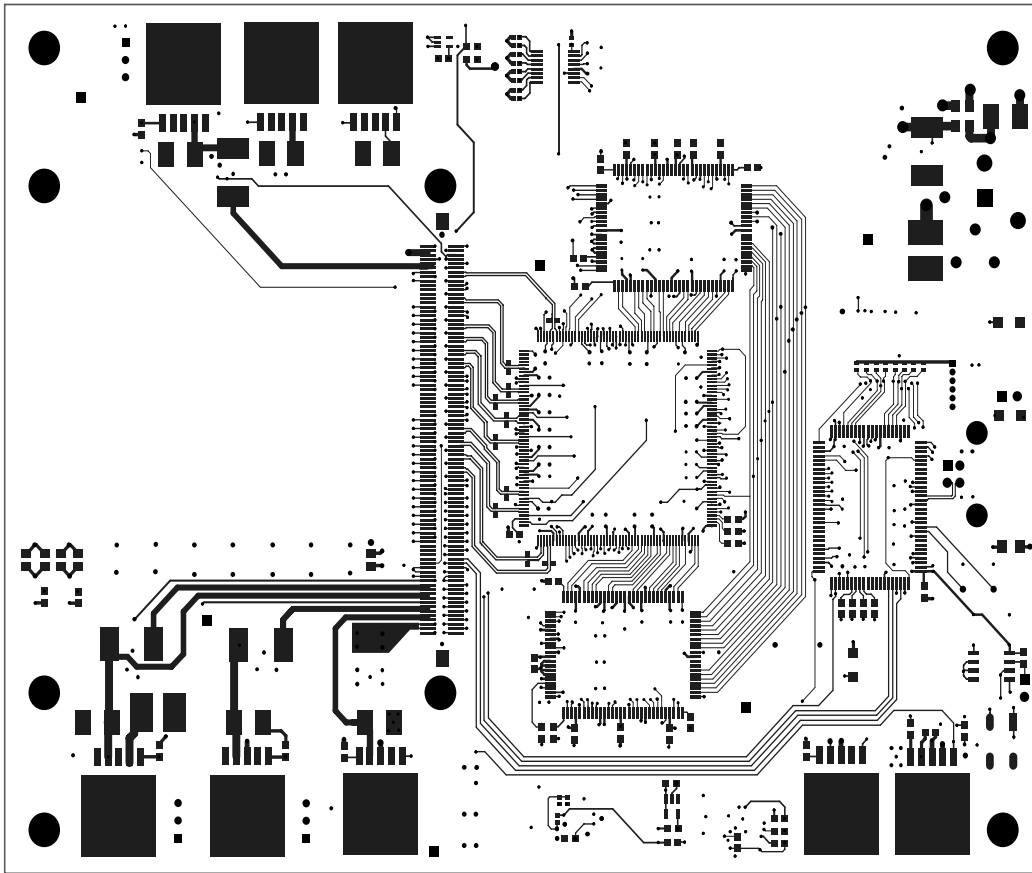


FIGURE 9. TOP LAYER

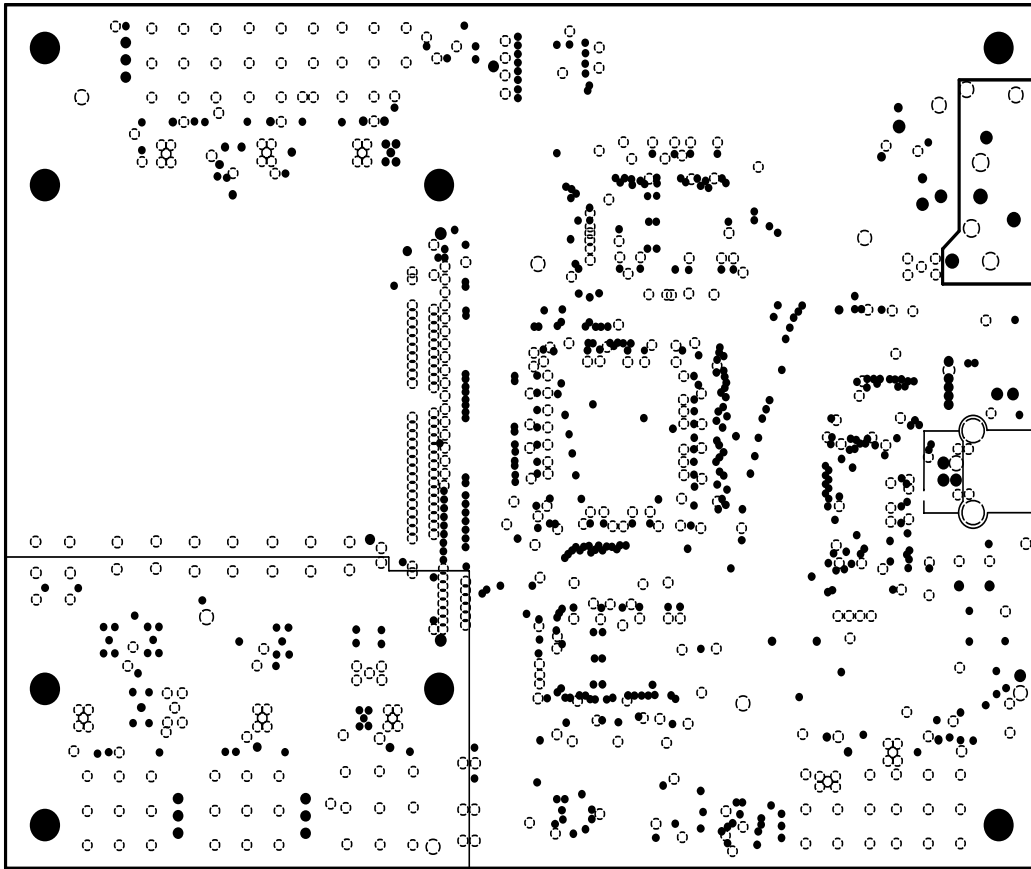
KMB001CEVAL Layers (Continued)

FIGURE 10. GND PLANE

KMB001CEVAL Layers (Continued)

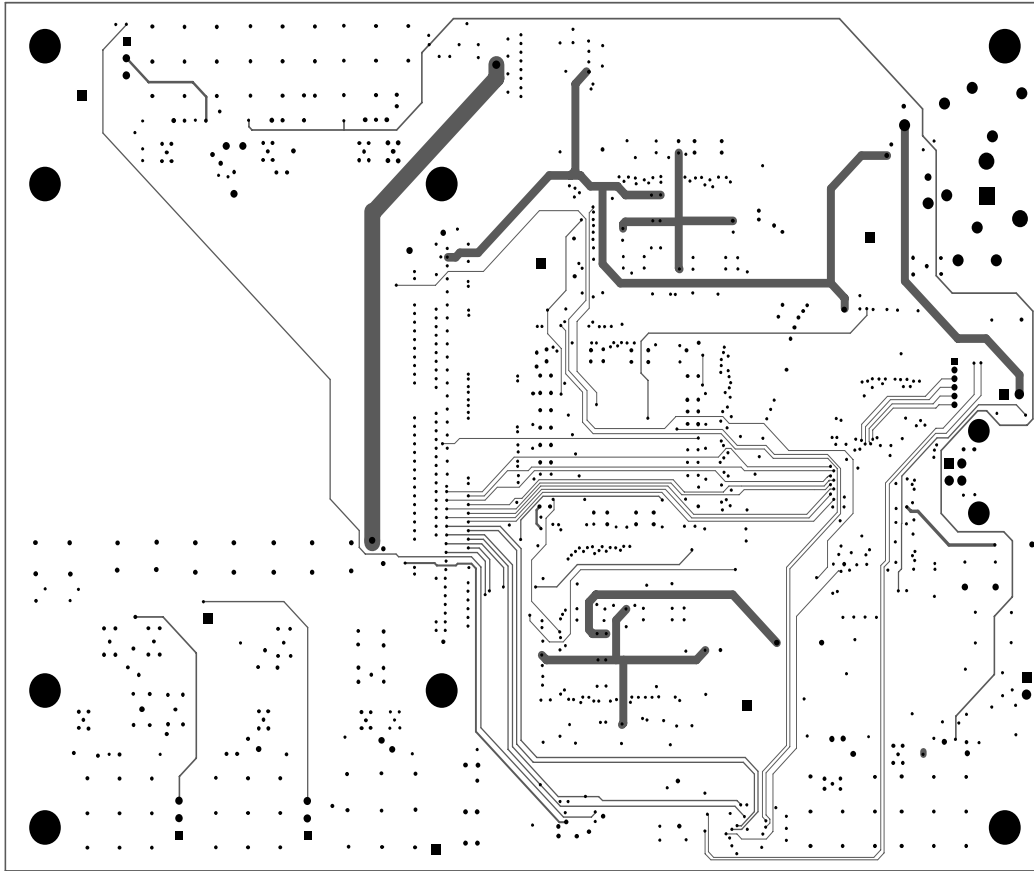


FIGURE 11. MID LAYER 1

KMB001CEVAL Layers (Continued)

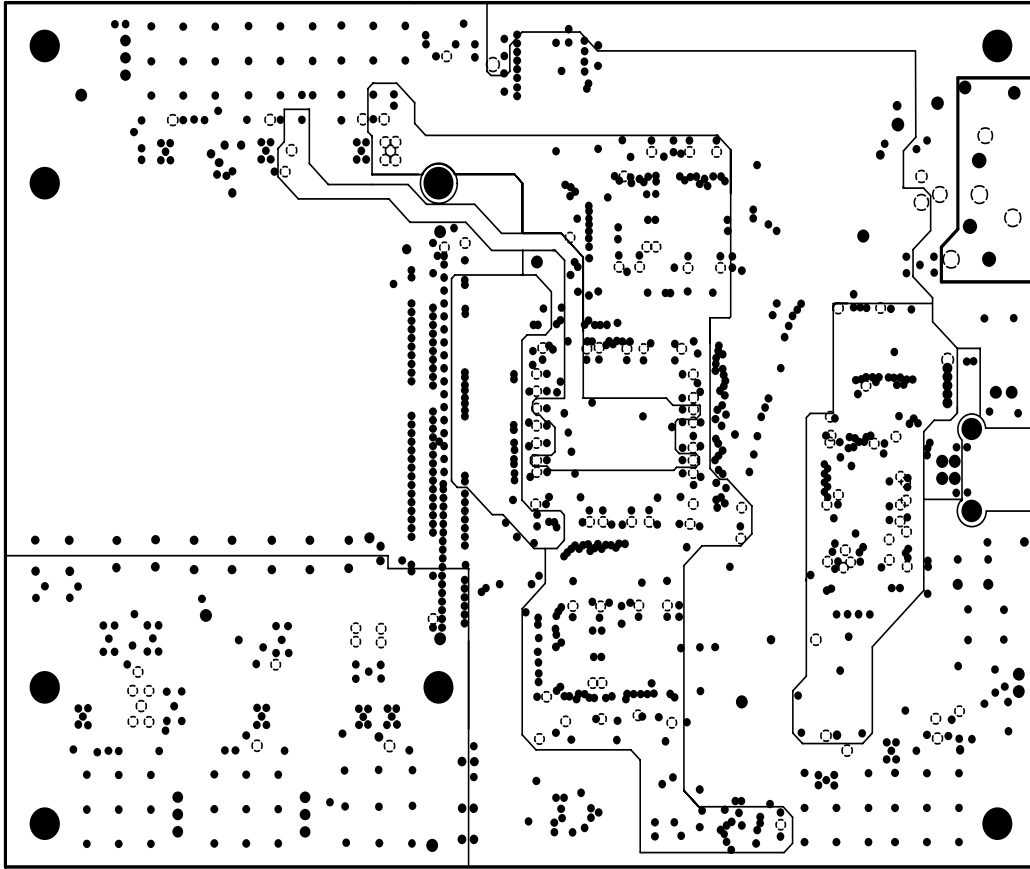


FIGURE 12. POWER PLANE

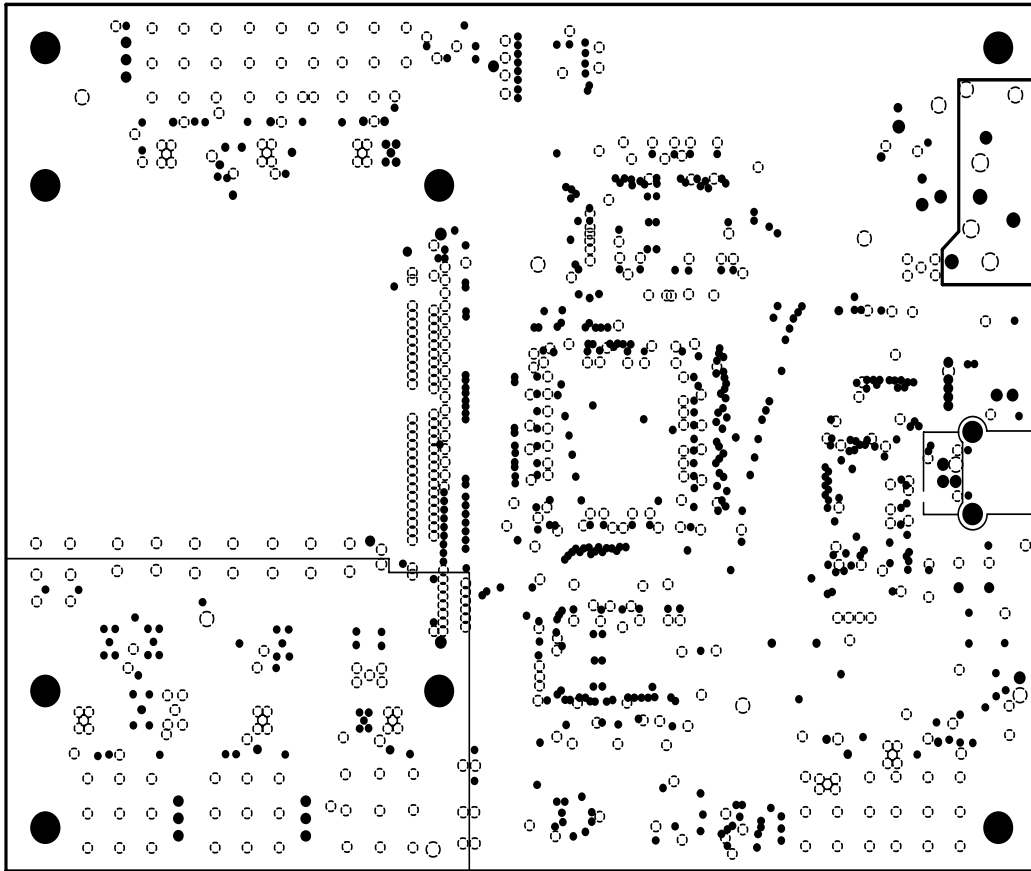
KMB001CEVAL Layers (Continued)

FIGURE 13. GND PLANE 2

KMB001CEVAL Layers (Continued)

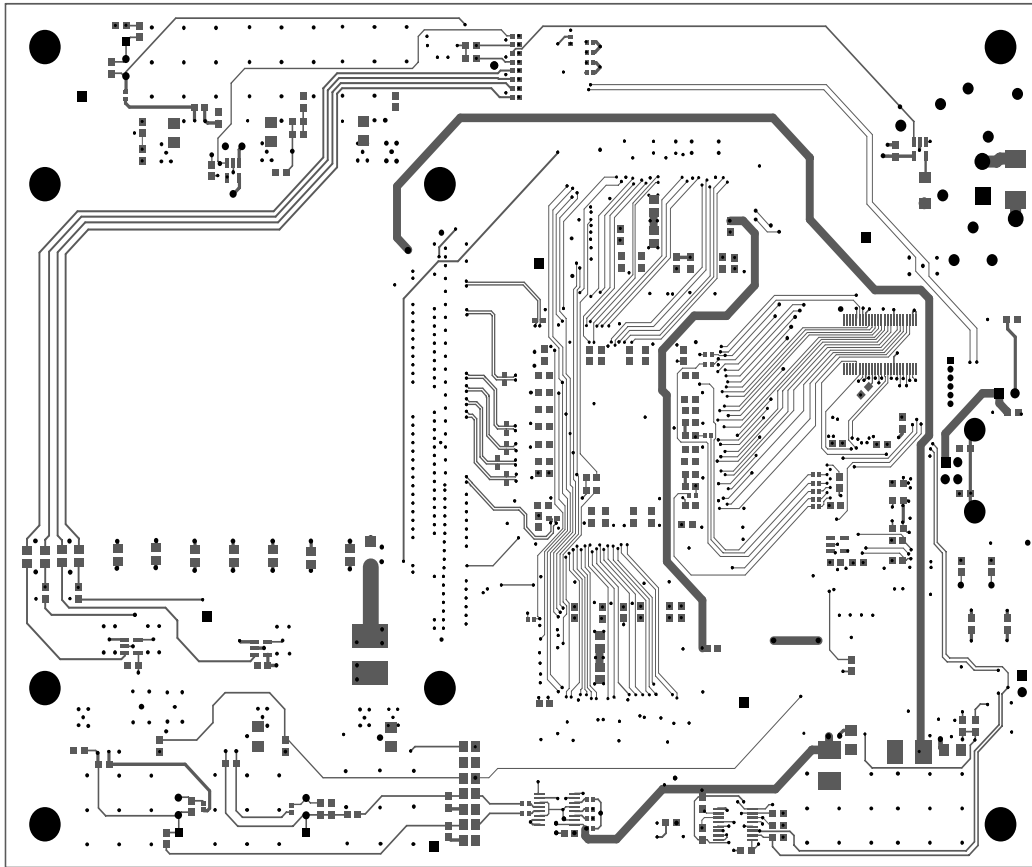


FIGURE 14. BOTTOM LAYER

KMB001CEVAL Layers (Continued)

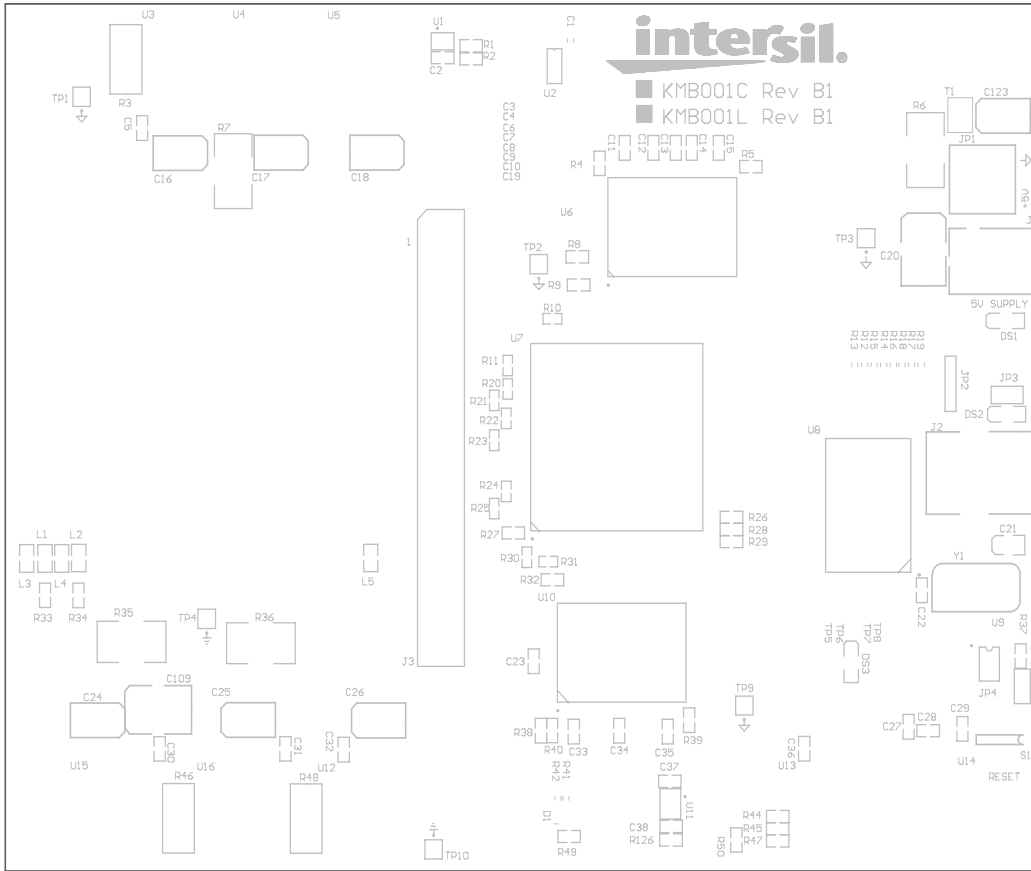


FIGURE 15. TOP OVERLAY

