

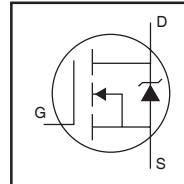
AUTOMOTIVE GRADE

AUIRLR2905Z

Features

- Logic Level
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *

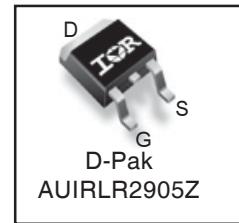
HEXFET® Power MOSFET



$V_{(BR)DSS}$	55V
$R_{DS(on)}$ max.	13.5mΩ
I_D (Silicon Limited)	60A
I_D (Package Limited)	42A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	60	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	43	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	42	
I_{DM}	Pulsed Drain Current ①	240	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	110	W
	Linear Derating Factor	0.72	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	57	mJ
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value ③	85	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ④		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting Torque, 6-32 or M3 screw	300	
		10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case ⑤	—	1.38	°C/W
$R_{θJA}$	Junction-to-Ambient (PCB mount) ⑥	—	40	
$R_{θJA}$	Junction-to-Ambient	—	110	

HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>

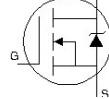
Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{\text{GS}} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.053	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	11	13.5	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}$, $I_D = 36\text{A}$ ③
		—	—	20	$\text{m}\Omega$	$V_{\text{GS}} = 5.0\text{V}$, $I_D = 30\text{A}$ ③
		—	—	22.5	$\text{m}\Omega$	$V_{\text{GS}} = 4.5\text{V}$, $I_D = 15\text{A}$ ③
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	1.0	—	3.0	V	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 250\mu\text{A}$
g_{fs}	Forward Transconductance	25	—	—	S	$V_{\text{DS}} = 25\text{V}$, $I_D = 36\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{\text{DS}} = 55\text{V}$, $V_{\text{GS}} = 0\text{V}$
		—	—	250	μA	$V_{\text{DS}} = 55\text{V}$, $V_{\text{GS}} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{\text{GS}} = 16\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-200	nA	$V_{\text{GS}} = -16\text{V}$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter		Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	—	23	35	nC	$I_D = 36\text{A}$
Q_{gs}	Gate-to-Source Charge	—	8.5	—		$V_{\text{DS}} = 44\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	12	—		$V_{\text{GS}} = 5.0\text{V}$ ③
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	14	—	ns	$V_{\text{DD}} = 28\text{V}$
t_r	Rise Time	—	130	—		$I_D = 36\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	24	—		$R_G = 15\Omega$
t_f	Fall Time	—	33	—		$V_{\text{GS}} = 5.0\text{V}$ ③
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1570	—	pF	$V_{\text{GS}} = 0\text{V}$
C_{oss}	Output Capacitance	—	230	—		$V_{\text{DS}} = 25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	130	—		$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	840	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 1.0\text{V}$, $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	180	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 44\text{V}$, $f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance	—	290	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 0\text{V}$ to 44V ④

Diode Characteristics

Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	42	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	240		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 36\text{A}$, $V_{\text{GS}} = 0\text{V}$ ③
t_{rr}	Reverse Recovery Time	—	22	33	ns	$T_J = 25^\circ\text{C}$, $I_F = 36\text{A}$, $V_{\text{DD}} = 28\text{V}$
Q_{rr}	Reverse Recovery Charge	—	14	21	nC	$\text{d}/\text{dt} = 100\text{A}/\mu\text{s}$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $LS+LD$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.089\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 36\text{A}$, $V_{GS} = 10\text{V}$. Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
- ④ $C_{\text{oss eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population, starting $T_J = 25^\circ\text{C}$, $L = 0.089\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 36\text{A}$, $V_{GS} = 10\text{V}$.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R_θ is measured at T_J approximately 90°C .

Qualification Information[†]

Qualification Level		Automotive (per AEC-Q101) ^{††}	
Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.			
Moisture Sensitivity Level		D-PAK	MSL1
ESD	Machine Model	Class M2 (200V) AEC-Q101-002	
	Human Body Model	Class H1B (1000V) AEC-Q101-001	
	Charged Device Model	Class C5 (1125V) AEC-Q101-005	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

^{††} Exceptions to AEC-Q101 requirements are noted in the qualification report.

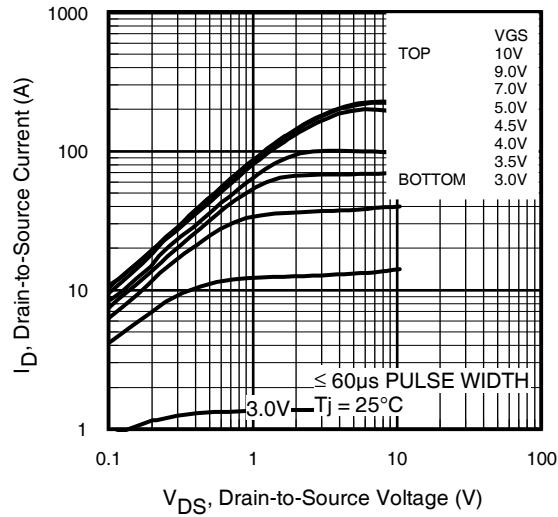


Fig 1. Typical Output Characteristics

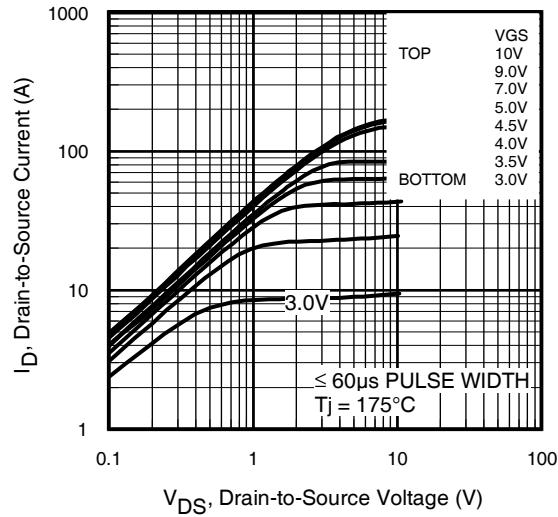


Fig 2. Typical Output Characteristics

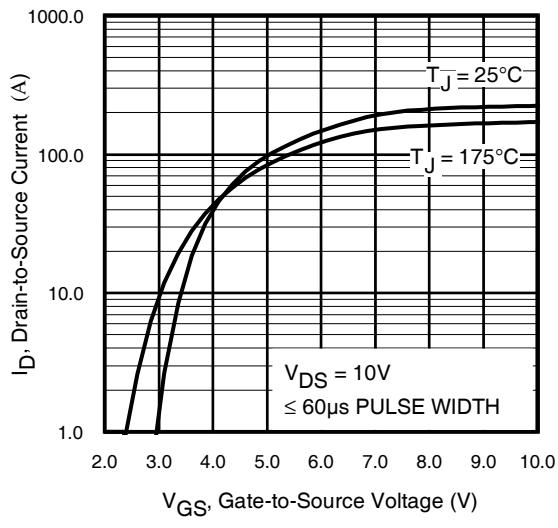


Fig 3. Typical Transfer Characteristics

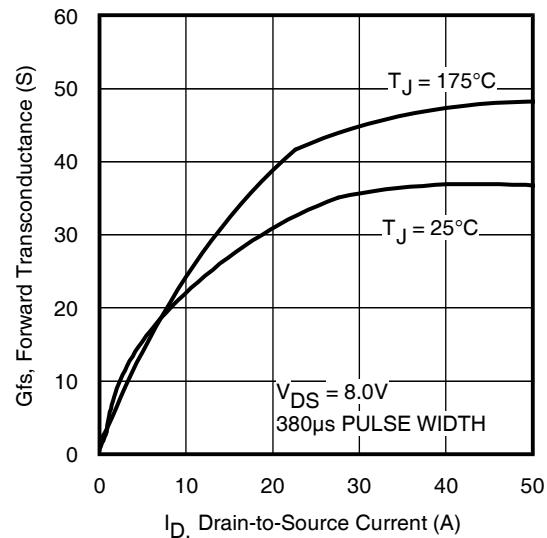


Fig 4. Typical Forward Transconductance Vs. Drain Current

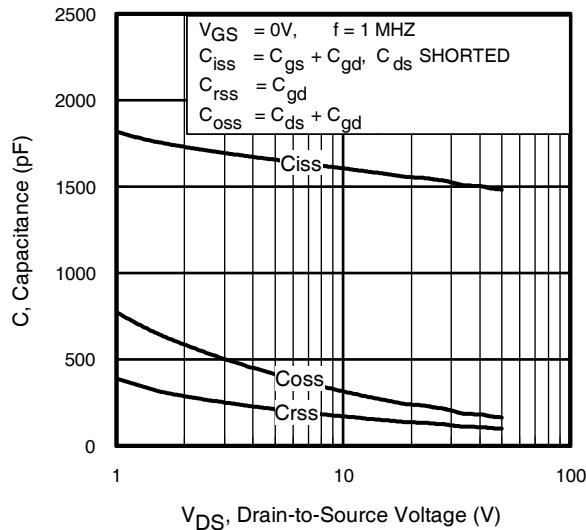


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

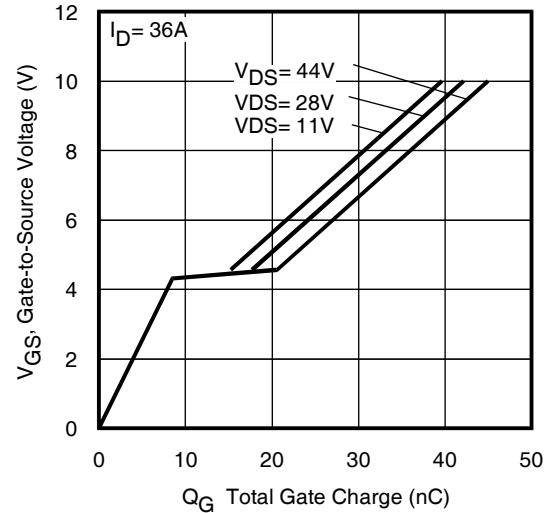


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

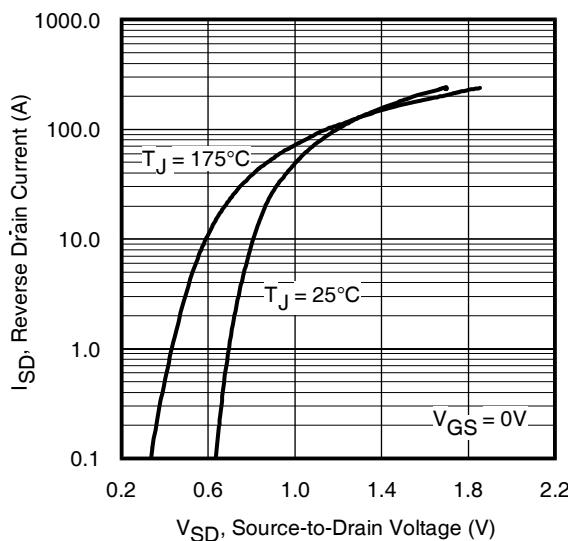


Fig 7. Typical Source-Drain Diode
Forward Voltage

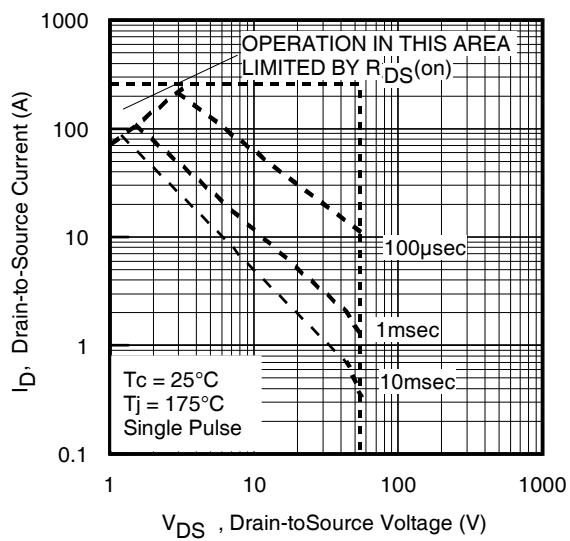


Fig 8. Maximum Safe Operating Area

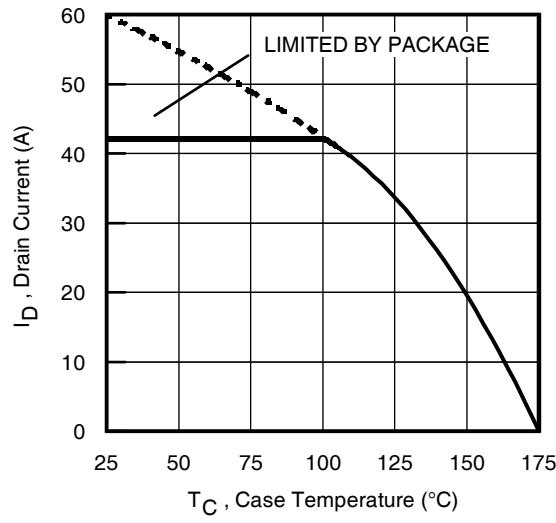


Fig 9. Maximum Drain Current Vs.
Case Temperature

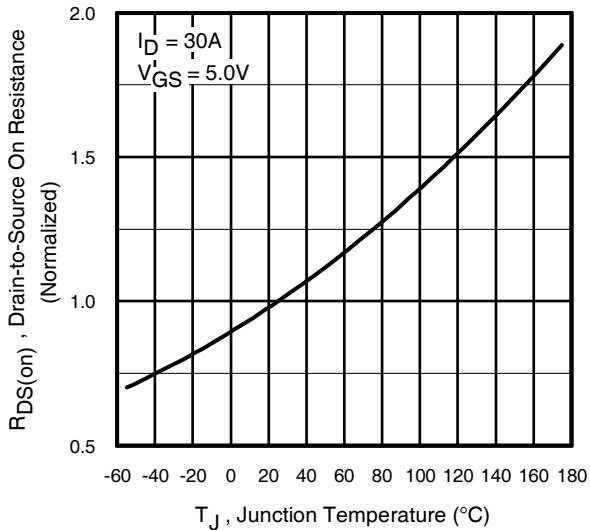


Fig 10. Normalized On-Resistance
Vs. Temperature

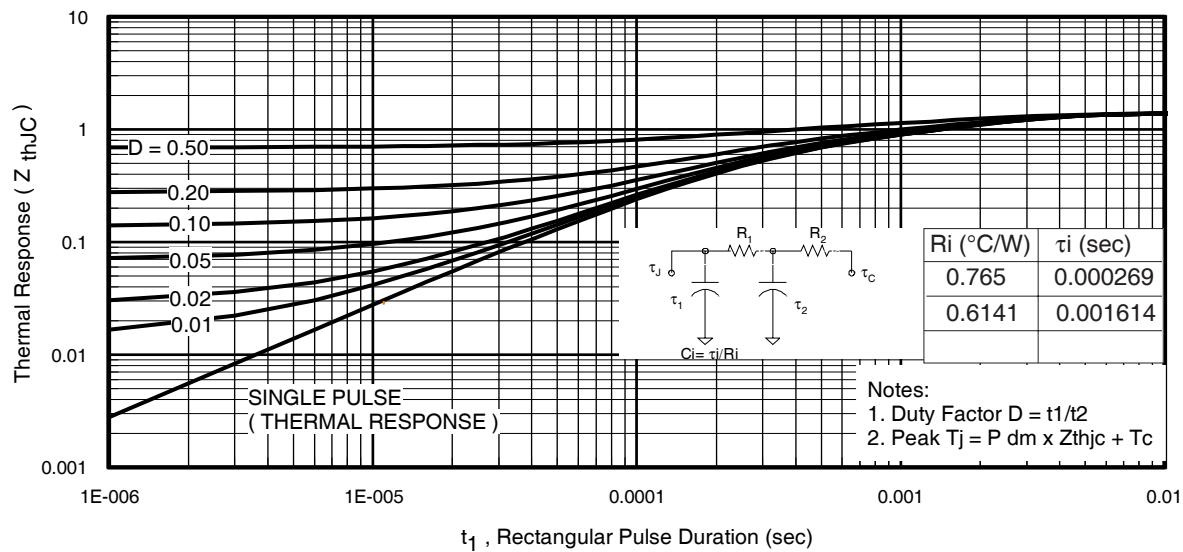


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

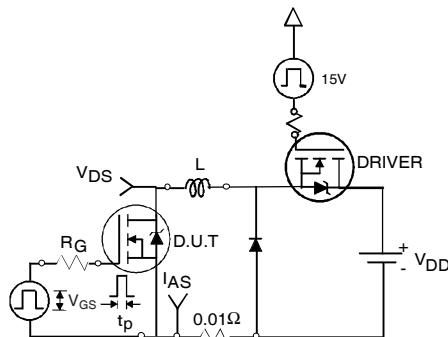


Fig 12a. Unclamped Inductive Test Circuit

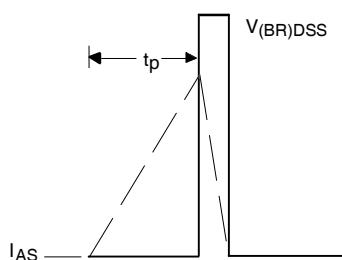


Fig 12b. Unclamped Inductive Waveforms

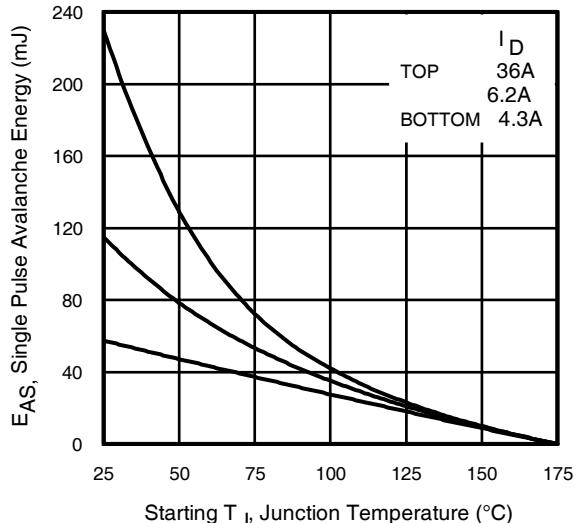


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

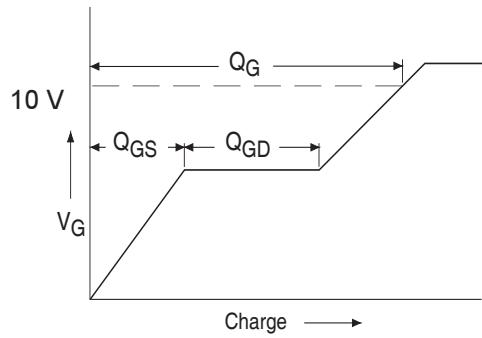


Fig 13a. Basic Gate Charge Waveform

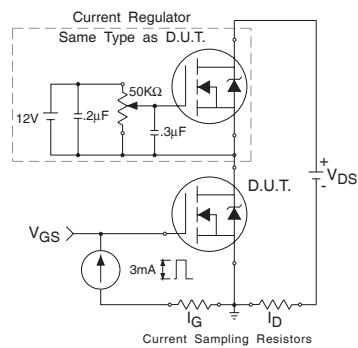


Fig 13b. Gate Charge Test Circuit
www.irf.com

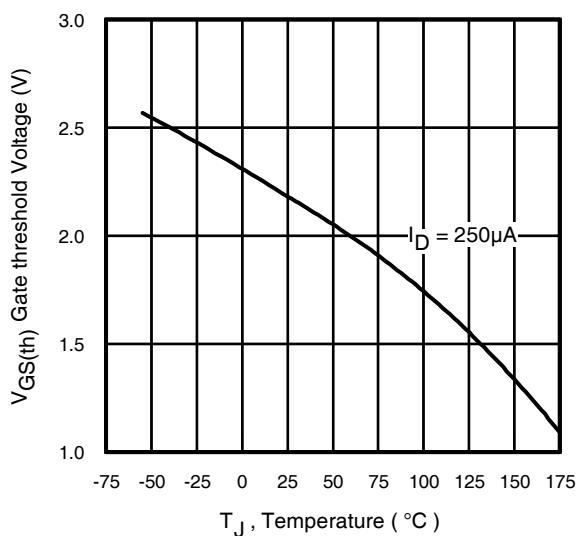


Fig 14. Threshold Voltage Vs. Temperature

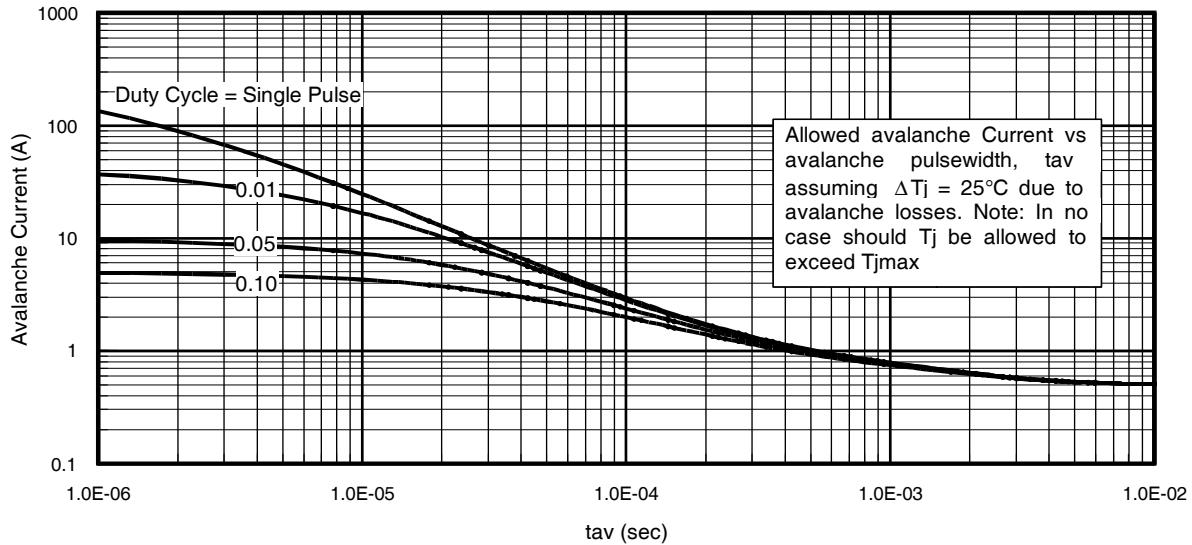
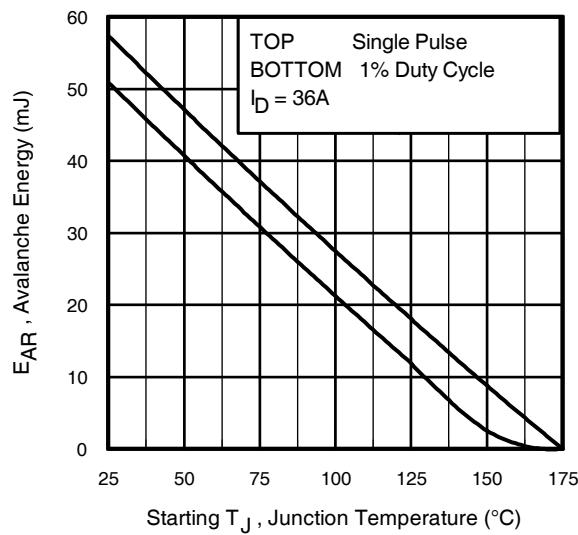


Fig 15. Typical Avalanche Current Vs.Pulsewidth



Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 16. Maximum Avalanche Energy Vs. Temperature

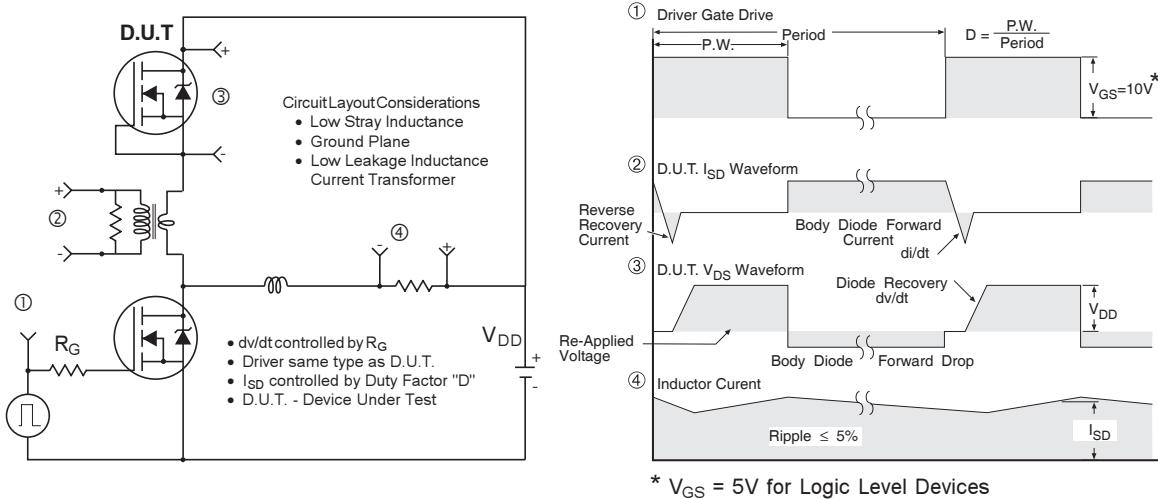


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

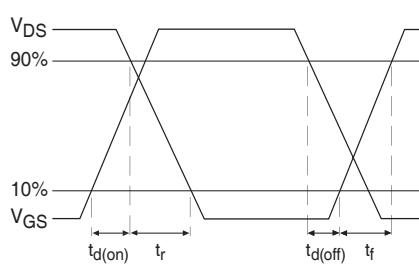
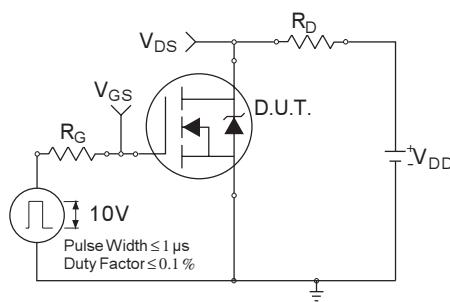
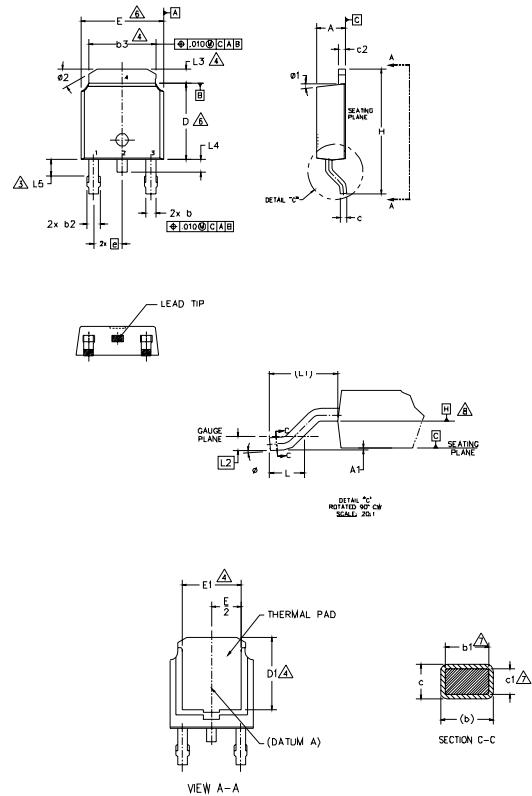


Fig 18b. Switching Time Waveforms

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
3. △ LEAD DIMENSION UNCONTROLLED IN L5.
4. △ DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5. SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
6. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
7. △ DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
8. △ DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
9. OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS		NOTES
	MILLIMETERS	INCHES	
	MIN.	MAX.	
A	2.18	2.39	.086 .094
A1	—	0.13	— .005
b	0.64	0.89	.025 .035
b1	0.65	0.79	.025 .031
b2	0.76	1.14	.030 .045
b3	4.95	5.46	.195 .215
c	0.46	0.61	.018 .024
c1	0.41	0.56	.016 .022
c2	0.46	0.89	.018 .035
D	5.97	6.22	.235 .245
D1	5.21	—	.205 —
E	6.35	6.73	.250 .265
E1	4.32	—	.170 —
e	2.29	BSC	.090 BSC
H	9.40	10.41	.370 .410
L	1.40	1.78	.055 .070
L1	2.74	BSC	.108 REF.
L2	0.51	BSC	.020 BSC
L3	0.89	1.27	.055 .050
L4	—	1.02	— .040
L5	1.14	1.52	.045 .060
Ø	0°	10°	0° 10°
Ø1	0°	15°	0° 15°
Ø2	25°	35°	.25° .35°

LEAD ASSIGNMENTS

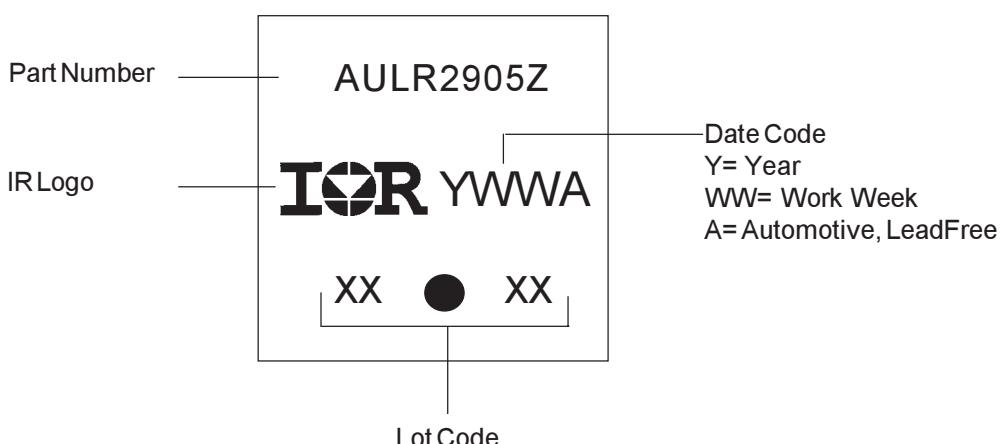
HEXFET

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

IGBT & CoPAK

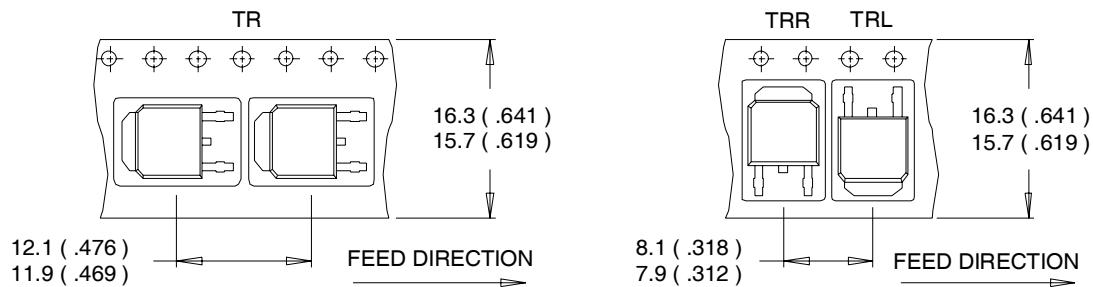
1. GATE
2. COLLECTOR
3. Emitter
4. COLLECTOR

D-Pak Part Marking Information

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

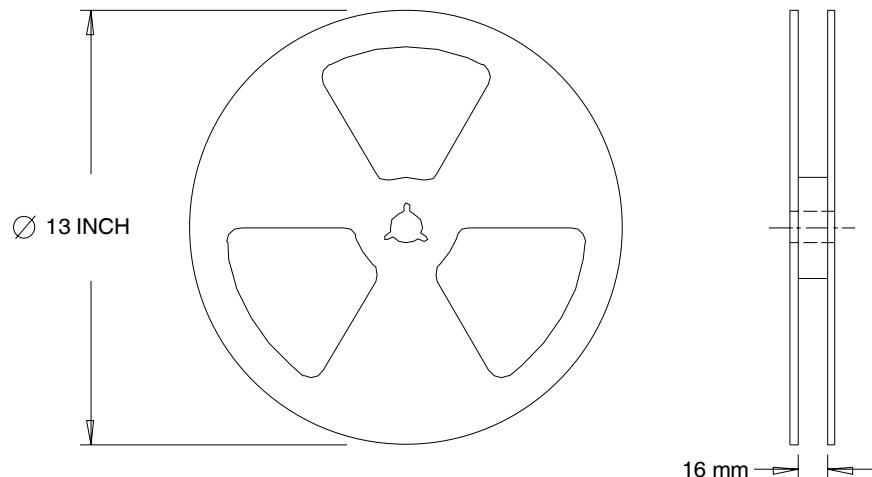
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRLR2905Z	Dpak	Tube	75	AUIRLR2905Z
		Tape and Reel	2000	AUIRLR2905ZTR
		Tape and Reel Left	3000	AUIRLR2905ZTRL
		Tape and Reel Right	3000	AUIRLR2905ZTRR

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For technical support, please contact IR's Technical Assistance Center

<http://www.irf.com/technical-info/>

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