

1. General description

Planar passivated high commutation three quadrant triac in a SOT186A (TO-220F) "full pack" plastic package. This "series ET" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers including microcontrollers. It is used in applications where "high junction operating temperature" capability is required.

2. Features and benefits

- 3Q technology for improved noise immunity
- Direct interfacing with low power drivers and microcontrollers
- Good immunity to false turn-on by dV/dt
- High commutation capability with sensitive gate
- High junction operating temperature capability
- High voltage capability
- Isolated mounting base package
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only

3. Applications

- Applications subject to high temperature
- Industrial and domestic heating circuits
- Motor controls e.g. washing machines and vacuum cleaners
- Refrigeration and air-conditioner compressor controls

4. Quick reference data

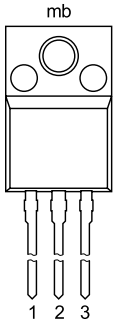
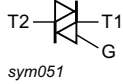
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	600	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_h \leq 98\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3		-	-	10	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5		-	-	100	A
T_j	junction temperature			-	-	150	$^{\circ}\text{C}$

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 7		0.5	-	10	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 7		0.5	-	10	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; Fig. 7		0.5	-	10	mA
Dynamic characteristics							
dV _D /dt _i	rate of rise of off-state voltage	V _{DM} = 402 V; T _j = 150 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit		50	-	-	V/μs
dI _{com} /dt	rate of change of commutating current	V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 10 A; dV _{com} /dt = 1 V/μs; gate open circuit		5	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BTA410X-600ET	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_h \leq 98\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	10	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig 4 ; Fig 5	-	100	A
		full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_p = 16.7\text{ ms}$	-	110	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	50	A^2s
dI_{T}/dt	rate of rise of on-state current	$I_G = 20\text{ mA}$	-	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_{j}	junction temperature		-	150	$^{\circ}\text{C}$

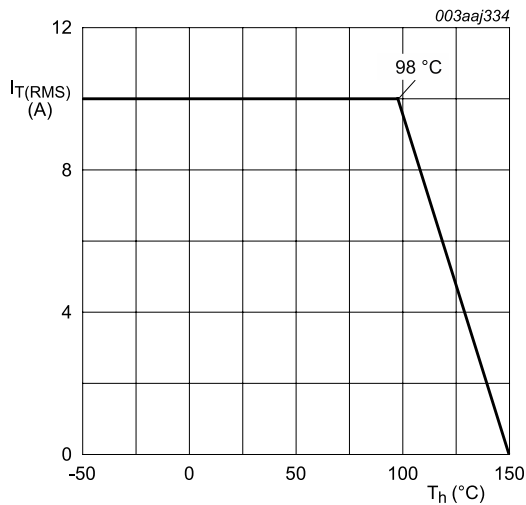
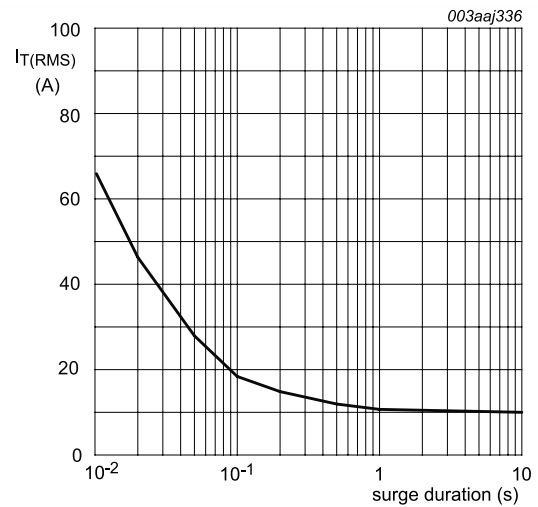


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values



$f = 50\text{ Hz}$; $T_h = 98\text{ }^{\circ}\text{C}$

Fig. 2. RMS on-state current as a function of surge duration; maximum values

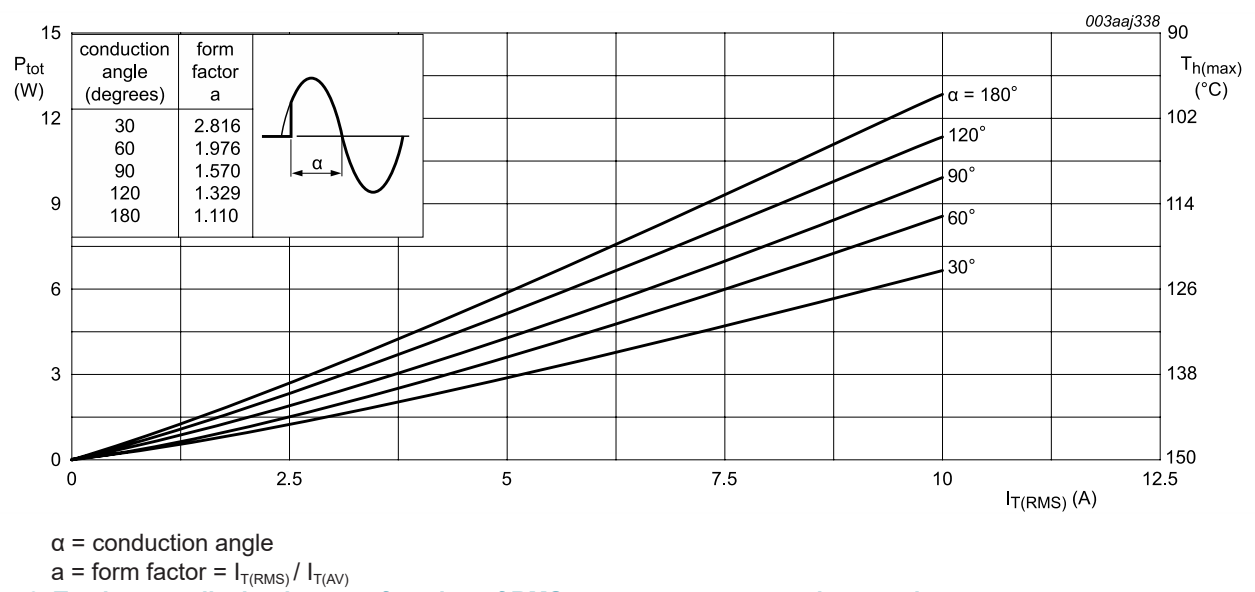


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

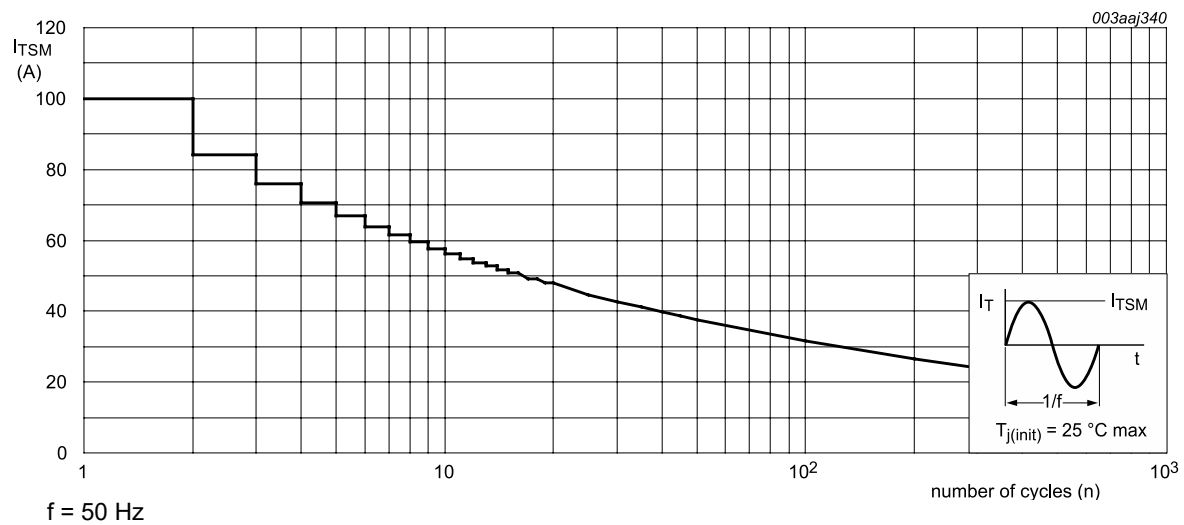
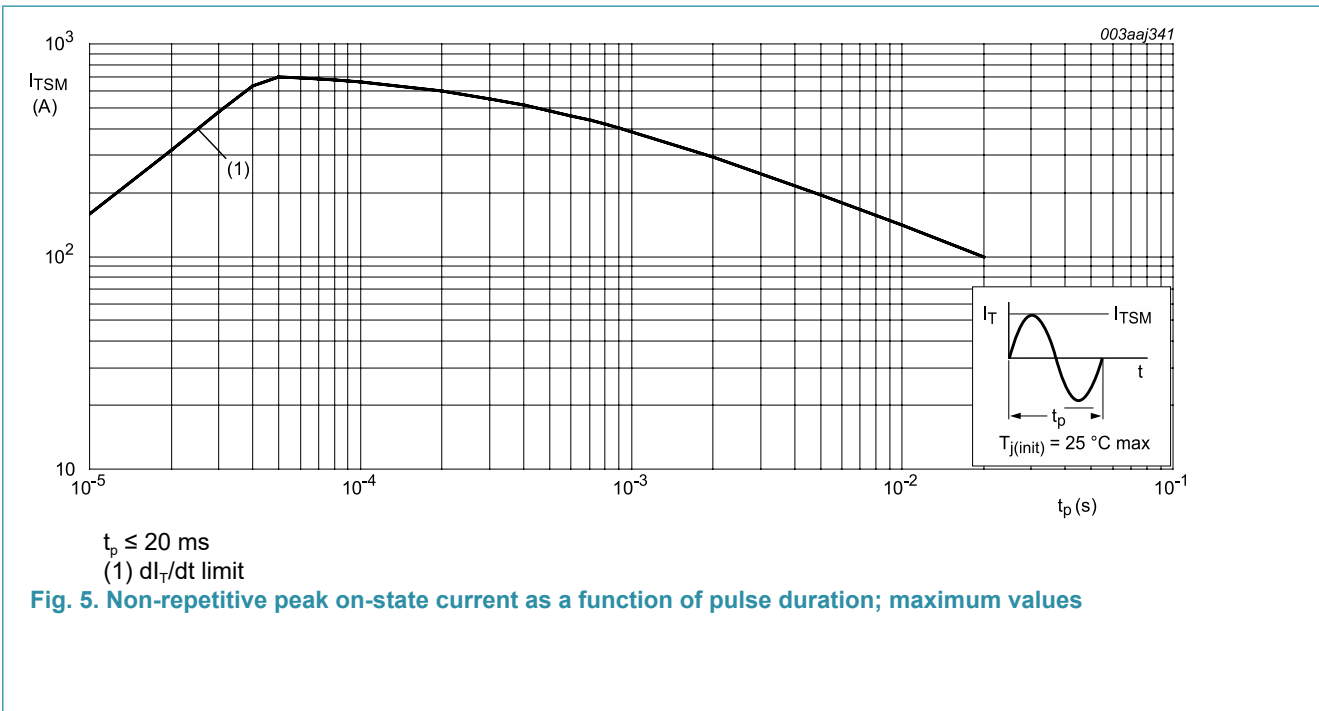


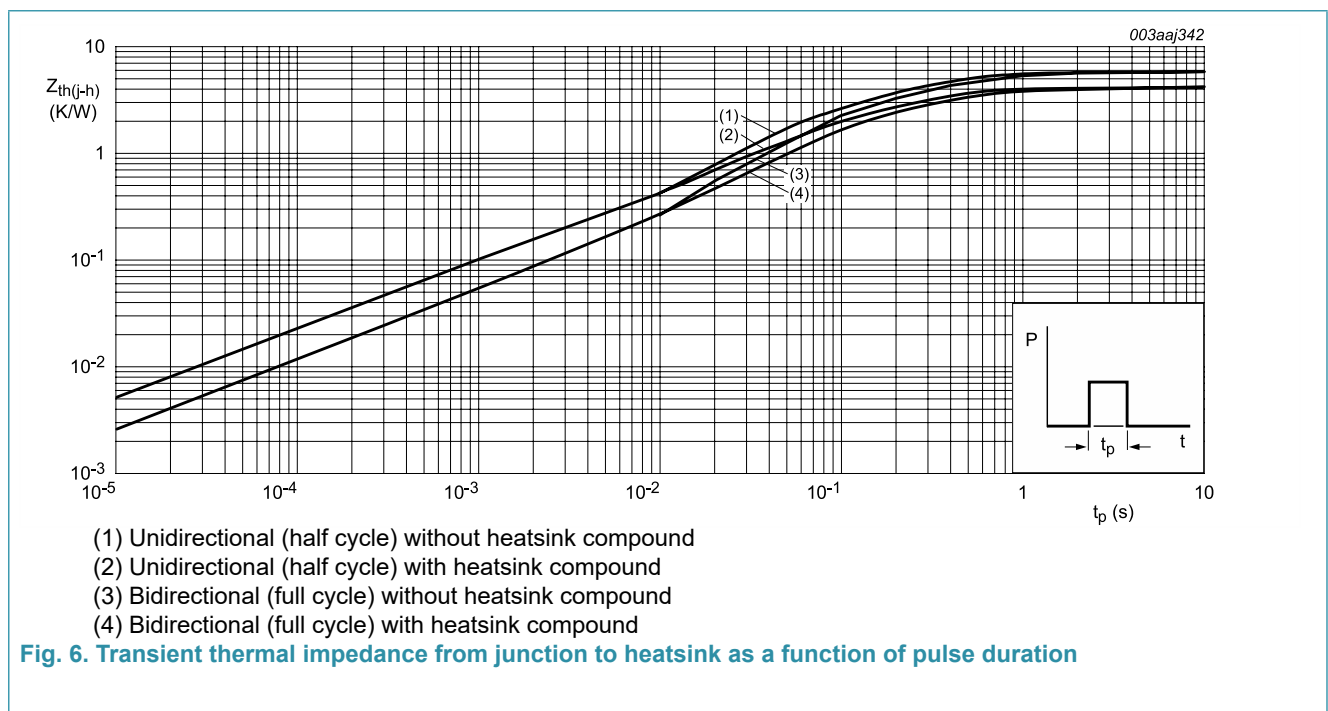
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full cycle or half cycle; with heatsink compound; Fig. 6	-	-	4	K/W
		full cycle or half cycle; without heatsink compound; Fig. 6	-	-	5.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	55	-	K/W



9. Isolation characteristics

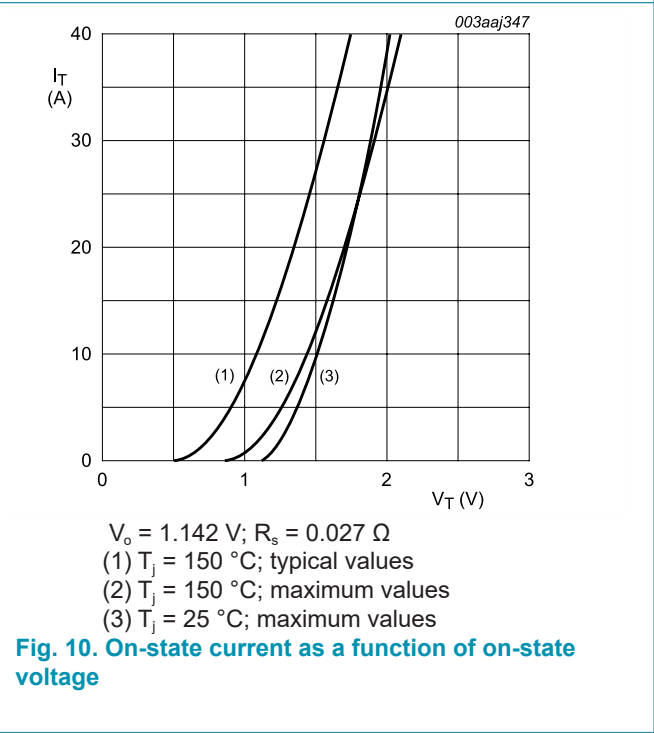
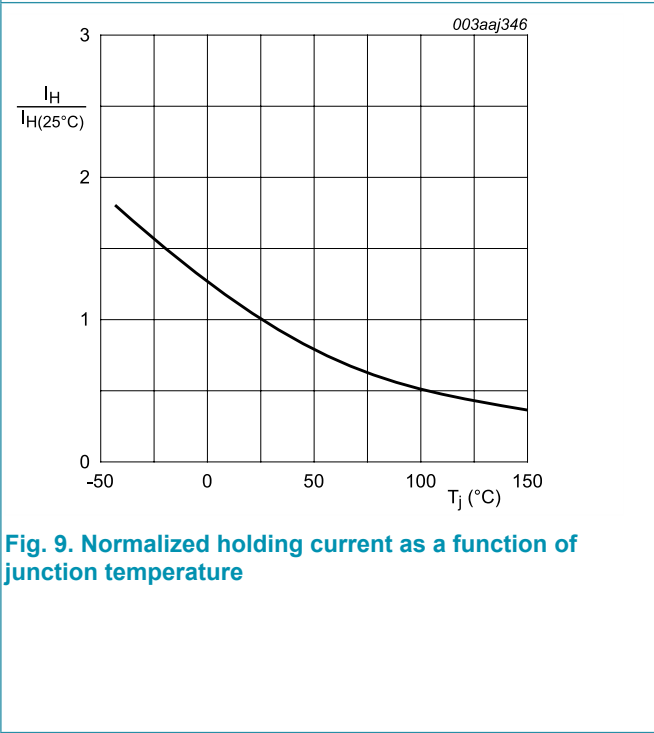
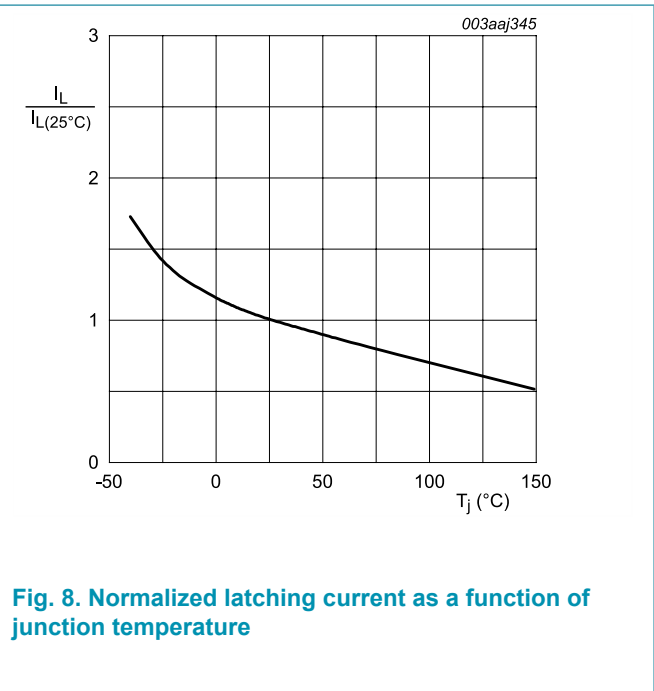
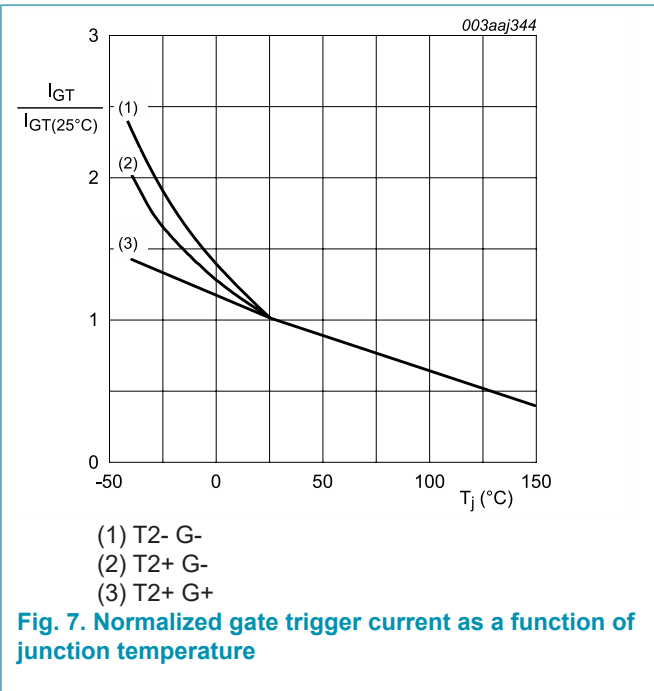
Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; $50\text{ Hz} \leq f \leq 60\text{ Hz}$; $RH \leq 65\%$; $T_h = 25\text{ }^\circ\text{C}$	-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; $f = 1\text{ MHz}$; $T_h = 25\text{ }^\circ\text{C}$	-	10	-	pF

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_J = 25\text{ }^\circ\text{C}$; Fig. 7		0.5	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_J = 25\text{ }^\circ\text{C}$; Fig. 7		0.5	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_J = 25\text{ }^\circ\text{C}$; Fig. 7		0.5	-	10	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_J = 25\text{ }^\circ\text{C}$; Fig. 8		-	-	25	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_J = 25\text{ }^\circ\text{C}$; Fig. 8		-	-	30	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_J = 25\text{ }^\circ\text{C}$; Fig. 8		-	-	25	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 9		-	-	15	mA
V_T	on-state voltage	$I_T = 15\text{ A}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 10		-	1.3	1.6	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 11		-	0.7	1	V
		$V_D = 400\text{ V}$; $T_J = 150\text{ }^\circ\text{C}$; Fig. 11		0.25	0.4	-	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_J = 150\text{ }^\circ\text{C}$		-	0.4	2	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_J = 150\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit		50	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_J = 150\text{ }^\circ\text{C}$; $I_{T(RMS)} = 10\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit		2	-	-	A/ms
		$V_D = 400\text{ V}$; $T_J = 150\text{ }^\circ\text{C}$; $I_{T(RMS)} = 10\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit		3.5	-	-	A/ms
		$V_D = 400\text{ V}$; $T_J = 150\text{ }^\circ\text{C}$; $I_{T(RMS)} = 10\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit		5	-	-	A/ms



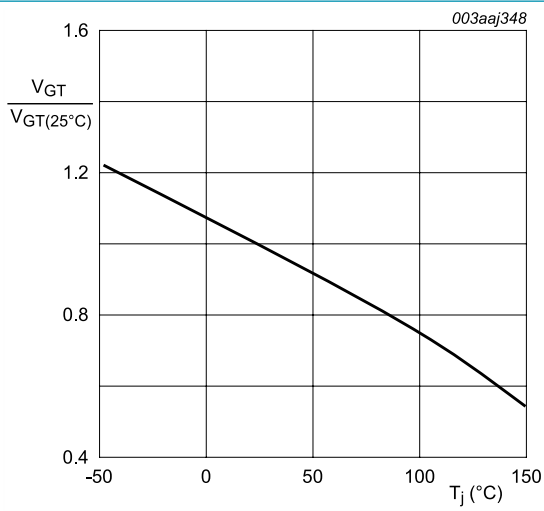
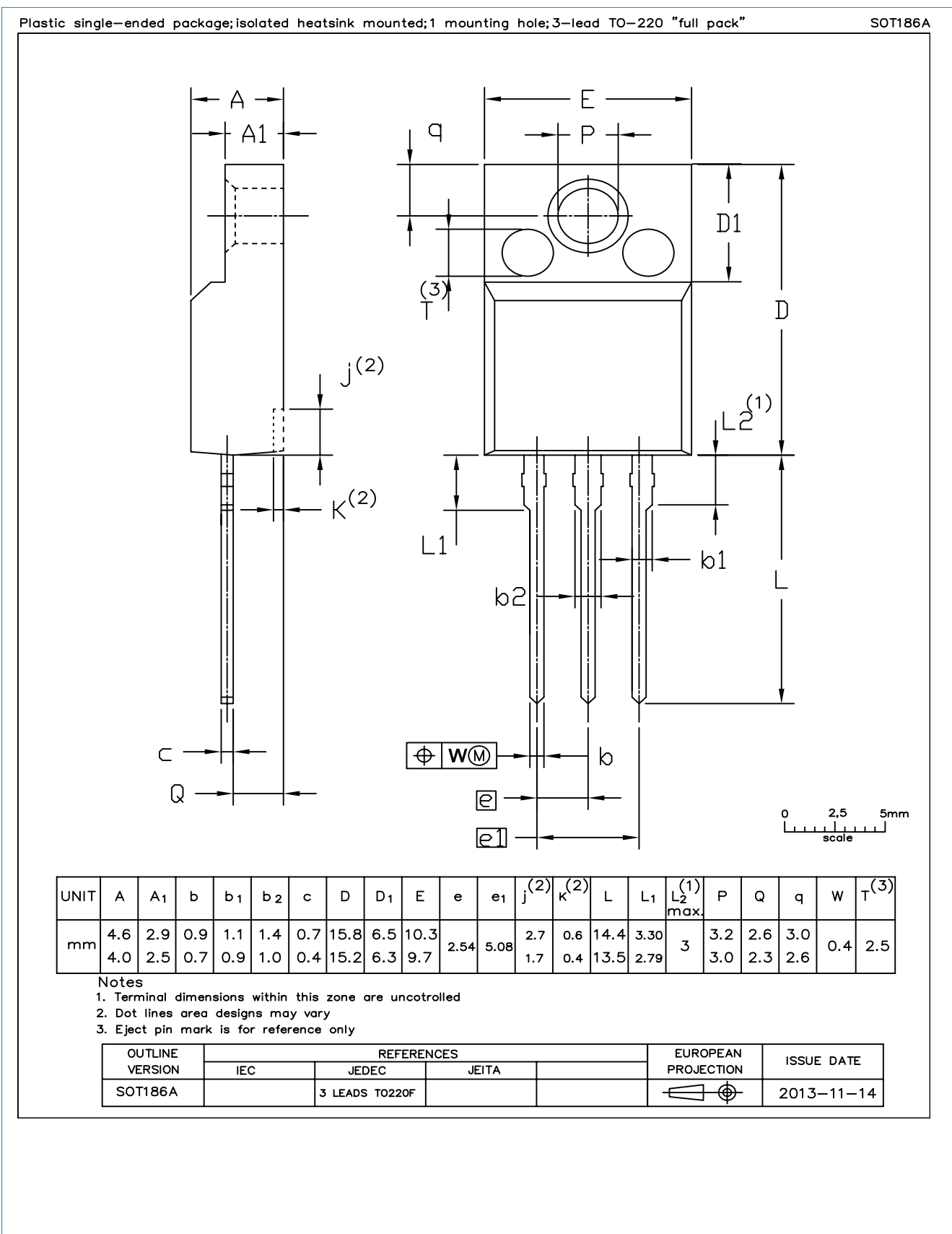


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline



12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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