

**SOURCE DRIVER FOR 240-OUTPUT TFT-LCD
(NAVIGATION, AUTOMOBILE LCD-TV)**

μ PD16448A is a source driver for TFT liquid crystal panels. This IC consists of a multiplexer circuit supporting a variety of pixel arrays, a shift register that generates sampling timing, and two sample and hold circuits that sample analog voltages. Because the two sample and hold circuits alternately execute sampling and holding, a high definition can be obtained.

In addition, simultaneous sampling and successive sampling are automatically selected according to the pixel array of the LCD panel. It is ideal for a wide range of applications, including navigation systems and automobile LCD-TVs.

FEATURES

- Can be driven on 5 V (Dynamic range: 4.3 V, $V_{DD2} = 5.0$ V)
- 240-output
- $f_{max.} = 18$ MHz ($V_{DD1} = 3.0$ V)
- Simultaneous/successive sampling selectable according to pixel array
 - Simultaneous sampling: vertical stripe
 - Successive sampling: delta array, mosaic array
- Two sample and hold circuits
- Low output deviation between pins (± 20 mV MAX.)
- Stripe, delta, and mosaic pixel arrays supported by internal multiplexer circuit
- Left and right shift selected by R/L pin
- Single-side mounting possible

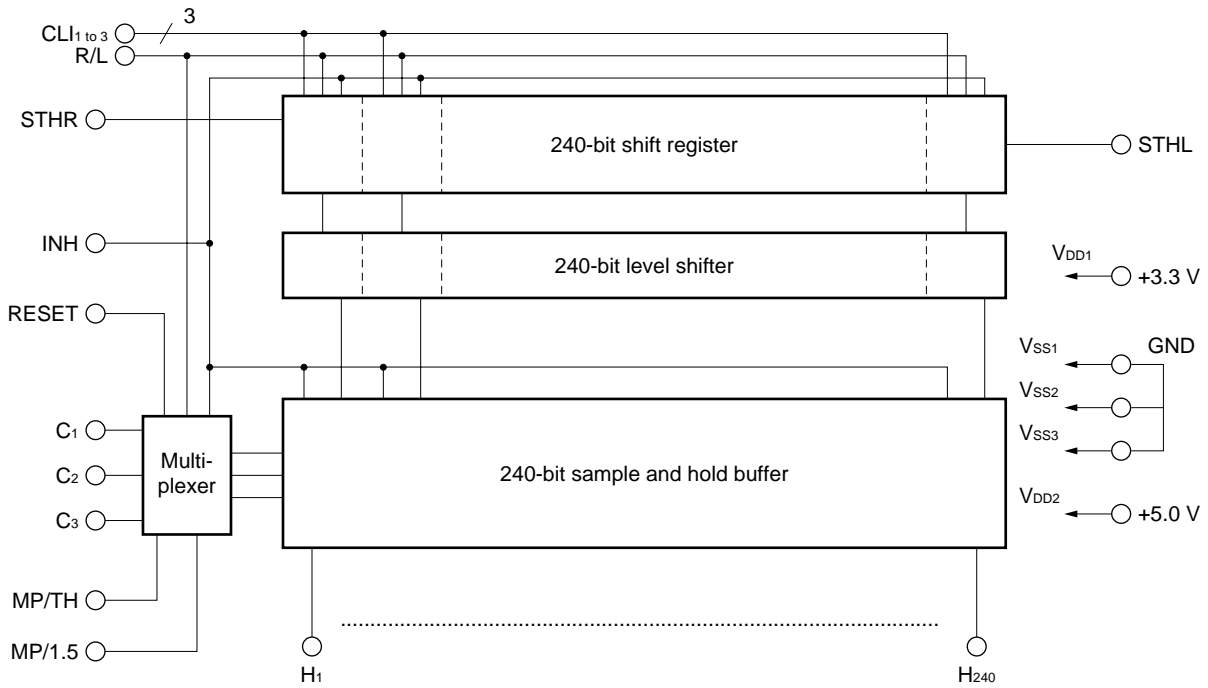
ORDERING INFORMATION

Part Number	Package
μ PD16448AN-xxx	TCP (TAB package)

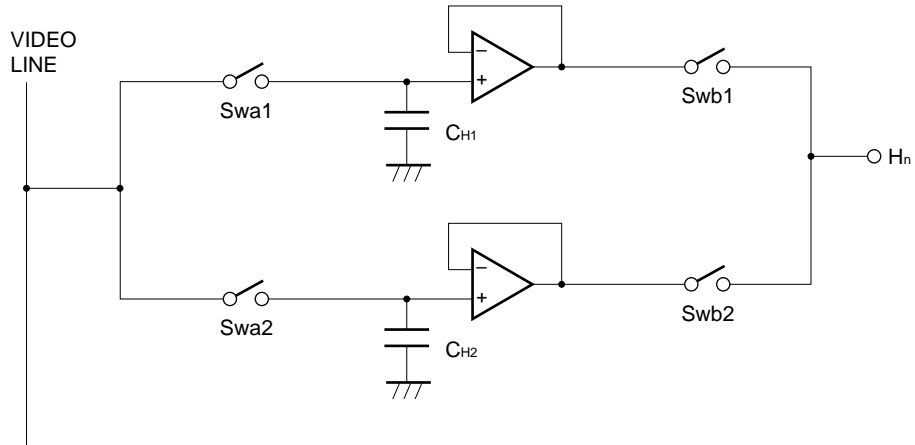
Remark The dimensions of TCP are custom-made. Please consult NEC for details.

The information in this document is subject to change without notice.

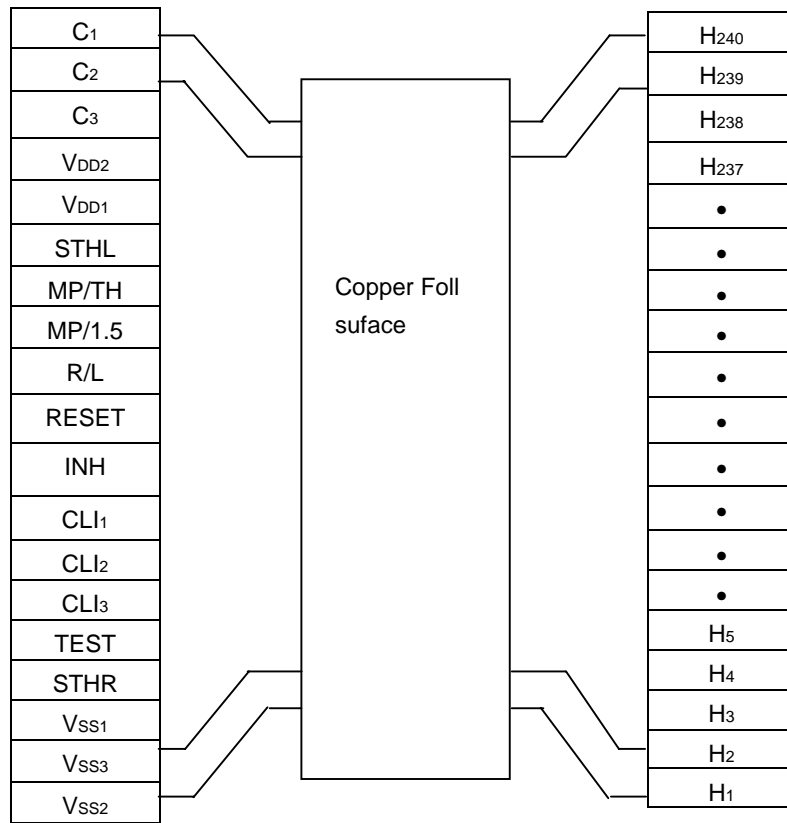
BLOCK DIAGRAM



SAMPLE AND HOLD CIRCUIT AND OUTPUT CIRCUIT



★ PIN CONFIGURATION (μPD16448A N-xxx)



Remark This figure does not specify the TCP package.

1. PIN DESCRIPTION

Symbol	Name	Function															
C ₁ to C ₃	Video signal input	Input R, G, and B video signals.															
H ₁ to H ₂₄₀	Video signal output	Video signal output pins. Output sampled and held video signals during horizontal period.															
STHR STHL	Cascade I/O	Start pulse I/O pins of sample hold timing. STHR serves as an input pin and STHL, as an output pin, in the case of right shift. In the case of left shift, STHL serves as an input pin, and STHR, as an output pin.															
CL ₁ CL ₂ CL ₃	Shift clock input	A start pulse is read at the rising edge of CL ₁ . Sampling pulse SHP _n is generated at the rising edge of CL ₁ through CL ₃ during successive sampling, and at the rising edge of CL ₁ during simultaneous sampling (for details, refer to the Timing charts in 2.FUNCTION DESCRIPTION).															
INH	Inhibit input	Selects a multiplexer and one of the two sample and hold circuits at the falling edge.															
RESET	Reset input	Resets the select counter of the multiplexer and the selector circuit of the two sample and hold circuits when it goes high. After reset, the multiplexer is turned OFF, so sure to input one pulse of the INH signal before inputting the video signal. If the video signal is input without the INH signal, sampling is not executed.															
MP/TH	Multiplexer circuit select input (1)	<p>Four types of color filter arrays can be supported by combination of MP/TH and MP/1.5.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Mode</th> <th>MP/TH</th> <th>MP/1.5</th> </tr> </thead> <tbody> <tr> <td>Vertical stripe array</td> <td>L</td> <td>L</td> </tr> <tr> <td>Single-side delta array</td> <td>L</td> <td>H</td> </tr> <tr> <td>Mosaic array</td> <td>H</td> <td>L</td> </tr> <tr> <td>Double-side delta array</td> <td>H</td> <td>H</td> </tr> </tbody> </table>	Mode	MP/TH	MP/1.5	Vertical stripe array	L	L	Single-side delta array	L	H	Mosaic array	H	L	Double-side delta array	H	H
Mode	MP/TH		MP/1.5														
Vertical stripe array	L	L															
Single-side delta array	L	H															
Mosaic array	H	L															
Double-side delta array	H	H															
MP/1.5	Multiplexer circuit select input (2)																
R/L	Shift direction select input	R/L = H; right shift: STHR → H ₁ → H ₂₄₀ → STHL R/L = L; left shift: STHL → H ₂₄₀ → H ₁ → STHR															
V _{DD1}	Logic power supply	3.0 V to 5.5 V															
V _{DD2}	Driver power supply	5.0 V ± 0.5 V															
V _{SS1}	Logic ground	Connect this pin to ground of system.															
V _{SS2}	Driver ground	Connect this pin to ground of system.															
V _{SS3}	Driver ground	Connect this pin to ground of system.															
TEST	Test pin	Fix this pin to L.															

2. FUNCTION DESCRIPTION

2.1 Multiplexer Circuit

This circuit selects RGB video signals input to the C₁, C₂, and C₃ pins according to the pixel array of the liquid crystal panel, and outputs the signals to the H₁ through H₂₄₀ pins.

Vertical stripe array, single-/double-side delta array, or mosaic array can be selected by using the MP/TH and MP/1.5 pins.

2.1.1 Vertical stripe array mode (MP/TH = L, MP/1.5 = L)

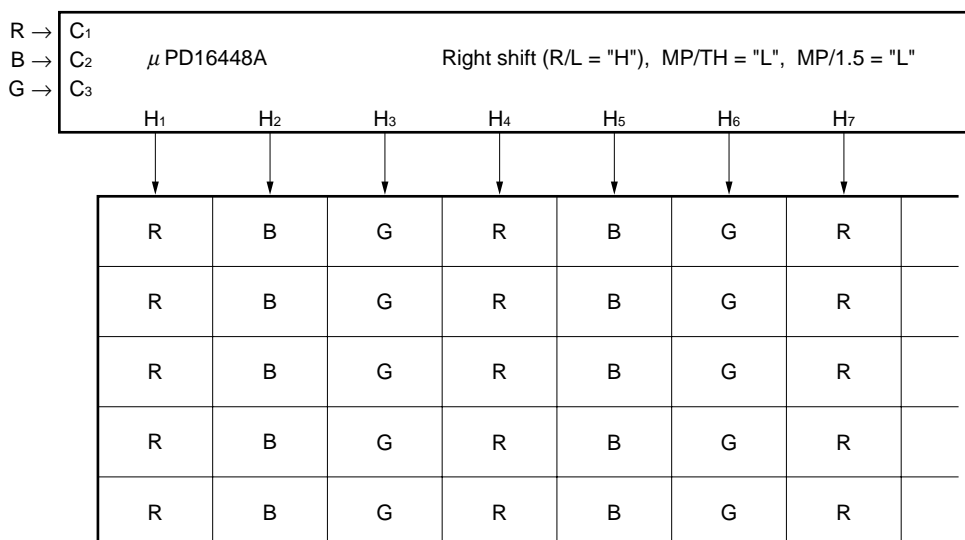
In this mode, the relation between video signals C₁, C₂, and C₃, and output pins is as shown below. This mode is used to drive a panel of vertical stripe array. In this mode, the multiplexer circuit is in the through status.

Relation between video signals C₁, C₂, and C₃, and output pins (during right shift)

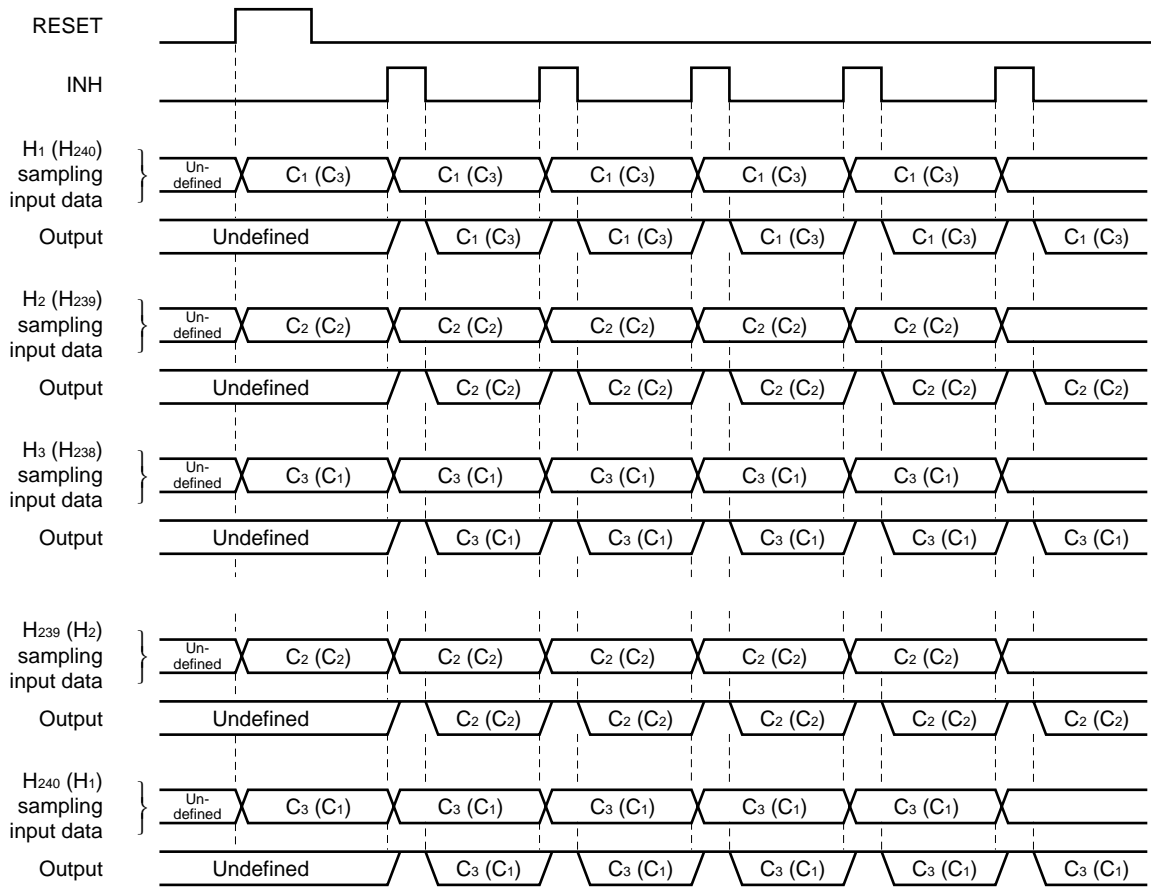
Line No. (number of INHs)	RESET	INH	H ₁ (H ₂₄₀)	H ₂ (H ₂₃₉)	H ₃ (H ₂₃₈)	H ₄ (H ₂₃₇)		H ₂₃₉ (H ₂)	H ₂₄₀ (H ₁)
0	H	L	Sampling C ₁ (C ₃)	Sampling C ₂ (C ₂)	Sampling C ₃ (C ₁)	Sampling C ₁ (C ₃)		Sampling C ₂ (C ₂)	Sampling C ₃ (C ₁)
1	L	↓	Output C ₁ (C ₃)	Output C ₂ (C ₂)	Output C ₃ (C ₁)	Output C ₁ (C ₃)		Output C ₂ (C ₂)	Output C ₃ (C ₁)
2	L	↓	Output C ₁ (C ₃)	Output C ₂ (C ₂)	Output C ₃ (C ₁)	Output C ₁ (C ₃)		Output C ₂ (C ₂)	Output C ₃ (C ₁)
3	L	↓	Output C ₁ (C ₃)	Output C ₂ (C ₂)	Output C ₃ (C ₁)	Output C ₁ (C ₃)		Output C ₂ (C ₂)	Output C ₃ (C ₁)
:	:	:	:	:	:	:		:	:
:	:	:	:	:	:	:		:	:

() indicates the case of left shift.

Pixel arrangement of vertical stripe array and multiplexer operation



Timing chart of vertical stripe array



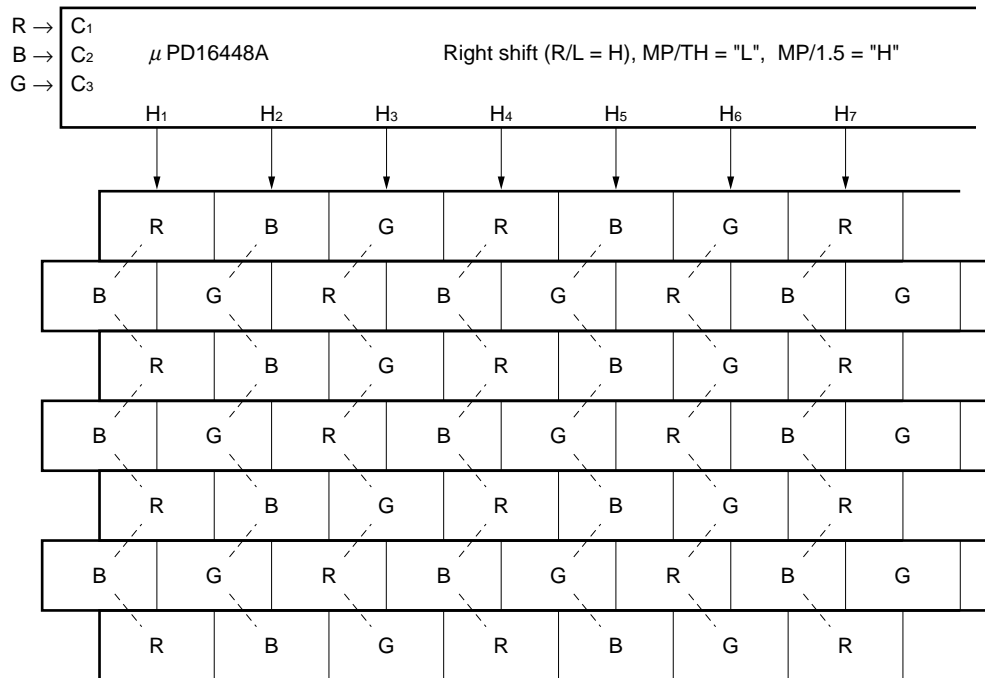
2.1.2 Single-side delta array mode (MP/TH = L, MP/1.5 = H)

Relation between video signals C₁, C₂, and C₃, and output pins

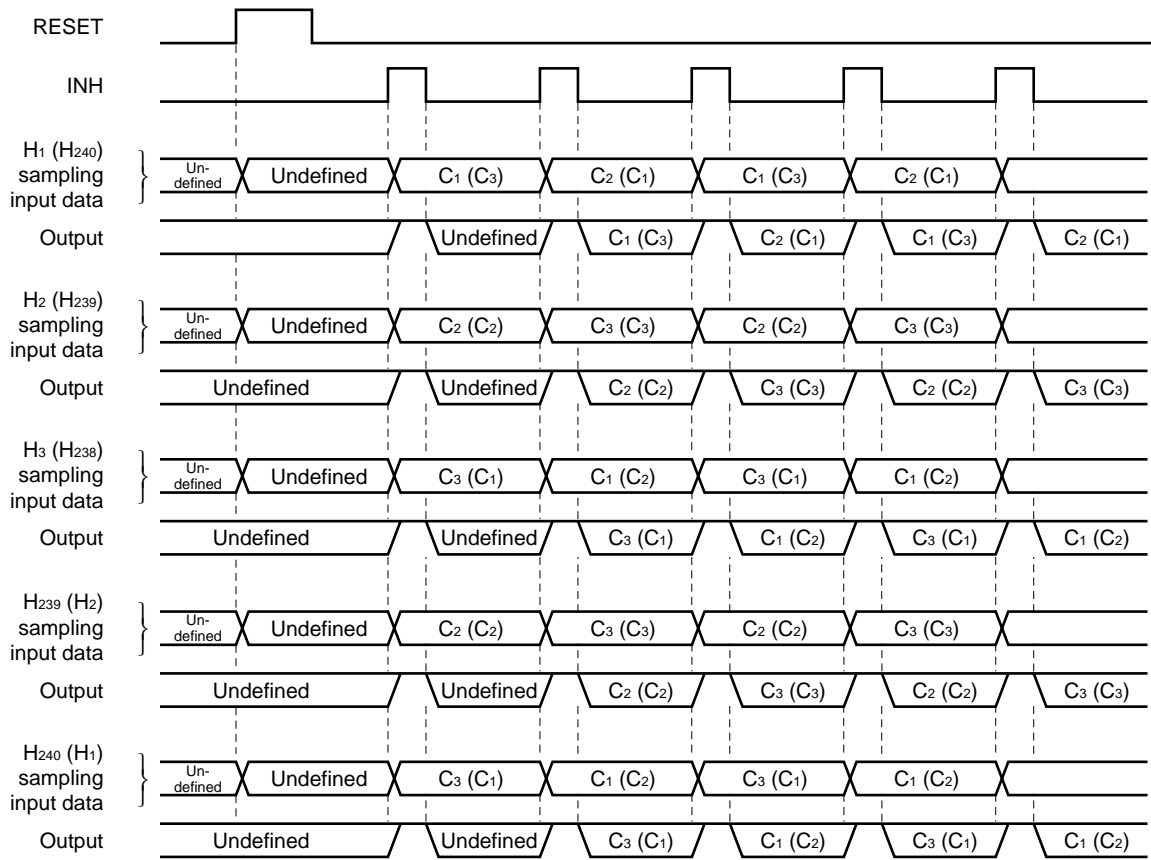
Line No. (number of INHs)	RESET	INH	H ₁ (H ₂₄₀)	H ₂ (H ₂₃₉)	H ₃ (H ₂₃₈)	H ₄ (H ₂₃₇)	H ₂₃₉ (H ₂)	H ₂₄₀ (H ₁)
0	H	L	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
1	L	↓	Sampling C ₁ (C ₃)	Sampling C ₂ (C ₂)	Sampling C ₃ (C ₁)	Sampling C ₁ (C ₃)	Sampling C ₂ (C ₂)	Sampling C ₃ (C ₁)
2	L	↓	Output C ₁ (C ₃)	Output C ₂ (C ₂)	Output C ₃ (C ₁)	Output C ₁ (C ₃)	Output C ₂ (C ₂)	Output C ₃ (C ₁)
3	L	↓	Output C ₂ (C ₁)	Output C ₃ (C ₃)	Output C ₁ (C ₂)	Output C ₂ (C ₁)	Output C ₃ (C ₃)	Output C ₁ (C ₂)
4	L	↓	Output C ₁ (C ₃)	Output C ₂ (C ₂)	Output C ₃ (C ₁)	Output C ₁ (C ₃)	Output C ₂ (C ₂)	Output C ₃ (C ₁)
5	L	↓	Output C ₂ (C ₁)	Output C ₃ (C ₃)	Output C ₁ (C ₂)	Output C ₂ (C ₁)	Output C ₃ (C ₃)	Output C ₁ (C ₂)

() indicates the case of left shift.

Pixel arrangement of single-side delta array and multiplexer operation



Timing chart of single-side delta array



2.1.3 Double-side delta array mode (MP/TH = H, MP/1.5 = H)

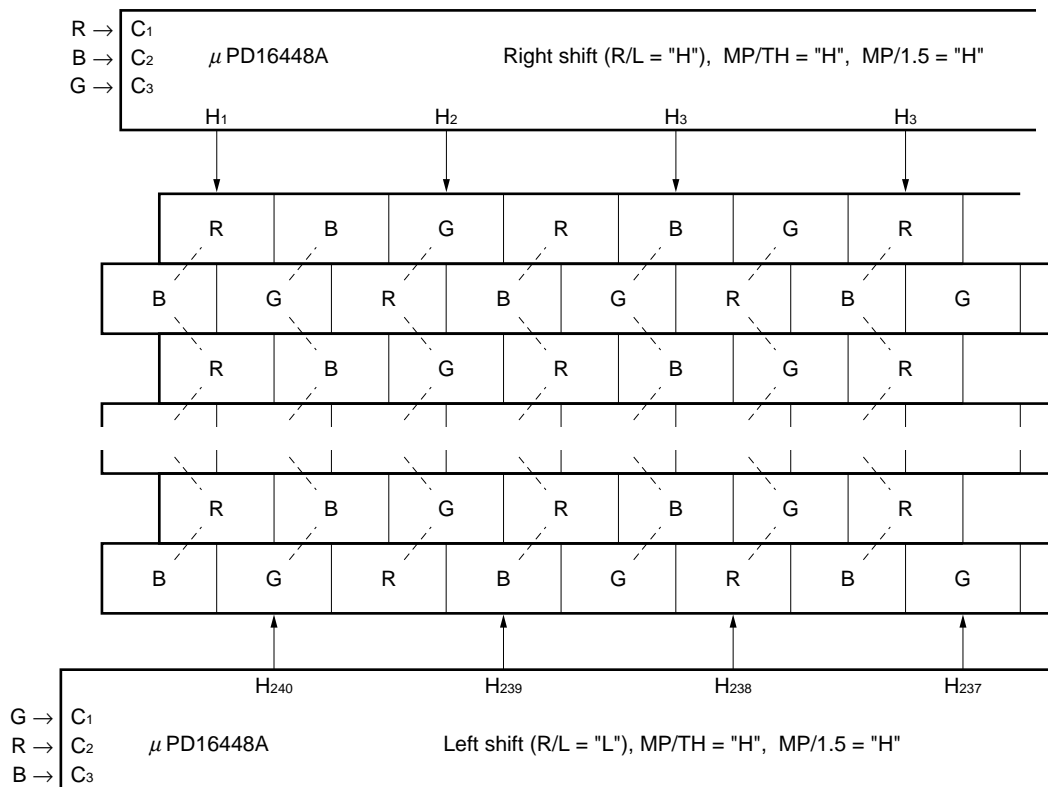
Because the pad pitch of the μPD16448A is designed so that the IC is mounted on one side, the output pitch must be expanded on the TCP if the IC is mounted on both sides.

Relation between video signals C₁, C₂, and C₃, and output pins

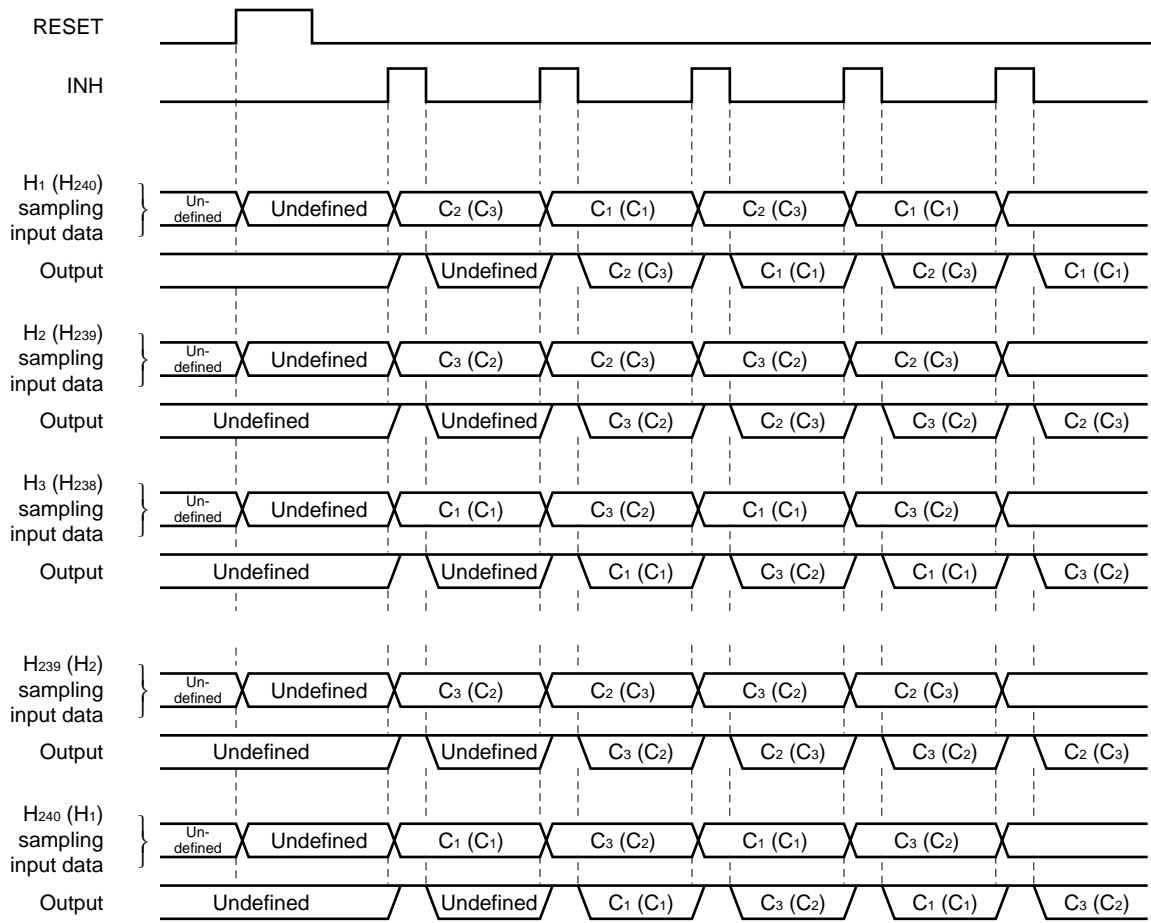
Line No. (number of INHs)	RESET	INH	H ₁ (H ₂₄₀)	H ₂ (H ₂₃₉)	H ₃ (H ₂₃₈)	H ₄ (H ₂₃₇)	H ₂₃₉ (H ₂)	H ₂₄₀ (H ₁)
0	H	L	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
1	L	↓	Sampling C ₂ (C ₃)	Sampling C ₃ (C ₂)	Sampling C ₁ (C ₁)	Sampling C ₂ (C ₃)	Sampling C ₃ (C ₂)	Sampling C ₁ (C ₁)
2	L	↓	Output C ₂ (C ₃)	Output C ₃ (C ₂)	Output C ₁ (C ₁)	Output C ₂ (C ₃)	Output C ₃ (C ₂)	Output C ₁ (C ₁)
3	L	↓	Output C ₁ (C ₁)	Output C ₂ (C ₃)	Output C ₃ (C ₂)	Output C ₁ (C ₁)	Output C ₂ (C ₃)	Output C ₃ (C ₂)
4	L	↓	Output C ₂ (C ₃)	Output C ₃ (C ₂)	Output C ₁ (C ₁)	Output C ₂ (C ₃)	Output C ₃ (C ₂)	Output C ₁ (C ₁)
5	L	↓	Output C ₁ (C ₁)	Output C ₂ (C ₃)	Output C ₃ (C ₂)	Output C ₁ (C ₁)	Output C ₂ (C ₃)	Output C ₃ (C ₂)

() indicates the case of left shift.

Pixel arrangement of double-side delta array and multiplexer operation



Timing chart of double-side delta array



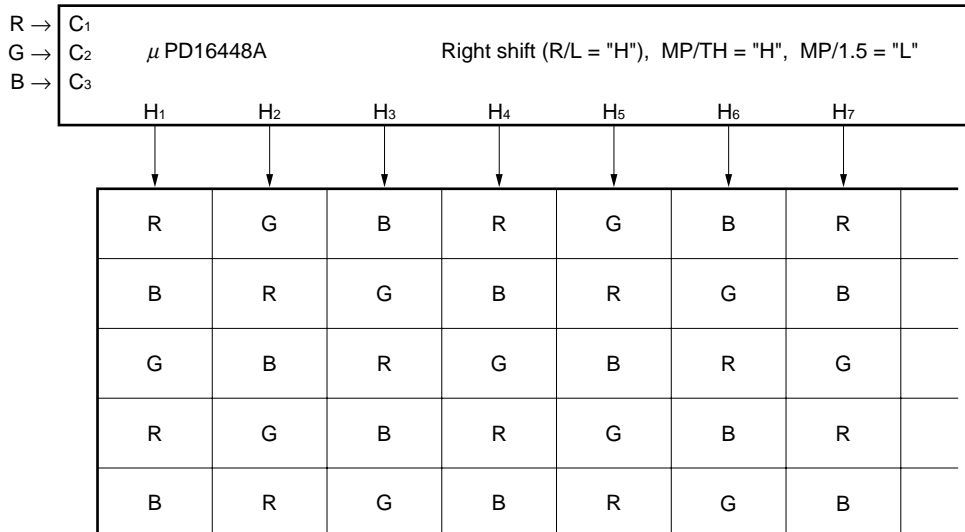
2.1.4 Mosaic array mode (MP/TH = H, MP/1.5 = L)

Relation between video signals C₁, C₂, and C₃, and output pins

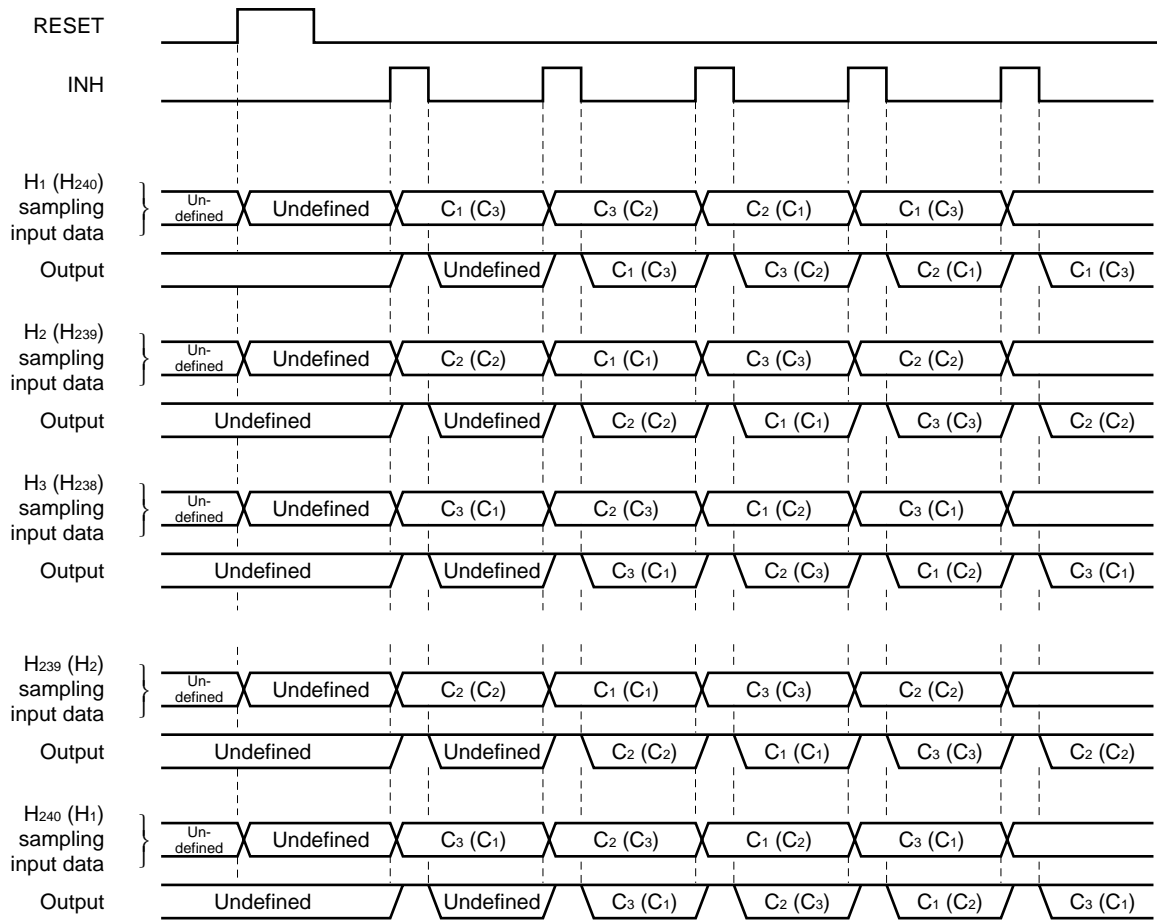
Line No. (number of INHs)	RESET	INH	H ₁ (H ₂₄₀)	H ₂ (H ₂₃₉)	H ₃ (H ₂₃₈)	H ₄ (H ₂₃₇)		H ₂₃₉ (H ₂)	H ₂₄₀ (H ₁)
0	H	L	Undefined	Undefined	Undefined	Undefined		Undefined	Undefined
1	L	↓	Sampling C ₁ (C ₃)	Sampling C ₂ (C ₂)	Sampling C ₃ (C ₁)	Sampling C ₁ (C ₃)		Sampling C ₂ (C ₂)	Sampling C ₃ (C ₁)
2	L	↓	Output C ₁ (C ₃)	Output C ₂ (C ₂)	Output C ₃ (C ₁)	Output C ₁ (C ₃)		Output C ₂ (C ₂)	Output C ₃ (C ₁)
3	L	↓	Output C ₃ (C ₂)	Output C ₁ (C ₁)	Output C ₂ (C ₃)	Output C ₃ (C ₂)		Output C ₁ (C ₁)	Output C ₂ (C ₃)
4	L	↓	Output C ₂ (C ₁)	Output C ₃ (C ₃)	Output C ₁ (C ₂)	Output C ₂ (C ₁)		Output C ₃ (C ₃)	Output C ₁ (C ₂)
5	L	↓	Output C ₁ (C ₃)	Output C ₂ (C ₂)	Output C ₃ (C ₁)	Output C ₁ (C ₃)		Output C ₂ (C ₂)	Output C ₃ (C ₁)
:	:	:	:	:	:	:		:	:
:	:	:	:	:	:	:		:	:

() indicates the case of left shift.

Pixel arrangement of mosaic array and multiplexer operation

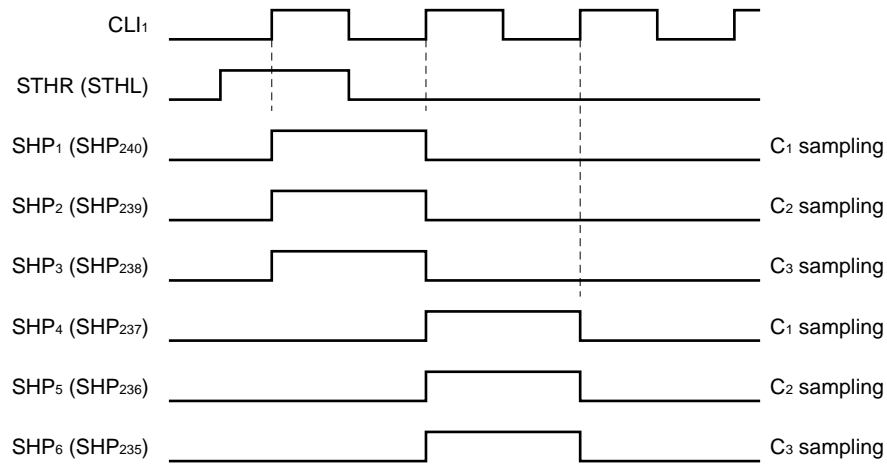


Timing chart of mosaic array



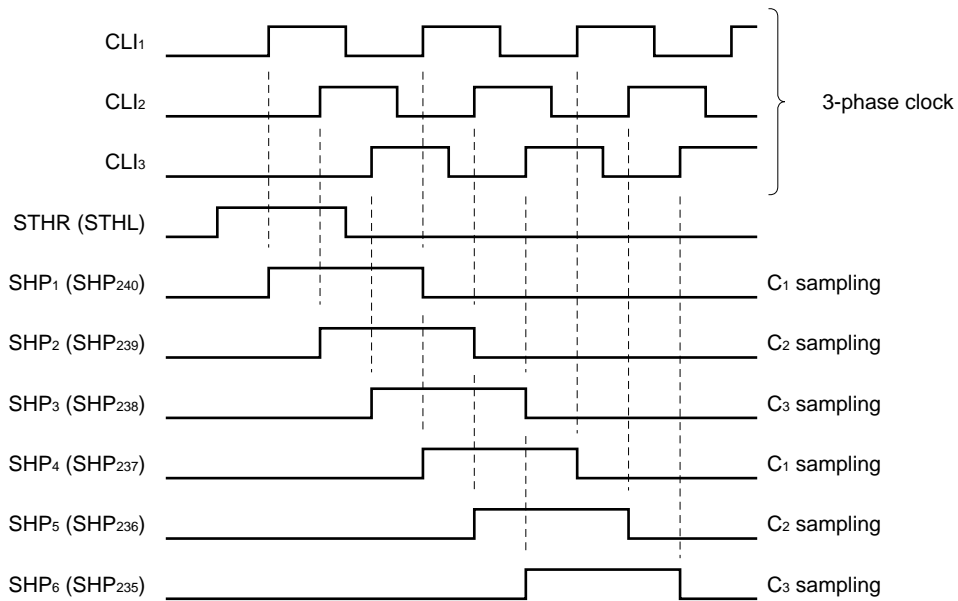
2.1.5 Relation between Shift Clock CLI_n and Internal Sampling Pulse SHP_n

(1) Simultaneous sampling (() indicates the case of left shift.)



Remark C₁ through C₃ are sampled while SHP_n is H.

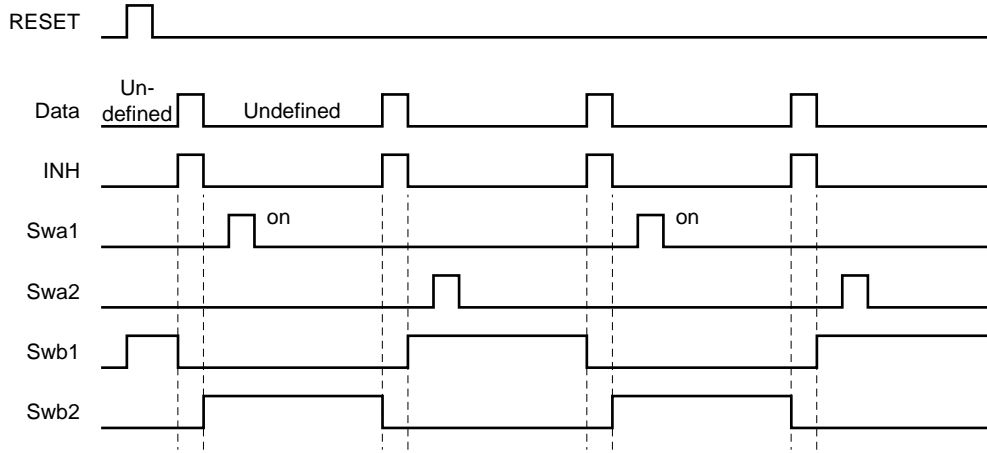
(2) Successive sampling (() indicates the case of left shift.)



- Remarks 1.** Input a three-phase clock to shift clock pins CLI_1 through CLI_3 .
- 2.** The video signals (C₁, C₂, and C₃) are sampled while SHP_n is H.

2.2 Sample and Hold Circuit

The sample and hold circuit samples and holds the video input signals C₁ through C₃ selected by the multiplexer circuit in the timing shown below. Swa1 through Swb2 are reset by the RESET signal and change at the rising and falling edges of the INH signal. (Refer to **BLOCK DIAGRAM**.)



★ 2.3 Write Operation Timing

The sampled video signals are written to the LCD panel by output currents I_{VOL} and I_{VOH} via output buffer. The dynamic range is $4.3 V_{MIN}$. ($V_{DD2} = 5.0 V$).

While $INH = H$, do not stop shift clocks $CL1_1$ through $CL1_3$.

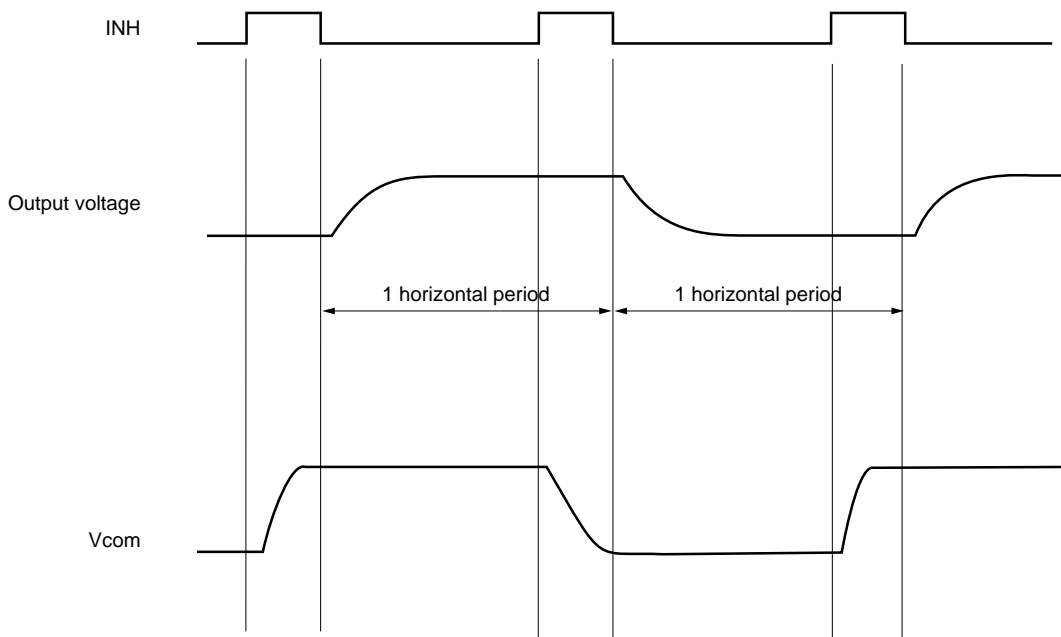
The output operation of this IC is controlled by INH signals.

$INH = HiZ$

$INH =$ Connected with internal circuit

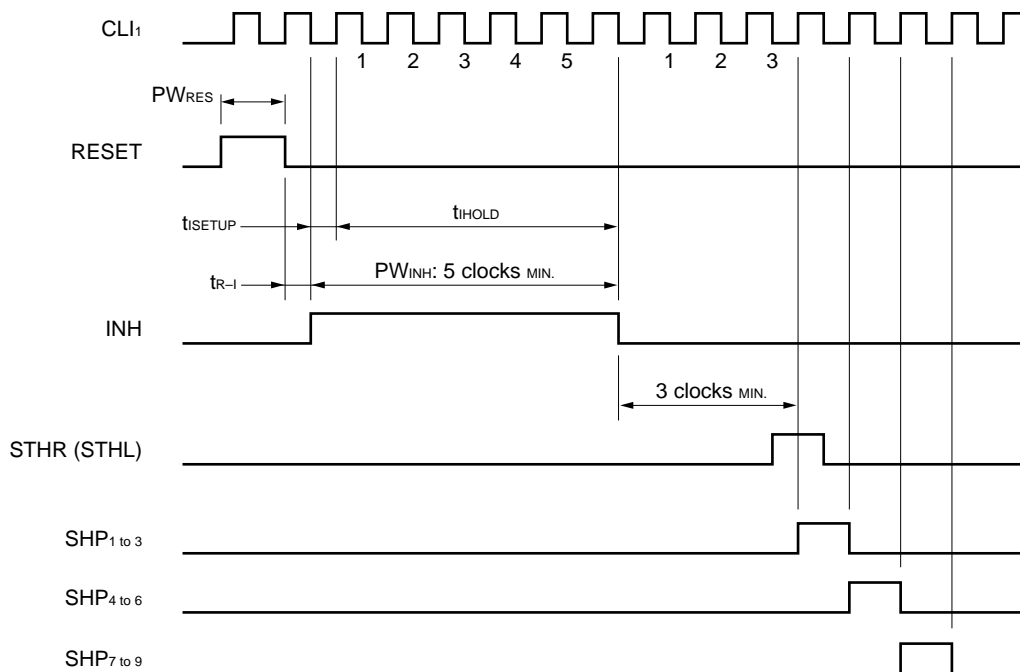
(switch sample and hold circuit at the falling edge.)

Therefore, performing V_{com} inversion while $INH = L$ causes current flow to these IC output pins, which may result in malfunction. Perform V_{com} inversion during $INH = H$ (Hi-z) and start output operation of the next line after the V_{com} signal is stable enough to operate. Make sure to evaluate this output operation sufficiently.



[Cautions on Use]

1. Turn ON power to V_{DD1} , logic input, V_{DD2} , and video signal input in that order to prevent destruction due to latchup, and turn off power in the reverse sequence. Observe this power sequence even during the transition period.
2. This IC is designed to input successive signals such as chrome signals. The input band of the video signals is designed to be 9 MHz MAX. If video signals faster than that are input, display is not performed correctly.
3. Insert a bypass capacitor of 0.1 μF between V_{DD1} and V_{SS1} and between V_{DD2} and V_{SS2} . If the power supply is not reinforced, the sampling voltage may be abnormal if the supply voltage fluctuates.
4. Display may not be correctly performed if noise is superimposed on the start pulse pin. Therefore, be sure to input a reset signal during the vertical blanking period.
5. Even if the start pulse width is extended by half a clock or more, sampling start timing SHP_1 is not affected, and the sampling operation is performed normally.
6. When the multiplexer circuit is used in the vertical stripe mode, C_1 , C_2 , and C_3 are simultaneously sampled at the rising edge of SHP_n . Internally, however, only CLI_1 is valid. Therefore, input a shift clock to CLI_1 only. At this time, keep the CLI_2 and CLI_3 pins to "L". When using the multiplexer circuit in the delta array mode or mosaic array mode, C_1 , C_2 , and C_3 are sequentially sampled. Input a three-phase clock to CLI_1 through CLI_3 . (For the sampling timing, refer to 2. FUNCTION DESCRIPTION.)
7. The recommended timing of t_{R-1} and PW_{RES} on starting is shown below. (The following timing chart shows simultaneous sampling.)
 An INH pulse width of at least 5 clocks is required to reset the internal logic. Unless the INH pulse is input after reset, sampling is not performed in the correct sequence.



3.ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	Ratings	Unit
Logic supply voltage	V _{DD1}		-0.5 to +7.0	V
Driver supply voltage	V _{DD2}		-0.5 to +7.0	V
Logic input voltage	V _I		-0.5 to V _{DD1} +0.5	V
Video input voltage	V _{VI}	C ₁ , C ₂ , C ₃	-0.5 to V _{DD2} +0.5	V
Logic output voltage	V _{O1}		-0.5 to V _{DD1} +0.5	V
Driver output voltage	V _{O2}		-0.5 to V _{DD2} +0.5	V
Driver output current	I _{O2}		±10	mA
Operating temperature range	T _A		-30 to +85	°C
Storage temperature range	T _{stg}		-65 to +125	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

RECOMMENDED OPERATING CONDITIONS (T_A = -30 to +85 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V _{DD1}	3.0	3.3	5.5	V
Driver supply voltage	V _{DD2}	4.5	5.0	5.5	V
Video input voltage	V _{VI}	V _{SS2} + 0.35		V _{DD2} - 0.35	V
Driver output voltage	V _{O2}	V _{SS2} + 0.35		V _{DD2} - 0.35	V
Input voltage, high	V _{IH}	0.7•V _{DD1}		V _{DD1}	V
Input voltage, low	V _{IL}	0		0.3•V _{DD1}	V

ELECTRICAL CHARACTERISTICS

($T_A = -30$ to $+85$ °C, $V_{DD1} = 3.0$ to 5.5 V, $V_{DD2} = 5.0$ V ± 0.5 V, $V_{SS1} = V_{SS2} = 0$ V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Maximum video signal output voltage	V_{VOH}		$V_{DD2} - 0.35$			V
Minimum video signal output voltage	V_{VOL}				0.35	V
Logic output voltage, high	V_{LOH}	STHL, STHR pins $I_{OH} = -1.0$ mA	$0.9 \cdot V_{DD1}$			V
Logic output voltage, low	V_{LOL}	STHL, STHR pins $I_{OL} = 1.0$ mA			$0.1 \cdot V_{DD1}$	V
Video signal output current, high	I_{VOH}	INH = L $V_O = V_{DD2} - 0.5$ V		-0.20	-0.08	mA
Video signal output current, low	I_{VOL}	INH = L $V_{of} = 1.0$ V, $V_O = 0.5$ V	-0.08	0.20		mA
Reference voltage 1	V_{REF1}	$V_{DD2} = 5.0$ V, $T_A = 25$ °C $V_{V1} = 0.5$ V		0.49		V
Reference voltage 2	V_{REF2}	$V_{DD2} = 5.0$ V, $T_A = 25$ °C $V_{V1} = 2.0$ V		1.99		V
Reference voltage 3	V_{REF3}	$V_{DD2} = 5.0$ V, $T_A = 25$ °C $V_{V1} = 3.5$ V		3.49		V
Output voltage deviation 1	ΔV_{VO1}	$V_{DD2} = 5.0$ V, $T_A = 25$ °C $V_{V1} = 0.5$ V			± 20	mV
Output voltage deviation 2	ΔV_{VO2}	$V_{DD2} = 5.0$ V, $T_A = 25$ °C $V_{V1} = 2.0$ V			± 20	mV
Output voltage deviation 3	ΔV_{VO3}	$V_{DD2} = 5.0$ V, $T_A = 25$ °C $V_{V1} = 3.5$ V			± 20	mV
Logic input leakage current	I_{LL}				± 1.0	μA
Video input leakage current	I_{VL}				± 10	μA
Logic dynamic current consumption	I_{DD1}	$f_{CL1} = 14$ MHz $V_{V1} = 2.0$ V, no load $f_{INH} = 15.4$ kHz $PW_{INH} = 5.0$ μs	$V_{DD1} = 3.3 \pm 0.3$ V		2.5	mA
			$V_{DD1} = 5.0 \pm 0.5$ V		4.0	
Driver dynamic current consumption	I_{DD2}	$f_{CL1} = 14$ MHz $V_{V1} = 2.0$ V, no load $f_{INH} = 15.4$ kHz $PW_{INH} = 5.0$ μs			10.0	mA

Remarks 1. V_{of} : output applied voltage, V_O : output voltage without load

2. The reference values are typical values only. The output deviation is only guaranteed within the chip.

SWITCHING CHARACTERISTICS ($T_A = -30$ to $+85$ °C, $V_{DD1} = 3.0$ to 5.5 V, $V_{DD2} = 5.0 \pm 0.5$ V, $V_{SS1} = V_{SS2} = 0$ V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start pulse propagation delay time	t_{PHL}	$C_L = 20$ pF	10		54	ns
	t_{PLH}	$C_L = 20$ pF	10		54	ns
Maximum clock frequency 1	$f_{max. 1}$		15			MHz
Maximum clock frequency 2	$f_{max. 2}$	With 3-phase clock input	8			MHz
Logic input capacitance	C_{I1}	Other than STHL, STHR			15	pF
STHL, STHR input capacitance	C_{I2}	STHL, STHR			20	pF
Video input capacitance	C_3	C_1 to C_3 , $V_{VI} = 2.0$ V			50	pF

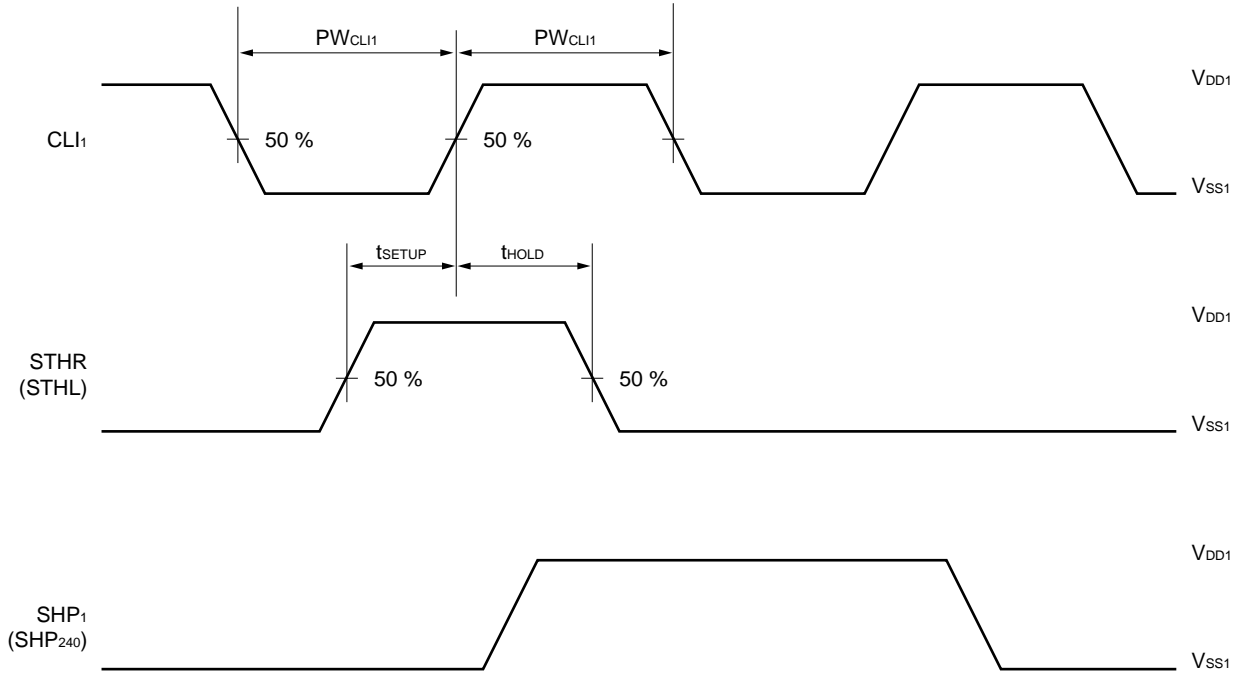
TIMING REQUIREMENTS ($T_A = -30$ to $+85$ °C, $V_{DD1} = 3.0$ to 5.5 V, $V_{DD2} = 5.0 \pm 0.5$ V, $V_{SS1} = V_{SS2} = 0$ V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW_{CLI}	Duty = 50 %	33			ns
Start pulse setup time	t_{SETUP}		8			ns
Start pulse hold time	t_{HOLD}		8			ns
Reset pulse width	PW_{RES}		66			ns
INH setup time	t_{ISETUP}		33			ns
INH hold time	t_{IHOLD}		33			ns
Reset-INH time	t_{R-I}		81			ns
INH pulse width	PW_{INH}		5			CLK

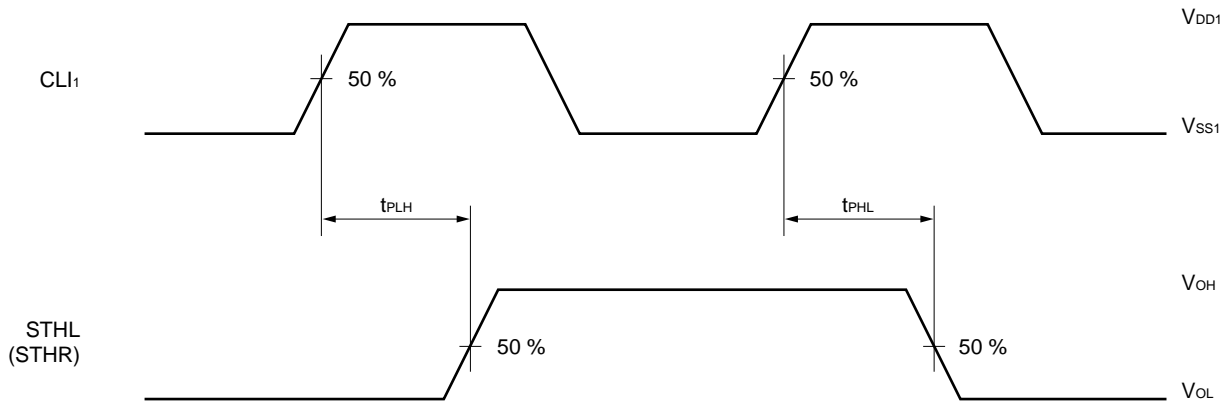
Remark Keep the rise and fall times of the logic input signals to within $t_r = t_f = 5$ ns (10 to 90%).
As an example, the switching characteristic wave of CLL_1 is defined on the next page.

SWITCHING CHARACTERISTIC WAVE (simultaneous/successive sampling)

Start Pulse Input Timing

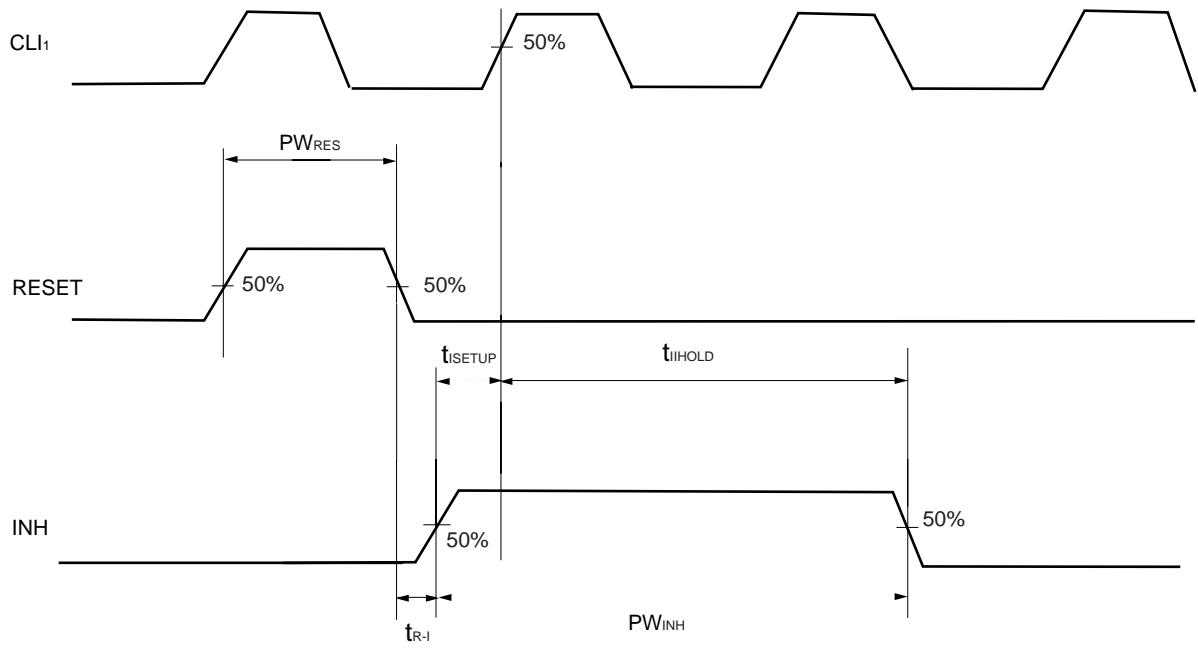


Start Pulse Output Timing



Remark The input/output timing of the start pulse is the same for simultaneous/successive sampling.

★ RESET INH Pulse Timing



4. RECOMMENDED CONDITIONS FOR INSTALLATION

This product should be installed under the following recommended conditions. Consult one of our sales representatives for installation under conditions other than those recommended.

Installation Condition	Installation Method	Condition
Thermocompression bonding	Soldering	Heat with heating tool at 300 °C to 350 °C under pressure of 100 g (per pin) for 2 to 3 seconds
	ACF (sheet type adhesive agent)	Temporary adhesion at 70 °C to 100 °C under pressure of 3 to 8 kg/cm ² for 3 to 5 seconds Permanent adhesion at 165 °C to 180 °C under pressure of 25 to 45 kg/cm ² for 30 to 40 seconds (when aeolotropic conductive film SUMIZAC 1003 from Sumitomo Bakelite Co., Ltd. is used)

Caution For installation conditions for the ACF part, contact the ACF manufacturer beforehand. Do not mix different installation methods.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

REFERENCE

NEC Semiconductor Device Reliability/Quality Control System	C10983E
Quality Grade on NEC Semiconductor Devices	C11531E

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.