

# 2SD0973, 2SD0973A (2SD973, 2SD973A)

Silicon NPN epitaxial planer type

For low-frequency power amplification

## Features

- Low collector to emitter saturation voltage  $V_{CE(sat)}$
- M type package allowing easy automatic and manual insertion as well as stand-alone fixing to the printed circuit board.

## Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Collector to base voltage	$V_{CBO}$	30	V
2SD0973A		60	
Collector to emitter voltage	$V_{CEO}$	25	V
2SD0973A		50	
Emitter to base voltage	$V_{EBO}$	5	V
Peak collector current	$I_{CP}$	1.5	A
Collector current	$I_C$	1	A
Collector power dissipation	$P_C^*$	1	W
Junction temperature	$T_j$	150	°C
Storage temperature	$T_{stg}$	-55 ~ +150	°C

\* Printed circuit board: Copper foil area of 1cm<sup>2</sup> or more, and the board thickness of 1.7mm for the collector portion

## Electrical Characteristics (Ta=25°C)

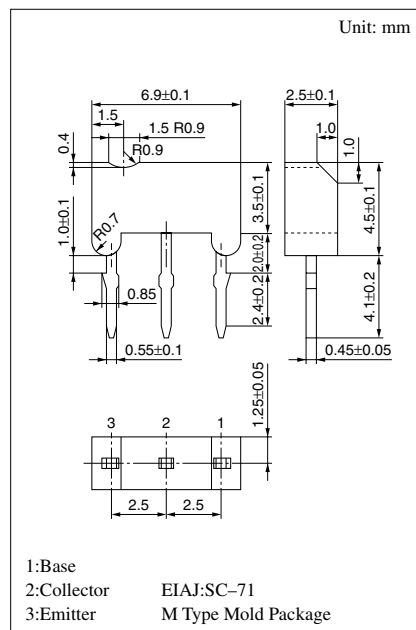
Parameter	Symbol	Conditions	min	typ	max	Unit
Collector cutoff current	$I_{CBO}$	$V_{CB} = 20V, I_E = 0$			0.1	μA
Collector to base voltage	$V_{CBO}$	$I_C = 10\mu A, I_E = 0$	30			V
			60			
Collector to emitter voltage	$V_{CEO}$	$I_C = 2mA, I_B = 0$	25			V
			50			
Emitter to base voltage	$V_{EBO}$	$I_E = 10\mu A, I_C = 0$	5			V
Forward current transfer ratio	$h_{FE1}^{*1}$	$V_{CE} = 10V, I_C = 500mA^{*2}$	85	160	340	
	$h_{FE2}$	$V_{CE} = 5V, I_C = 1A^{*2}$	50	100		
Collector to emitter saturation voltage	$V_{CE(sat)}$	$I_C = 500mA, I_B = 50mA^{*2}$		0.2	0.4	V
Base to emitter saturation voltage	$V_{BE(sat)}$	$I_C = 500mA, I_B = 50mA^{*2}$		0.85	1.2	V
Transition frequency	$f_T$	$V_{CB} = 10V, I_E = -50mA, f = 200MHz$		200		MHz
Collector output capacitance	$C_{ob}$	$V_{CB} = 10V, I_E = 0, f = 1MHz$		11	20	pF

<sup>\*2</sup> Pulse measurement

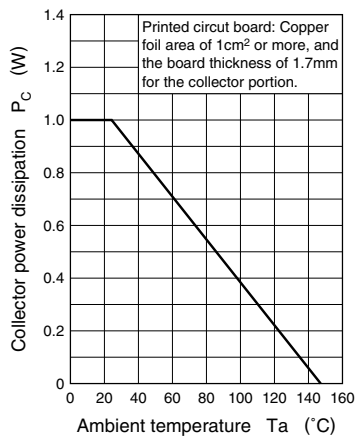
<sup>\*1</sup> $h_{FE1}$  Rank classification

Rank	Q	R	S
$h_{FE1}$	85 ~ 170	120 ~ 240	170 ~ 340

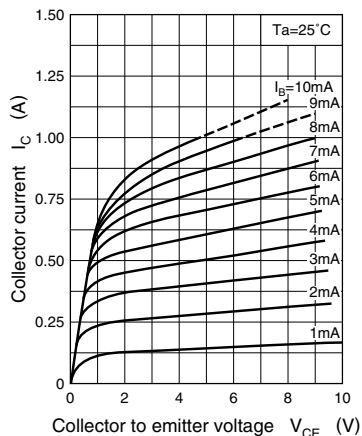
Note.) The Part numbers in the Parenthesis show conventional part number.



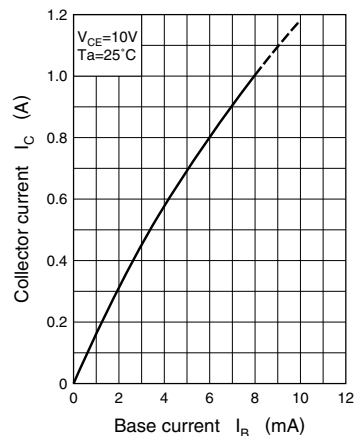
$P_C - T_a$



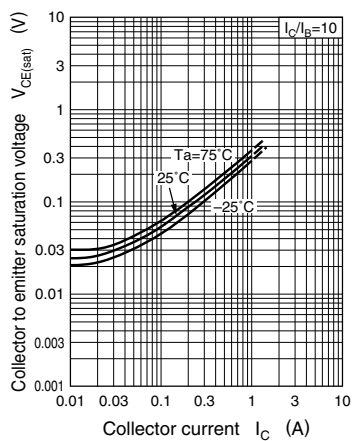
$I_C - V_{CE}$



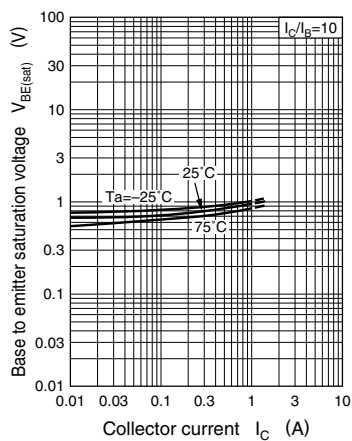
$I_C - I_B$



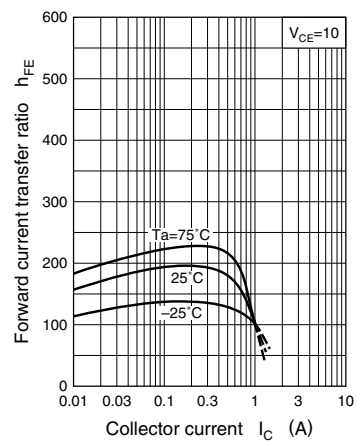
$V_{CE(sat)} - I_C$



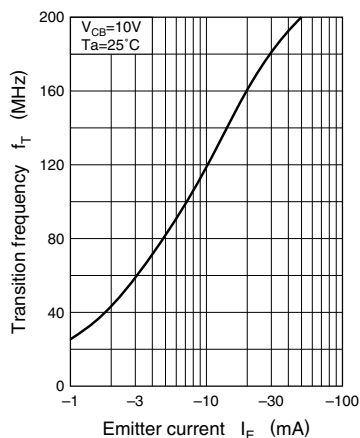
$V_{BE(sat)} - I_C$



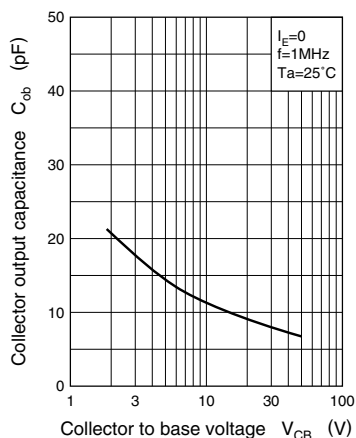
$h_{FE} - I_C$



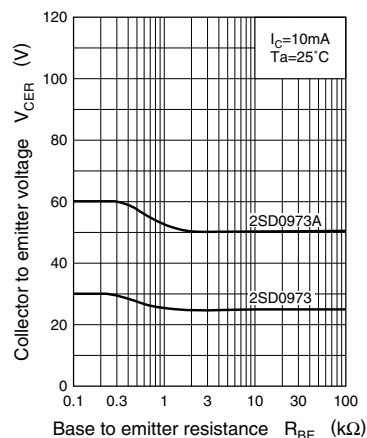
$f_T - I_E$

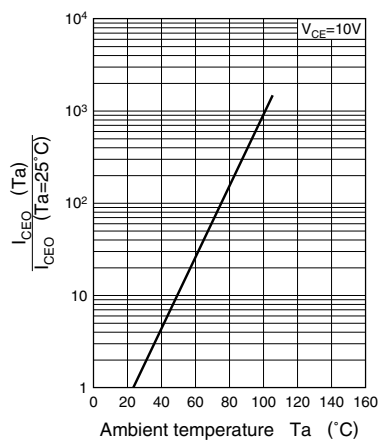


$C_{ob} - V_{CB}$

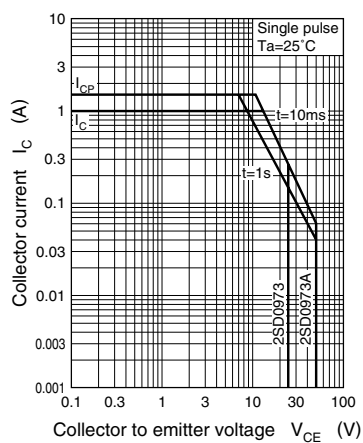


$V_{CER} - R_{BE}$



$I_{CEO} - T_a$ 

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