



AFE1203

2Mbps, Single Pair HDSL ANALOG FRONT END

FEATURES

- E1/T1 SINGLE PAIR 2B1Q OPERATION
- COMPLETE ANALOG INTERFACE
- 385mW POWER DISSIPATION
- PROGRAMMABLE POWER

- 48-LEAD SSOP PACKAGE
- SCALEABLE DATA RATE
- OPERATION FROM 2.3Mbps TO 160kbps
- +5V ONLY (5V OR 3.3V DIGITAL)
- -40°C TO +85°C OPERATION

DESCRIPTION

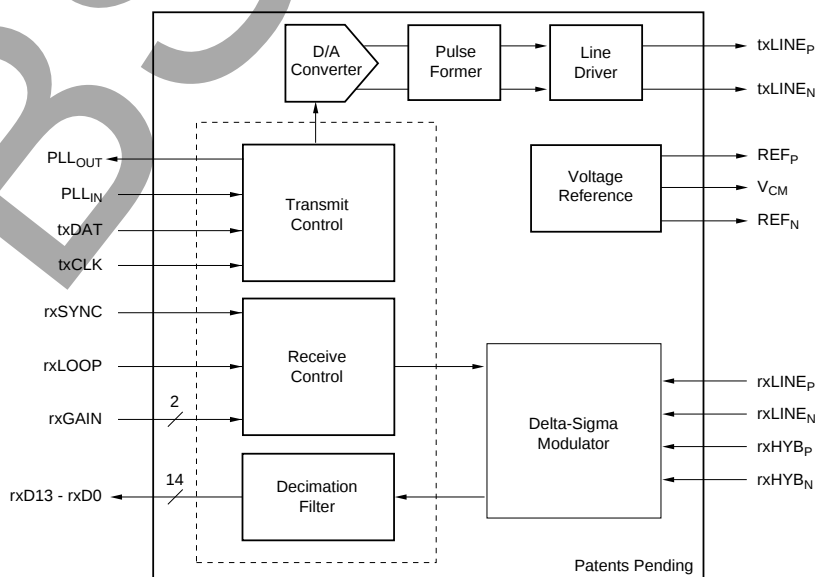
Burr-Brown's Analog Front End greatly reduces the size and cost of a single pair HDSL (High bit rate Digital Subscriber Line) system by providing all of the active analog circuitry needed to connect an HDSL digital signal processor to an external compromise hybrid and an HDSL line transformer. The transmit and receive filter responses automatically change with clock frequency, allowing the AFE1203 to operate over a wide range of data rates. The power dissipation of the device can be reduced under digital control for operation at lower speeds. The AFE1203 will operate at bit rates from 160kbps to 2.3Mbps. It meets ETSI PSD specifications for single pair E1, as well as ETSI and ANSI PSD specifications for two pair E1 and T1.

Functionally, this unit consists of a transmit and a receive section. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section filters and digitizes the symbol data received on the telephone line. This IC operates

on a single 5V supply. The digital circuitry in the unit can be connected to a supply from 3.3V to 5V. The chip uses only 385mW for full-speed operation. It is housed in a small 48-lead SSOP package.

The receive channel is designed around a fourth-order delta-sigma analog-to-digital converter. It includes a difference amplifier designed to be used with an external compromise hybrid for first-order analog echo cancellation. A programmable gain amplifier with gains 0dB to +9dB is also included. The delta-sigma modulator, operating at a 24X oversampling ratio, produces a 14-bit output at symbol rates up to 1168kHz (for 2.3Mbps operation).

The transmit channel consists of a digital-to-analog converter and switched-capacitor pulse forming network followed by a differential line driver. The pulse forming network receives symbol data and generates a standard 2B1Q output waveform. The differential line driver uses a composite output stage combining class B operation (for high efficiency driving large signals) with class AB operation (to minimize crossover distortion).



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

Typical at 25°C, AV_{DD} = +5V, DV_{DD} = +3.3V, f_{TX} = 1168kHz (E1 single pair rate) and Normal Power mode, unless otherwise specified.

PARAMETER	COMMENTS	AFE1203E			UNITS
		MIN	TYP	MAX	
RECEIVE CHANNEL					
Number of Inputs	Differential	2			
Input Voltage Range	Balanced Differential ⁽¹⁾		±3.0		V
Common-Mode Voltage	1.5V CMV Recommended		+1.5		V
Input Impedance	All Inputs		See Typical Performance Curves		
Input Capacitance			10		pF
Input Gain Matching	Line Input vs Hybrid Input		±2		%
Resolution					Bits
Programmable Gain	Four Gains: 0dB, 3.25dB, 6dB, and 9dB	14			
Settling Time	Gain, rxSYNC, or Power Mode Change ⁽⁸⁾		6		Symbol Periods
Gain + Offset Error	Tested at Each Gain Range		5		%FSR ⁽²⁾
Output Data Coding			Binary Two's Complement		
Data Rate	Normal Power	384		2320	kbps
	Medium Power	192		1168	kbps
	Low Power	160		320	kbps
	Normal Power, rxSYNC ⁽³⁾	196		1168	kHz
TRANSMIT CHANNEL					
Transmit Clock Rate, f _{TX}	Symbol Rate, Normal Power	196		1168	kHz
	Symbol Rate, Medium Power	96		584	kHz
	Symbol Rate, Low Power	80		160	kHz
Transmit -3dB Point	2320kbps		485		kHz
	1168kbps		292		kHz
	784kbps		196		kHz
Transmit Power ⁽⁴⁾		13	13.5	14	dBm
Pulse Output			See Typical Performance Curves		
Common-Mode Voltage, V _{CM}			AV _{DD} /2		V
Output Resistance ⁽⁵⁾	DC to 1MHz		1		Ω
TRANSCEIVER PERFORMANCE					
Uncancelled Echo ⁽⁶⁾	rxGAIN = 0dB, Loopback Enabled			-67	dB
	rxGAIN = 0dB, Loopback Disabled			-67	dB
	rxGAIN = 3.25dB, Loopback Disabled			-69	dB
	rxGAIN = 6dB, Loopback Disabled			-71	dB
	rxGAIN = 9dB, Loopback Disabled			-73	dB
DIGITAL INTERFACE⁽⁵⁾					
Logic Levels					
V _{IH}	I _{IH} < 10μA	DV _{DD} - 1		DV _{DD} + 0.3	V
V _{IL}	I _{IL} < 10μA	-0.3		+0.8	V
V _{OH}	I _{OH} = -20μA	DV _{DD} - 0.5			V
V _{OL}	I _{OL} = 20μA			+0.4	V
POWER					
Analog Power Supply Voltage	Specification		5		V
	Operating Range	4.75		5.25	V
Digital Power Supply Voltage	Specification		3.3		V
	Operating Range	3.15		5.25	V
Power Dissipation ^(4, 7)	Normal Power		385		mW
	Medium Power		300		mW
	Low Power		240		mW
Power Dissipation ⁽⁷⁾	Normal Power, DV _{DD} = 5V		415		mW
PSRR			55		dB
TEMPERATURE RANGE					
Operating ⁽⁵⁾		-40		+85	°C

NOTES: (1) With a balanced differential signal, the positive input is 180° out of phase with the negative input, therefore the actual voltage swing about the common mode voltage on each pin is ±1.5V to achieve a differential input range of ±3.0V or 6Vp-p. (2) FSR is Full-Scale Range. (3) The output data is available at twice the symbol rate with interpolated values. (4) With a pseudo-random equiprobable sequence of HDSL pulses; 13.5dBm applied to the transformer (27dBm output from txLINE_P and txLINE_N). (5) Guaranteed by design and characterization. (6) Uncancelled Echo is a measure of the total analog errors in the transmitter and receiver sections including the effect of non-linearity and noise. See the Discussion of Specifications section of this data sheet for more information. (7) Power dissipation includes only the power dissipated within the component and does not include power dissipated in the external loads. The AFE1203 is tested with a 1:2 line transformer. (8) This is the settling time required for any gain change, change of rxSYNC or any change of power mode.

PIN DESCRIPTIONS

PIN #	TYPE	NAME	DESCRIPTION
1	Ground	AGND	Analog Ground for PLL
2	Power	AV _{DD}	Analog Supply (+5V) for PLL
3	Input	txCLK	Symbol Clock
4	Input	txDAT _N	XMITB Line
5	Input	txDAT _P	XMIT Line
6	Output	rxD0	ADC Output Bit-0
7	Output	rxD1	ADC Output Bit-1
8	Output	rxD2	ADC Output Bit-2
9	Output	rxD3	ADC Output Bit-3
10	Output	rxD4	ADC Output Bit-4
11	Output	rxD5	ADC Output Bit-5
12	Ground	DGND	Digital Ground
13	Power	DV _{DD}	Digital Supply (+3.3V to +5V)
14	Output	rxD6	ADC Output Bit-6
15	Output	rxD7	ADC Output Bit-7
16	Output	rxD8	ADC Output Bit-8
17	Output	rxD9	ADC Output Bit-9
18	Output	rxD10	ADC Output Bit-10
19	Output	rxD11	ADC Output Bit-11
20	Output	rxD12	ADC Output Bit-12
21	Output	rxD13	ADC Output Bit-13
22	Input	PWSEL	Power Control
23	Input	rxSYNC	ADC Sync Signal
24	Input	rxGAIN0	Receive Gain Control Bit-0
25	Input	rxGAIN1	Receive Gain Control Bit-1
26	Input	rxLOOP	Loopback Control Signal (loopback is enabled by positive signal)
27	Power	AV _{DD}	Analog Supply (+5V)
28	Input	rxHYB _N	Negative Input from Hybrid Network
29	Input	rxHYB _P	Positive Input from Hybrid Network
30	Input	rxLINE _N	Negative Line Input
31	Input	rxLINE _P	Positive Line Input
32	Ground	AGND	Analog Ground
33	Ground	AGND	Analog Ground
34	Output	REF _P	Positive Reference Output, Nominally 3.5V
35	Output	V _{CM}	Common-Mode Voltage (buffered), Nominally 2.5V
36	Output	REF _N	Negative Reference Output, Nominally 1.5V
37	Power	AV _{DD}	Analog Supply (+5V)
38	Ground	AGND	Analog Ground
39	Output	txLINE _N	Transmit Line Output Negative
40	Power	AV _{DD}	Analog Supply (+5V)
41	Output	txLINE _P	Transmit Line Output Positive
42	Ground	AGND	Analog Ground
43	NC	NC	Connection to Ground Recommended
44	NC	NC	Connection to Ground Recommended
45	NC	NC	Connection to Ground Recommended
46	NC	NC	Connection to Ground Recommended
47	Output	PLL _{OUT}	PLL Filter Output
48	Input	PLL _{IN}	PLL Filter Input

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: Current	$\pm 100\text{mA}$, Momentary
	$\pm 10\text{mA}$, Continuous
Voltage	AGND -0.3V to $\text{AV}_{\text{DD}} + 0.3\text{V}$
Analog Outputs Short Circuit to Ground ($+25^\circ\text{C}$)	Continuous
AV_{DD} to AGND	-0.3V to 6V
DV_{DD} to DGND	-0.3V to 6V
PLL _{IN} or PLL _{OUT} to AGND	-0.3V to $\text{AV}_{\text{DD}} + 0.3\text{V}$
Digital Input Voltage to DGND	-0.3V to $\text{DV}_{\text{DD}} + 0.3\text{V}$
Digital Output Voltage to DGND	-0.3V to $\text{DV}_{\text{DD}} + 0.3\text{V}$
AGND, DGND Differential Voltage	0.3V
Junction Temperature (T_j)	$+150^\circ\text{C}$
Storage Temperature Range	-40°C to $+125^\circ\text{C}$
Lead Temperature (soldering, 3s)	$+260^\circ\text{C}$
Power Dissipation	700mW

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
AFE1203E	48-Lead SSOP	333	-40°C to $+85^\circ\text{C}$

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

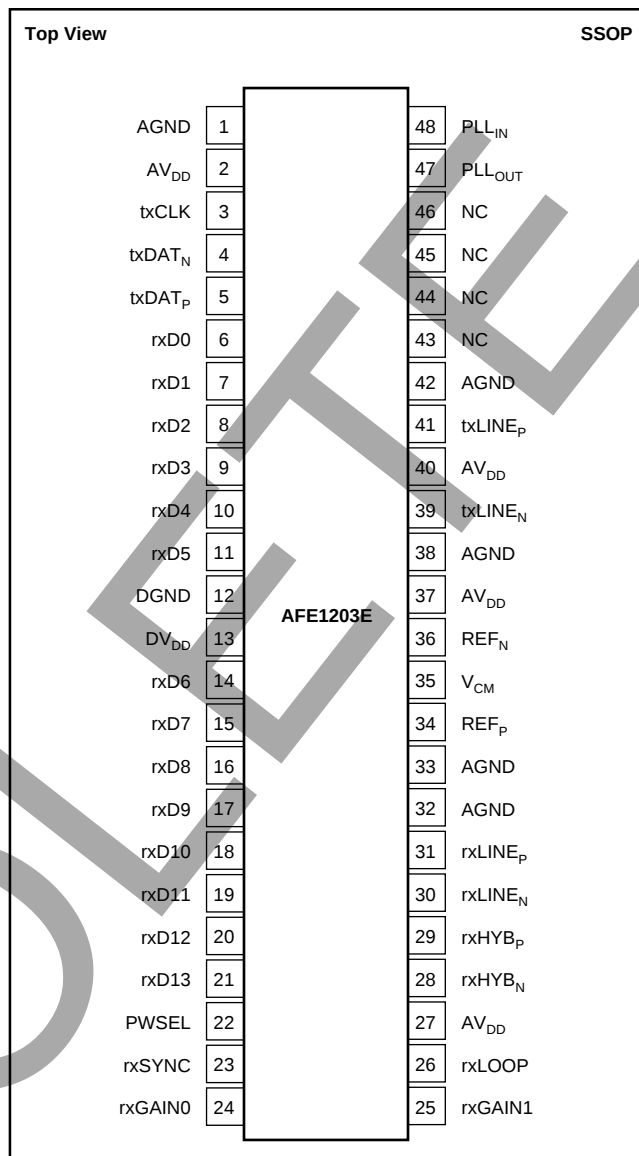


ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

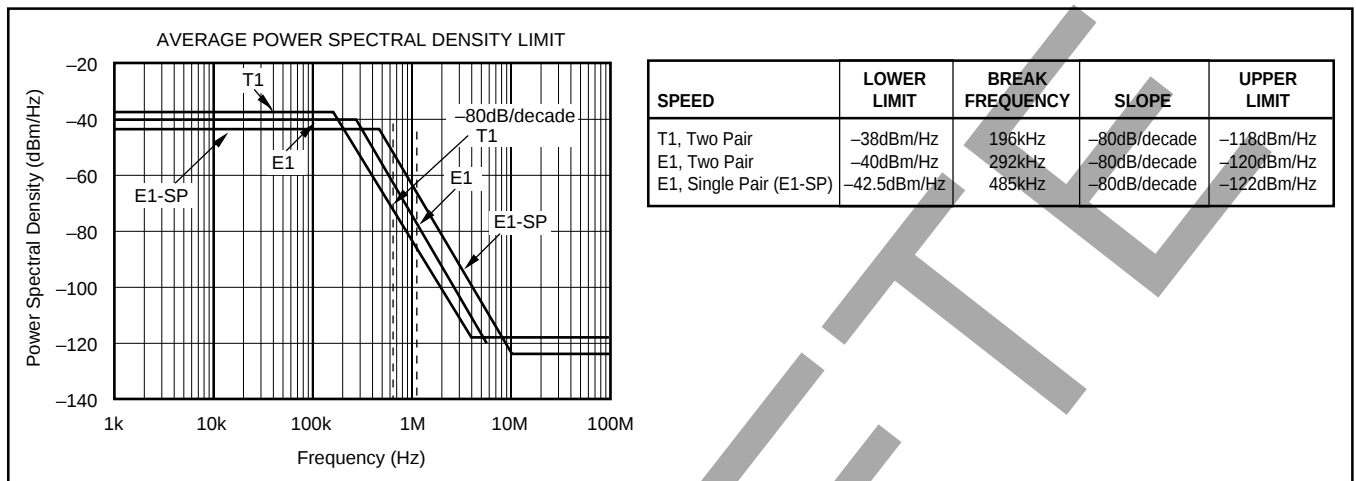
PIN CONFIGURATION



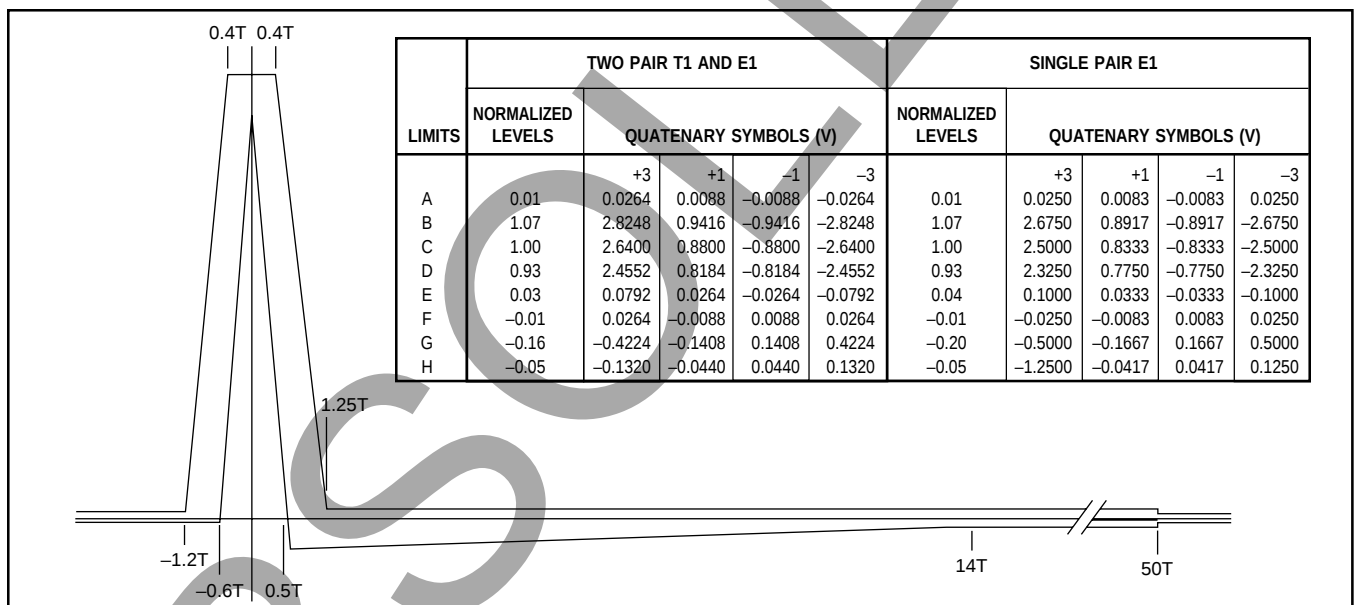
TYPICAL PERFORMANCE CURVES

At Output of Pulse Transformer

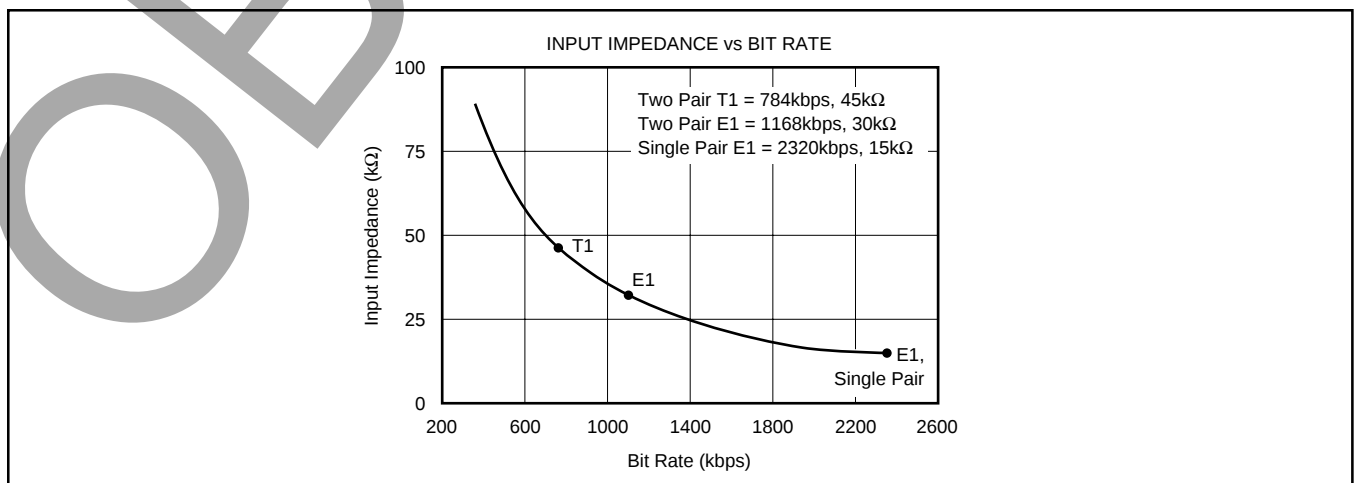
Typical at 25°C, $AV_{DD} = +5V$, and $DV_{DD} = +3.3V$, unless otherwise specified.



CURVE 1. Upper Bound of Power Spectral Density Measured at the Transformer Output.



CURVE 2. Transmitted Pulse Template and Actual Performance as Measured at the Transformer Output.



CURVE 3. Input Impedance of rxLINE and rxHYB.

THEORY OF OPERATION

The transmit channel consists of a D/A converter and a switched-capacitor pulse forming network followed by a differential line driver. The pulse forming network receives symbol data from the DSP and generates a 2B1Q output waveform. The output meets the pulse mask and power spectral density requirements defined in European Telecommunications Standards Institute document RTR/TM-03036 for E1 mode and in sections 6.2.1 and 6.2.2.1 of Bellcore technical advisory TA-NWT-001210 for T1 mode. The differential line driver uses a composite output stage combining class B operation (for high efficiency driving large signals) with class AB operation (to minimize crossover distortion).

The receive channel is designed around a fourth-order delta sigma A/D converter. It includes a difference amplifier designed to be used with an external compromise hybrid for first-order analog crosstalk reduction. A programmable gain amplifier with gains of 0dB to +9dB is also included. The delta sigma modulator operating at a 24X oversampling ratio produces 14 bits of resolution at output rates up to 584kHz. The basic functionality of the AFE1203 is illustrated in Figure 1.

The receive channel operates by summing the two differential inputs, one from the line (rxLINE) and the other from the compromise hybrid (rxHYB). The connection of these two inputs so that the hybrid signal is subtracted from the line signal is described in the paragraph titled "Echo Cancellation in the AFE". The equivalent gain for each input in the difference amp is 1. The resulting signal then passes to a programmable gain amplifier which can be set for gains of 0dB through 9dB. The ADC converts the signal to a 14-bit digital word, rxD13-rxD0.

SCALEABLE TIMING

The AFE1203 scales operation with the clock frequency. All internal filters, the A/D converter, the D/A converter, and the pulse former change frequency with the clock speed so that the unit can be used at different frequencies by changing the clock speed.

rxLOOP INPUT

rxLOOP is the loopback control signal. When enabled, the rxLINE_P and rxLINE_N inputs are disconnected from the AFE. The rxHYB_P and rxHYB_N inputs remain connected. Loopback is enabled by applying a positive signal (Logic 1) to rxLOOP.

ECHO CANCELLATION IN THE AFE

The rxHYB input is designed to be subtracted from the rxLINE input for first-order echo cancellation. To accomplish this, note that the rxLINE input is connected to the same polarity signal at the transformer (positive to positive and negative to negative) while the rxHYB input is connected to opposite polarity through the compromise hybrid (negative to positive and positive to negative) as shown in Figure 2.

RECEIVE DATA CODING

The data from the receive channel A/D converter is coded in Straight Offset Binary.

ANALOG INPUT	OUTPUT CODE (rxD13 - rxD0)
Positive Full Scale	11111111111111
Negative Full Scale	00000000000000

RECEIVE CHANNEL PROGRAMMABLE GAIN AMPLIFIER

The gain of the amplifier at the input of the Receive Channel is set by two gain control pins, rxGAIN1 and rxGAIN0. The resulting gain between 0dB and +9dB is shown below.

rxGAIN1	rxGAIN0	GAIN
0	0	0dB
0	1	3.25dB
1	0	6dB
1	1	9dB

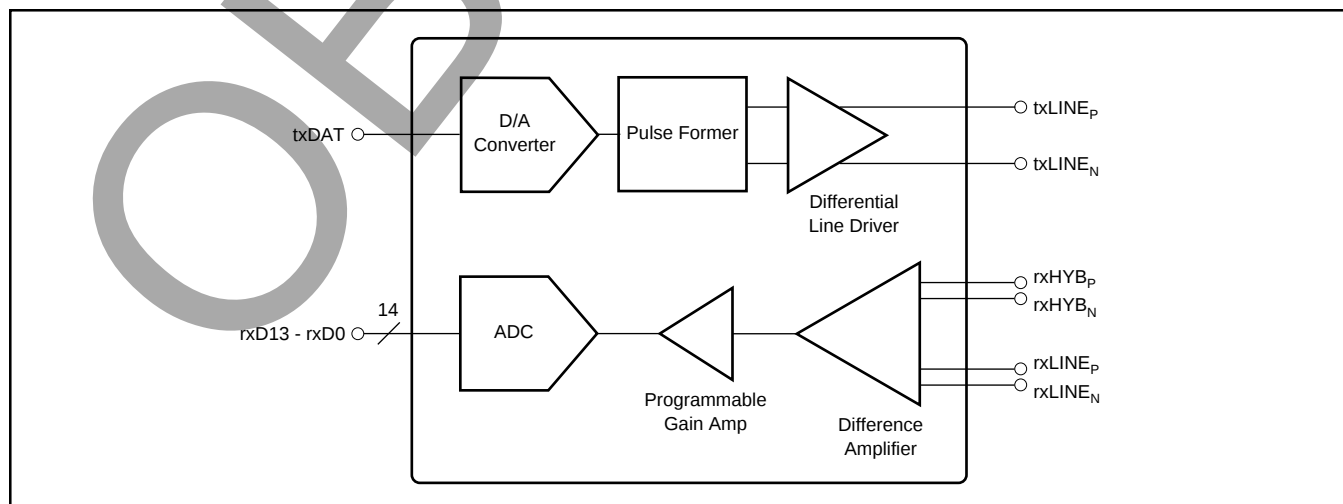


FIGURE 1. Functional Block Diagram of AFE1203.

TIMING DIAGRAM

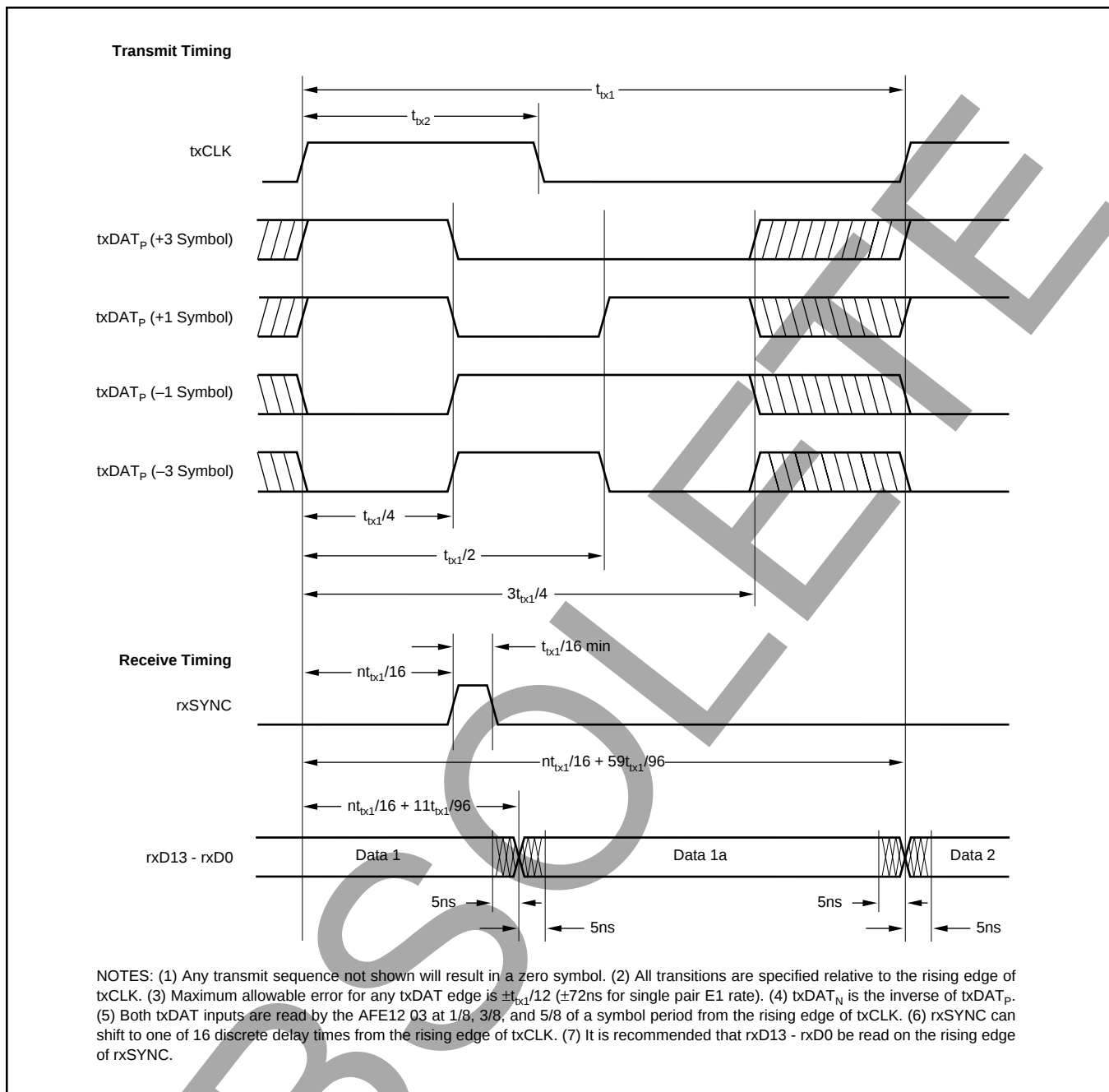


FIGURE 3. Timing Diagram.

RECEIVE TIMING

The rxSYNC signal controls portions of the A/D converter's decimation filter and the data output timing of the A/D converter. It is generated at the symbol rate by the user and must be synchronized with txCLK. The leading edge of rxSYNC can occur at the leading edge of txCLK or it can be shifted by the user in increments of 1/16 of a symbol period to one of 15 discrete delay times after the leading edge of txCLK.

RECEIVE OUTPUT DATA RATE

The receive channel delta-sigma A/D converter of the AFE1203 uses a modulator which operates at an oversampling

rate of 24X the symbol rate. The A/D converter's decimation filter downsamples the modulator output by a factor of 12. The bandwidth of the decimation filter is equal to one-half the symbol rate. This yields two output words per symbol period. These two output words are shown as Data 1 and Data 1a in Figure 3. The specifications of the AFE1203 assume that one A/D converter output is used per symbol period and the other output is ignored. The Receive Timing diagram above suggests using the rising edge of the rxSYNC pulse to read the first data output in a symbol period. Either data output may be used. Both data outputs may be used for more flexible post-processing.

DISCUSSION OF SPECIFICATIONS

UNCANCELLED ECHO

The key measure of transceiver performance is uncanceled echo. This measurement is made as shown in the diagram of Figure 4. The AFE is connected to an output circuit including a typical 1:2 line transformer. The line is simulated by a 135Ω resistor. Symbol sequences are generated by the tester and applied both to the AFE and to the input of an adaptive filter. The output of the adaptive filter is subtracted from the AFE output to form the uncanceled echo signal. Once the filter taps have converged, the rms value of the uncanceled echo is calculated. Since there is no far-end signal source or additive line noise, the uncanceled echo contains only noise and linearity errors generated in the transmitter and receiver.

The data sheet value for uncanceled echo is the ratio of the rms uncanceled echo (referred to the receiver input through the receiver gain) to the nominal transmitted signal (13.5dBm into 135Ω, or 1.74Vrms). This echo value is measured under a variety of conditions: with loopback enabled (line input disconnected); with loopback disabled under all receiver gain ranges; and with the line shorted (S_1 closed in Figure 4).

PROGRAMMABLE POWER DISSIPATION

The power dissipation of the AFE1203 is digitally programmable by the user to three levels: Normal, Medium, and Low. The maximum bit rate of the AFE1203 is 2.3Mbps with Normal power dissipation. At lower power dissipation

levels, the maximum bit rate is lower and in addition, the minimum bit rate is lower. The power control pin (pin 22) has three input levels, Logic 1, Logic 0, and high impedance. In the high impedance state, up to 20μA leakage current can be tolerated out of the power control pin. The AFE1203 requires six baud periods to settle after a change in the power control pin status.

Typical power dissipation specifications, shown in Table I, assume a 5V analog supply, a 3.3V digital supply, standard 13.5dBm delivered to the line, a pseudo random equiprobable sequence of HDSL output pulses, and a 1:2 turns ratio line transformer. The power dissipation specifications include all power dissipated in the AFE1203—it does not include power dissipated in the external load. The external power is 16.5dBm, 13.5dBm to the line and 13.5dBm to the impedance matching resistors. The external power of 16.5dBm is 45mW. If a 5V digital supply is used rather than a 3.3V supply, the power dissipation increases by approximately 3mW.

POWER LEVEL	MAXIMUM SPEED (Mbps)	MINIMUM SPEED (kbps)	TYPICAL POWER DISSIPATION (mW)	PIN 22 INPUT
Normal	2.320	384	385	Logic 1
Medium	1.168	192	300	Logic 0
Low	0.320	160	240	High Impedance

TABLE I. Power Control Operation.

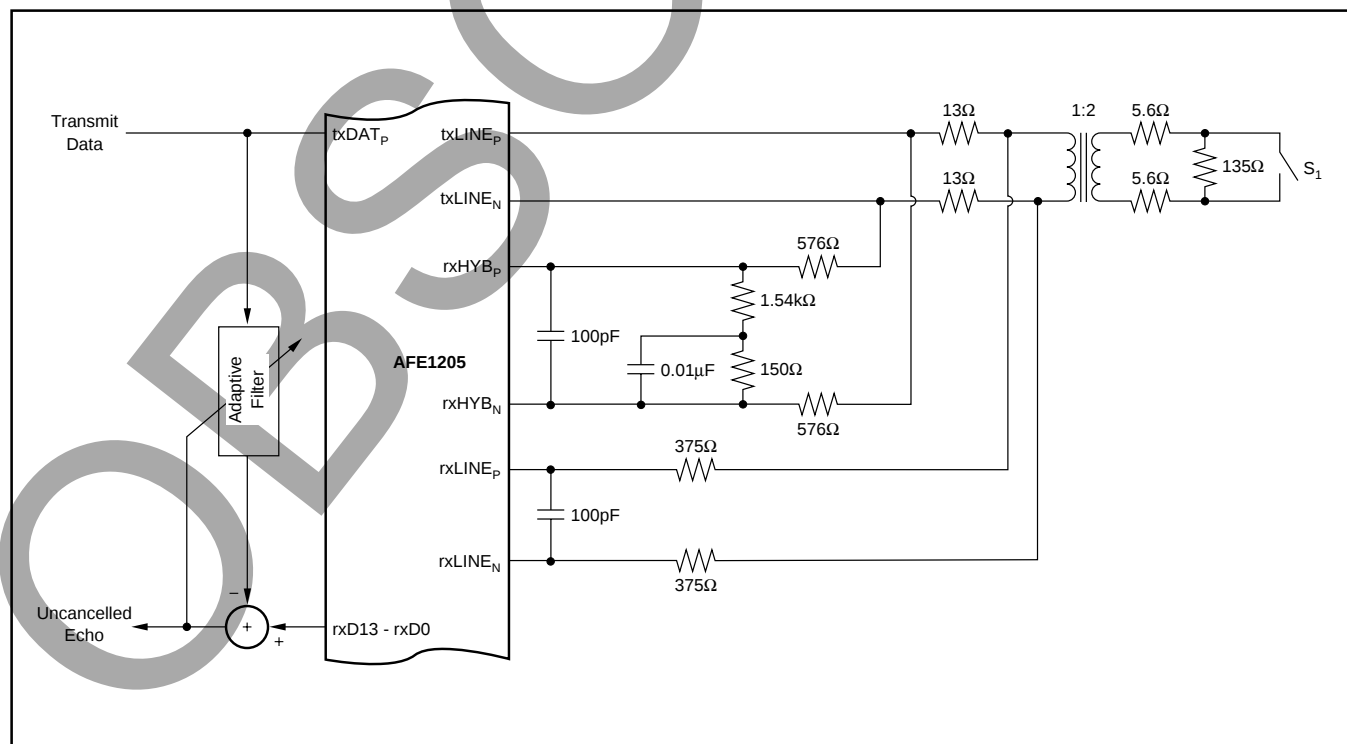


FIGURE 4. Uncanceled Echo Test Diagram.

LAYOUT

The analog front end of an HDSL system has a number of conflicting requirements. It must accept and deliver digital outputs at fairly high rates of speed, phase-lock to a high-speed digital clock, and convert the line input to a high-precision (14-bit) digital output. Thus, there are really three sections of the AFE1203: the digital section, the phase-locked loop, and the analog section. A combined analog and digital ground plane is recommended. The ground plane should pass under all of the AFE1203 and its pins.

The power supply for the digital section of the AFE1203 can range from 3.3V to 5V. This supply should be decoupled to ground with a ceramic 0.1 μ F capacitor placed as close to DGND (pin 12) and DV_{DD} (pin 13) as possible. Ideally, both a digital power supply plane and a ground plane should run up to and underneath the digital pins of the AFE1203 (pins 3 through 26). However, DV_{DD} may be supplied by a wide printed circuit board (PCB) trace. A ground plane underneath all digital pins is strongly recommended.

The Phase Locked Loop (PLL) analog supply, pin 2, must be derived from AV_{DD}, the general analog supply. The power supply to the PLL must be in the range of 4.75V to 5.25V. The PLL section of the AFE1203 should be decoupled with

both a 10 μ F tantalum capacitor and a 0.1 μ F ceramic capacitor. Both capacitors should be placed between pins 1 and 2. The ceramic capacitor should be placed as close to the AFE1203 as possible. The placement of the tantalum capacitor is not as critical, but should be close. A 5 Ω to 10 Ω resistor should be used to connect the PLL supply (pin 2) to the analog supply. This resistor, in combination with the 10 μ F tantalum capacitor, form a low pass filter to keep glitches that occur on the general analog supply, AV_{DD}, from affecting the PLL supply. The PLL ground (pin 1) should connect directly to the ground plane. The ground plane should also extend underneath PLL_{OUT} and PLL_{IN} (pins 47 and 48, respectively).

The remaining portion of the AFE1203 should be considered analog. All AGND pins should be connected directly to the common ground plane and all AV_{DD} pins should be connected to an analog 5V power plane. Both of these planes should have a low impedance path to the power supply.

Ideally, all ground planes and traces and all power planes and traces should return to the power supply connector before being connected together (if necessary). Each ground and power trace pair should be routed over each other, should not overlap any portion of another pair, and the pairs should be separated by a distance of at least 0.25 inch (6mm).

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 2000, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
AFE1203E/1K	NRND	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		AFE1203E	
AFE1203E/1KG4	NRND	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		AFE1203E	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE1203E/1K	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE1203E/1K	SSOP	DL	48	1000	367.0	367.0	55.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com