

# LVCMOS/LVTTL FANOUT BUFFER/DIVIDER

ICS87004I-03

## GENERAL DESCRIPTION



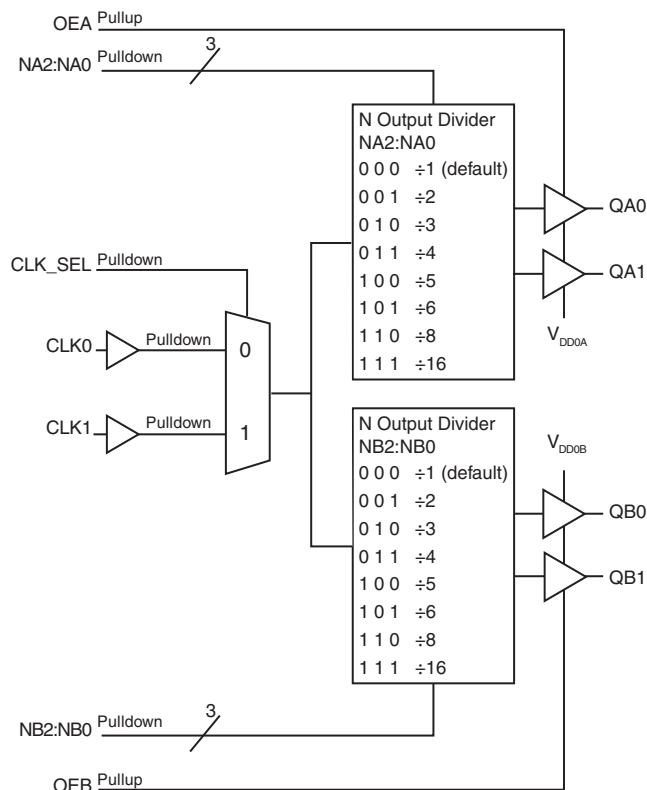
The ICS87004I-03 is a low skew,  $\div 1$ ,  $\div 2$ ,  $\div 3$ ,  $\div 4$ ,  $\div 5$ ,  $\div 6$ ,  $\div 8$ ,  $\div 16$  LVCMOS/LVTTL Fanout Buffer/Divider and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS87004I-03 has selectable clock inputs that accept single ended input levels. Output enable pin controls whether the output is in the active or high impedance state.

The ICS87004I-03 is characterized at 3.3V, 2.5V and mixed 3.3V/2.5V, 3.3V/1.8V, 2.5V/1.8V input/output supply operating modes. Guaranteed bank, output, and part-to-part skew characteristics make the ICS87004I-03 ideal for those applications demanding well defined performance and repeatability.

## FEATURES

- Two banks of two LVCMOS/LVTTL outputs, 15Ω typical output impedance
- Selectable LVCMOS/LVTTL clock inputs
- LVCMOS\_CLK supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Output skew: 40ps (typical)
- Bank skew: 20ps (typical)
- Part-to-part skew: TBD
- Power supply modes:  
Core/Output  
3.3V/3.3V  
3.3V/2.5V  
3.3V/1.8V  
2.5V/2.5V  
2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT

|         |    |    |      |
|---------|----|----|------|
| VDD     | 1  | 20 | OEA  |
| NA2     | 2  | 19 | VDDA |
| NA1     | 3  | 18 | QA0  |
| NA0     | 4  | 17 | QA1  |
| CLK0    | 5  | 16 | GND  |
| CLK_SEL | 6  | 15 | QB1  |
| CLK1    | 7  | 14 | QB0  |
| NB2     | 8  | 13 | VDOB |
| NB1     | 9  | 12 | GND  |
| NB0     | 10 | 11 | OEB  |

**ICS87004I-03**

**20-Lead TSSOP**

6.50mm x 4.40mm x 0.925mm package body

**G Package**

Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

| Number   | Name          | Type   |          | Description                                                                                                                                 |
|----------|---------------|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 1        | $V_{DD}$      | Power  |          | Power supply pin.                                                                                                                           |
| 2, 3, 4  | NA2, NA1, NA0 | Input  | Pulldown | N divider pins for Bank A outputs. LVCMOS / LVTTL interface levels.                                                                         |
| 5, 7     | CLK0, CLK1    | Input  | Pulldown | Single-ended clock inputs. LVCMOS / LVTTL interface levels.                                                                                 |
| 6        | CLK_SEL       | Input  | Pulldown | Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS / LVTTL interface levels.                           |
| 8, 9, 10 | NB2, NB1, NB0 | Input  | Pulldown | N divider pins for Bank B outputs. LVCMOS / LVTTL interface levels.                                                                         |
| 11       | OEB           | Input  | Pullup   | Output enable. When LOW, Bank B outputs are in HIGH impedance state. When HIGH, Bank B outputs are active. LVCMOS / LVTTL interface levels. |
| 12, 16   | GND           | Power  |          | Power supply ground.                                                                                                                        |
| 13       | $V_{DDOB}$    | Power  |          | Output supply pin for Bank B outputs.                                                                                                       |
| 14, 15   | QB0, QB1      | Output |          | Single-ended Bank B clock outputs. LVCMOS / LVTTL interface levels.                                                                         |
| 17, 18   | QA1, QA0      | Output |          | Single-ended Bank A clock outputs. LVCMOS / LVTTL interface levels.                                                                         |
| 19       | $V_{DDOA}$    | Power  |          | Bank A output supply pin.                                                                                                                   |
| 20       | OEA           | Input  | Pullup   | Output enable. When LOW, Bank A outputs are in HIGH impedance state. When HIGH, Bank A outputs are active. LVCMOS / LVTTL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol         | Parameter                                  | Test Conditions | Minimum | Typical | Maximum | Units      |
|----------------|--------------------------------------------|-----------------|---------|---------|---------|------------|
| $C_{IN}$       | Input Capacitance                          |                 |         | 4       |         | pF         |
| $R_{PULLUP}$   | Input Pullup Resistor                      |                 |         | 51      |         | k $\Omega$ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor                    |                 |         | 51      |         | k $\Omega$ |
| $C_{PD}$       | Power Dissipation Capacitance (per output) |                 |         | 10      |         | pF         |
| $R_{OUT}$      | Output Impedance                           |                 |         | 15      |         | $\Omega$   |

TABLE 3. PROGRAMMABLE OUTPUT DIVIDER FUNCTION TABLE

| Inputs |    |    | N Divider Value    | Output Frequency (MHz) |
|--------|----|----|--------------------|------------------------|
| N2     | N1 | N0 |                    |                        |
| 0      | 0  | 0  | $\div 1$ (default) | 250                    |
| 0      | 0  | 1  | $\div 2$           | 125                    |
| 0      | 1  | 0  | $\div 3$           | 83.333                 |
| 0      | 1  | 1  | $\div 4$           | 62.5                   |
| 1      | 0  | 0  | $\div 5$           | 50                     |
| 1      | 0  | 1  | $\div 6$           | 41.667                 |
| 1      | 1  | 0  | $\div 8$           | 31.25                  |
| 1      | 1  | 1  | $\div 16$          | 15.625                 |

NOTE: Some combinations of Bank A and Bank B output divider selections are not synchronous.

**ABSOLUTE MAXIMUM RATINGS**

|                                          |                            |
|------------------------------------------|----------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                       |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$   |
| Outputs, $V_O$                           | -0.5V to $V_{DDOX} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$ | 91.1°C/W (0 mps)           |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C             |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

| Symbol               | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$             | Power Supply Voltage  |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDOA}, V_{DDOB}$ | Output Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{DD}$             | Power Supply Current  |                 |         | 40      |         | mA    |
| $I_{DDOA}, I_{DDOB}$ | Output Supply Current |                 |         | 1       |         | mA    |

**TABLE 4B. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDOA} = V_{DDOB} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

| Symbol               | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$             | Power Supply Voltage  |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDOA}, V_{DDOB}$ | Output Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$             | Power Supply Current  |                 |         | 40      |         | mA    |
| $I_{DDOA}, I_{DDOB}$ | Output Supply Current |                 |         | 1       |         | mA    |

**TABLE 4C. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDOA} = V_{DDOB} = 1.8V \pm 0.15V$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

| Symbol               | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$             | Power Supply Voltage  |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDOA}, V_{DDOB}$ | Output Supply Voltage |                 | 1.65    | 1.8     | 1.95    | V     |
| $I_{DD}$             | Power Supply Current  |                 |         | 40      |         | mA    |
| $I_{DDOA}, I_{DDOB}$ | Output Supply Current |                 |         | 1       |         | mA    |

**TABLE 4D. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDOA} = V_{DDOB} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

| Symbol               | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$             | Power Supply Voltage  |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{DDOA}, V_{DDOB}$ | Output Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$             | Power Supply Current  |                 |         | 39      |         | mA    |
| $I_{DDOA}, I_{DDOB}$ | Output Supply Current |                 |         | 1       |         | mA    |

**TABLE 4E. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDOA} = V_{DDOB} = 1.8V \pm 0.15V$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

| Symbol               | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$             | Power Supply Voltage  |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{DDOA}, V_{DDOB}$ | Output Supply Voltage |                 | 1.65    | 1.8     | 1.95    | V     |
| $I_{DD}$             | Power Supply Current  |                 |         | 39      |         | mA    |
| $I_{DDOA}, I_{DDOB}$ | Output Supply Current |                 |         | 1       |         | mA    |

**TABLE 4F. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$   $V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$ ,  $2.5V \pm 5\%$  OR  $1.8V \pm 0.15V$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

| Symbol    | Parameter                   |                                       | Test Conditions                               | Minimum | Typical | Maximum        | Units         |
|-----------|-----------------------------|---------------------------------------|-----------------------------------------------|---------|---------|----------------|---------------|
| $V_{IH}$  | Input High Voltage          |                                       | $V_{DD} = 3.3V$                               | 2       |         | $V_{DD} + 0.3$ | V             |
|           |                             |                                       | $V_{DD} = 2.5V$                               | 1.7     |         | $V_{DD} + 0.3$ | V             |
| $V_{IL}$  | Input Low Voltage           |                                       | $V_{DD} = 3.3V$                               | -0.3    |         | 0.8            | V             |
|           |                             |                                       | $V_{DD} = 2.5V$                               | -0.3    |         | 0.7            | V             |
| $I_{IH}$  | Input High Current          | CLK0, CLK1, CLK_SEL, NA2:NA0, NB2:NB0 | $V_{DD} = V_{IN} = 3.465V$ or $2.625V$        |         |         | 150            | $\mu\text{A}$ |
|           |                             | OEA, OEB                              | $V_{DD} = V_{IN} = 3.465V$ or $2.625V$        |         |         | 5              | $\mu\text{A}$ |
| $I_{IL}$  | Input Low Current           | CLK0, CLK1, CLK_SEL, NA2:NA0, NB2:NB0 | $V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$ | -5      |         |                | $\mu\text{A}$ |
|           |                             | OEA, OEB                              | $V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$ | -150    |         |                | $\mu\text{A}$ |
| $V_{OH}$  | Output High Voltage; NOTE 1 |                                       | $V_{DDOX} = 3.3V \pm 5\%$                     | 2.6     |         |                | V             |
|           |                             |                                       | $V_{DDOX} = 2.5V \pm 5\%$                     | 1.8     |         |                | V             |
|           |                             |                                       | $V_{DDOX} = 1.8V \pm 0.15V$                   | 1.5     |         |                | V             |
| $V_{OL}$  | Output Low Voltage; NOTE 1  |                                       | $V_{DDOX} = 3.3V \pm 5\%$                     |         |         | 0.5            | V             |
|           |                             |                                       | $V_{DDOX} = 2.5V \pm 5\%$                     |         |         | 0.5            | V             |
|           |                             |                                       | $V_{DDOX} = 1.8V \pm 0.15V$                   |         |         | 0.4            | V             |
| $I_{OZL}$ | Output Hi-Z Current Low     |                                       |                                               | -5      |         |                | $\mu\text{A}$ |
| $I_{OZH}$ | Output Hi-Z Current High    |                                       |                                               |         |         | 5              | $\mu\text{A}$ |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDOX}/2$ . See Parameter Measurement Information, Output Load Test Circuit.

**TABLE 5A. AC CHARACTERISTICS,  $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

| Symbol      | Parameter                     | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-------------------------------|-----------------|---------|---------|---------|-------|
| $f_{MAX}$   | Output Frequency              |                 |         |         | 250     | MHz   |
| $t_{PD}$    | Propagation Delay, NOTE 1     |                 |         | 4.3     |         | ns    |
| $tsk(o)$    | Output Skew; NOTE 2, 3        |                 |         | 40      |         | ps    |
| $tsk(pp)$   | Part-to-Part Skew; NOTE 3, 4  |                 |         |         |         | ps    |
| $tsk(b)$    | Bank Skew; NOTE 3, 5          |                 |         | 20      |         | ps    |
| $t_R / t_F$ | Output Rise/Fall Time; NOTE 6 | 20% to 80%      |         | 700     |         | ps    |
| odc         | Output Duty Cycle             |                 |         | 50      |         | %     |
| $t_{EN}$    | Output Enable Time; NOTE 6    |                 |         |         | 5       | ns    |
| $t_{DIS}$   | Output Disable Time; NOTE 6   |                 |         |         | 5       | ns    |

All parameters measured at  $f \leq \text{TBD MHz}$  unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDOX}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at  $V_{DDOX}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDOX}/2$ .

NOTE 5: Defined as skew within a bank with equal load conditions.

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

**TABLE 5B. AC CHARACTERISTICS**,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDOA} = V_{DDOB} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$ 

| Symbol      | Parameter                     | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-------------------------------|-----------------|---------|---------|---------|-------|
| $f_{MAX}$   | Output Frequency              |                 |         |         | 250     | MHz   |
| $t_{PD}$    | Propagation Delay, NOTE 1     |                 |         | 4.6     |         | ns    |
| $tsk(o)$    | Output Skew; NOTE 2, 3        |                 |         | 40      |         | ps    |
| $tsk(pp)$   | Part-to-Part Skew; NOTE 3, 4  |                 |         |         |         | ps    |
| $tsk(b)$    | Bank Skew; NOTE 3, 5          |                 |         | 20      |         | ps    |
| $t_R / t_F$ | Output Rise/Fall Time; NOTE 6 | 20% to 80%      |         | 800     |         | ps    |
| odc         | Output Duty Cycle             |                 |         | 50      |         | %     |
| $t_{EN}$    | Output Enable Time; NOTE 6    |                 |         |         | 5       | ns    |
| $t_{DIS}$   | Output Disable Time; NOTE 6   |                 |         |         | 5       | ns    |

All parameters measured at  $f \leq$  TBDMHz unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDOX}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at  $V_{DDOX}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDOX}/2$ .

NOTE 5: Defined as skew within a bank with equal load conditions.

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

**TABLE 5C. AC CHARACTERISTICS**,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDOA} = V_{DDOB} = 1.8V \pm 0.15V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$ 

| Symbol      | Parameter                     | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-------------------------------|-----------------|---------|---------|---------|-------|
| $f_{MAX}$   | Output Frequency              |                 |         |         | 250     | MHz   |
| $t_{PD}$    | Propagation Delay, NOTE 1     |                 |         | 5.0     |         | ns    |
| $tsk(o)$    | Output Skew; NOTE 2, 3        |                 |         | 40      |         | ps    |
| $tsk(pp)$   | Part-to-Part Skew; NOTE 3, 4  |                 |         |         |         | ps    |
| $tsk(b)$    | Bank Skew; NOTE 3, 5          |                 |         | 20      |         | ps    |
| $t_R / t_F$ | Output Rise/Fall Time; NOTE 6 | 20% to 80%      |         | 1       |         | ns    |
| odc         | Output Duty Cycle             |                 |         | 50      |         | %     |
| $t_{EN}$    | Output Enable Time; NOTE 6    |                 |         |         | 5       | ns    |
| $t_{DIS}$   | Output Disable Time; NOTE 6   |                 |         |         | 5       | ns    |

All parameters measured at  $f \leq$  TBDMHz unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDOX}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at  $V_{DDOX}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDOX}/2$ .

NOTE 5: Defined as skew within a bank with equal load conditions.

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

**TABLE 5D. AC CHARACTERISTICS,  $V_{DD} = V_{DDOA} = V_{DDOB} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

| Symbol      | Parameter                     | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-------------------------------|-----------------|---------|---------|---------|-------|
| $f_{MAX}$   | Output Frequency              |                 |         |         | 250     | MHz   |
| $t_{PD}$    | Propagation Delay, NOTE 1     |                 |         | 4.7     |         | ns    |
| $tsk(o)$    | Output Skew; NOTE 2, 3        |                 |         | 40      |         | ps    |
| $tsk(pp)$   | Part-to-Part Skew; NOTE 3, 4  |                 |         |         |         | ps    |
| $tsk(b)$    | Bank Skew; NOTE 3, 5          |                 |         | 20      |         | ps    |
| $t_R / t_F$ | Output Rise/Fall Time; NOTE 6 | 20% to 80%      |         | 900     |         | ps    |
| odc         | Output Duty Cycle             |                 |         | 50      |         | %     |
| $t_{EN}$    | Output Enable Time; NOTE 6    |                 |         |         | 5       | ns    |
| $t_{DIS}$   | Output Disable Time; NOTE 6   |                 |         |         | 5       | ns    |

All parameters measured at  $f \leq \text{TBD MHz}$  unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDOX}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at  $V_{DDOX}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDOX}/2$ .

NOTE 5: Defined as skew within a bank with equal load conditions.

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

**TABLE 5E. AC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDOA} = V_{DDOB} = 1.8V \pm 0.15V$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

| Symbol      | Parameter                     | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-------------------------------|-----------------|---------|---------|---------|-------|
| $f_{MAX}$   | Output Frequency              |                 |         |         | 250     | MHz   |
| $t_{PD}$    | Propagation Delay, NOTE 1     |                 |         | 5.0     |         | ns    |
| $tsk(o)$    | Output Skew; NOTE 2, 3        |                 |         | 40      |         | ps    |
| $tsk(pp)$   | Part-to-Part Skew; NOTE 3, 4  |                 |         |         |         | ps    |
| $tsk(b)$    | Bank Skew; NOTE 3, 5          |                 |         | 20      |         | ps    |
| $t_R / t_F$ | Output Rise/Fall Time; NOTE 6 | 20% to 80%      |         | 1.1     |         | ns    |
| odc         | Output Duty Cycle             |                 |         | 50      |         | %     |
| $t_{EN}$    | Output Enable Time; NOTE 6    |                 |         |         | 5       | ns    |
| $t_{DIS}$   | Output Disable Time; NOTE 6   |                 |         |         | 5       | ns    |

All parameters measured at  $f \leq \text{TBD MHz}$  unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDOX}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at  $V_{DDOX}/2$ .

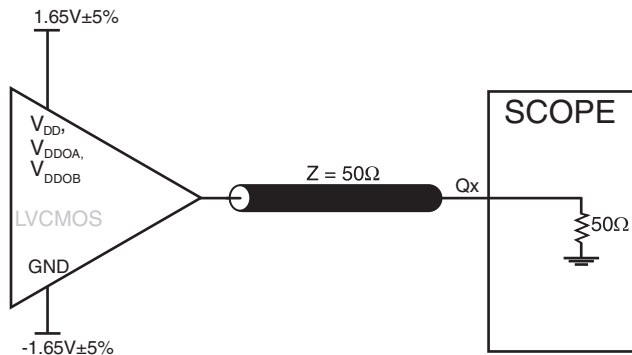
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDOX}/2$ .

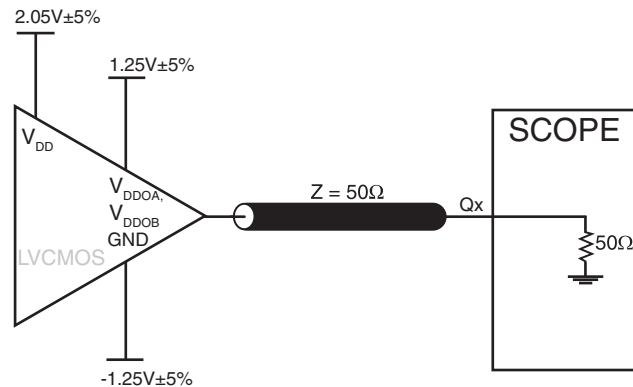
NOTE 5: Defined as skew within a bank with equal load conditions.

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

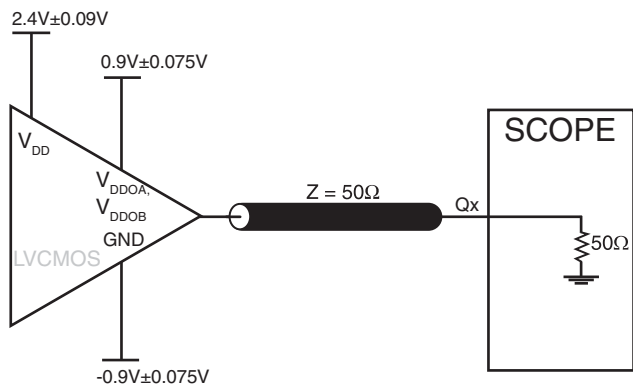
## PARAMETER MEASUREMENT INFORMATION



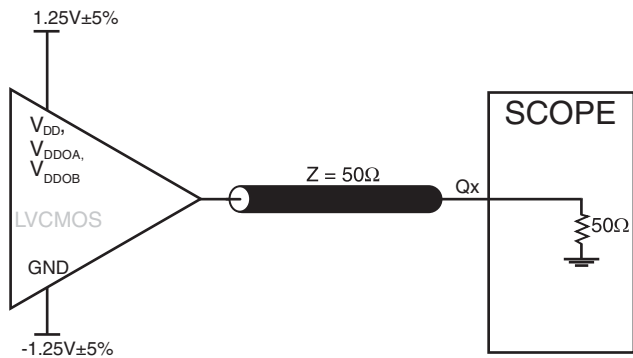
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



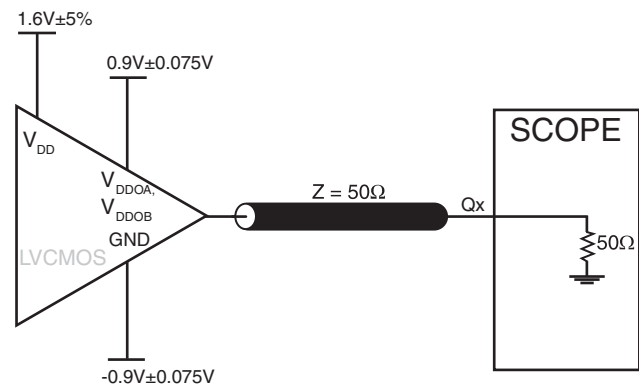
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



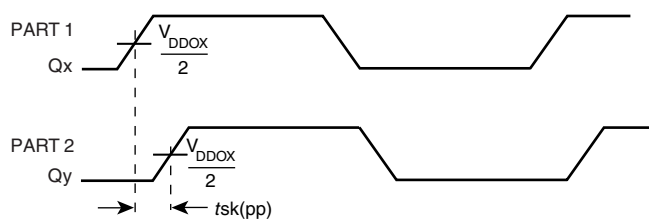
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT

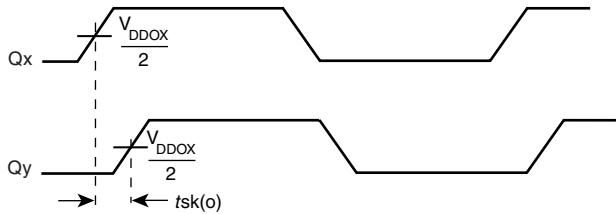


2.5V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT

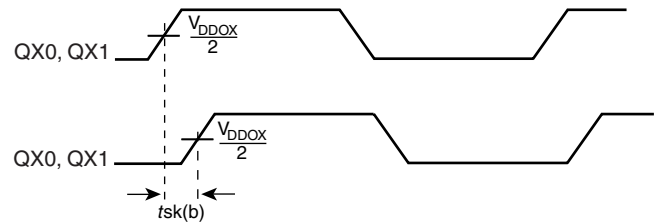


PART-TO-PART SKEW

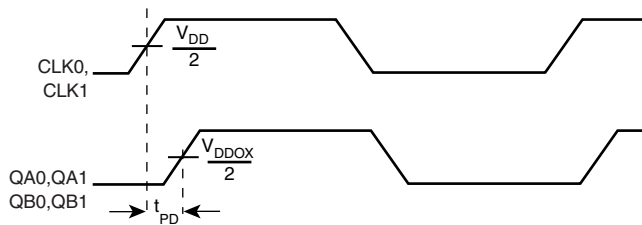
## PARAMETER MEASUREMENT INFORMATION, CONTINUED



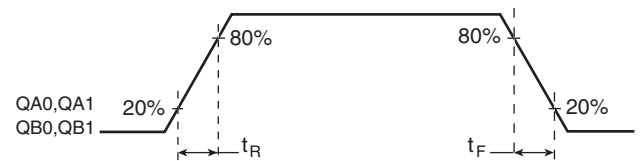
OUTPUT SKEW



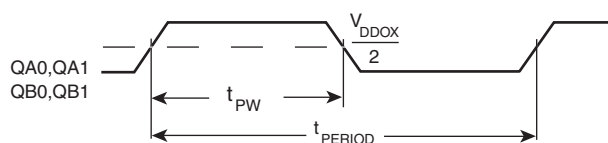
BANK SKEW (where X denotes outputs in the same bank)



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

## APPLICATION INFORMATION

### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### CLK INPUTS

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the CLK input to ground.

##### LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### OUTPUTS:

##### LVCMOS OUTPUTS

All unused LVCMOS output can be left floating. There should be no trace attached.

## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

| $\theta_{JA}$ by Velocity (Meters per Second) |          |          |          |
|-----------------------------------------------|----------|----------|----------|
|                                               | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards   | 91.1°C/W | 86.7°C/W | 84.6°C/W |

### TRANSISTOR COUNT

The transistor count for ICS87004I-03 is: 2781

## PACKAGE OUTLINE AND DIMENSIONS

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

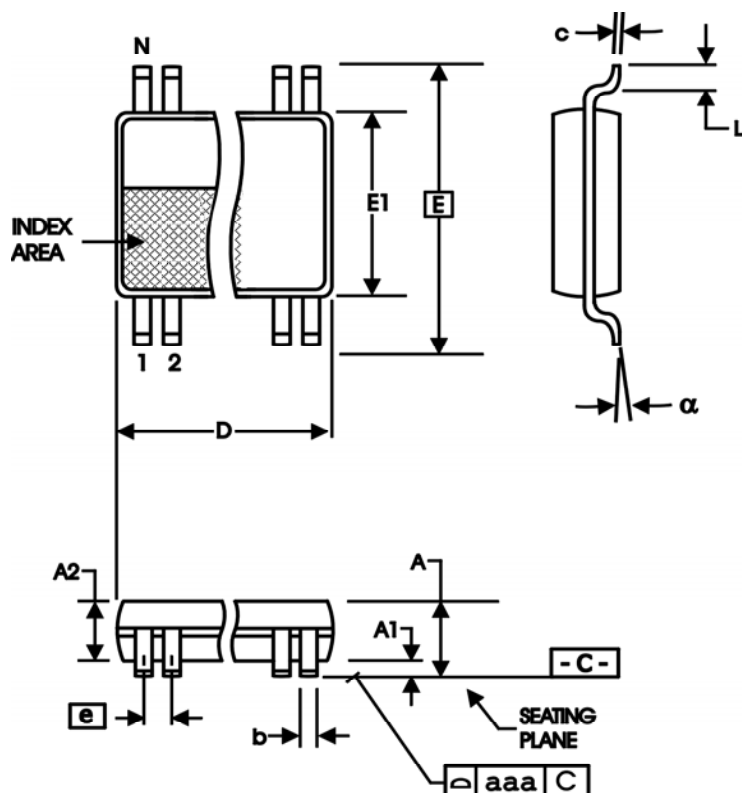


TABLE 7. PACKAGE DIMENSIONS

| SYMBOL   | Millimeters |      |
|----------|-------------|------|
|          | MIN         | MAX  |
| N        | 20          |      |
| A        | --          | 1.20 |
| A1       | 0.05        | 0.15 |
| A2       | 0.80        | 1.05 |
| b        | 0.19        | 0.30 |
| c        | 0.09        | 0.20 |
| D        | 6.40        | 6.60 |
| E        | 6.40 BASIC  |      |
| E1       | 4.30        | 4.50 |
| e        | 0.65 BASIC  |      |
| L        | 0.45        | 0.75 |
| $\alpha$ | 0°          | 8°   |
| aaa      | --          | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

| Part/Order Number | Marking      | Package                   | Shipping Packaging | Temperature   |
|-------------------|--------------|---------------------------|--------------------|---------------|
| 87004BGI-03       | ICS87004BI03 | 20 Lead TSSOP             | tube               | -40°C to 85°C |
| 87004BGI-03T      | ICS87004BI03 | 20 Lead TSSOP             | 2500 tape & reel   | -40°C to 85°C |
| 87004BGI-03LF     | TBD          | 20 Lead "Lead-Free" TSSOP | tube               | -40°C to 85°C |
| 87004BGI-03LFT    | TBD          | 20 Lead "Lead-Free" TSSOP | 2500 tape & reel   | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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