Philips Components

Data sheet	
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SAA7197

Clock signal generation circuit (SCGC) for Desktop Video systems

FEATURES

- PLL frequency multiplier
- Two different clock frequencies
- Power fail detection circuit

APPLICATIONS

- Desktop video systems

GENERAL DESCRIPTION

The SAA7197 is a clock generation circuit (SCGC) which generates all clock signals required for a desktop video system utilizing the SAA719X family of devices. The circuit operates in either the phase-locked-loop mode (PLL) or voltage controlled oscillator mode (VCO).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage	4.5	-	5.5	V
I_{DD}	digital supply current	10	-	60	mA
I_{DDA}	analog supply current	5	-	*	mA
$P_{tot(c)}$	total power consumption	-	-	0.4	W
T_{amb}	operating ambient temperature range	0	-	70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7197P	20	DIL	plastic	SOT146
SAA7197T	20	SO20	plastic	SOT163A

* Value to be fixed.

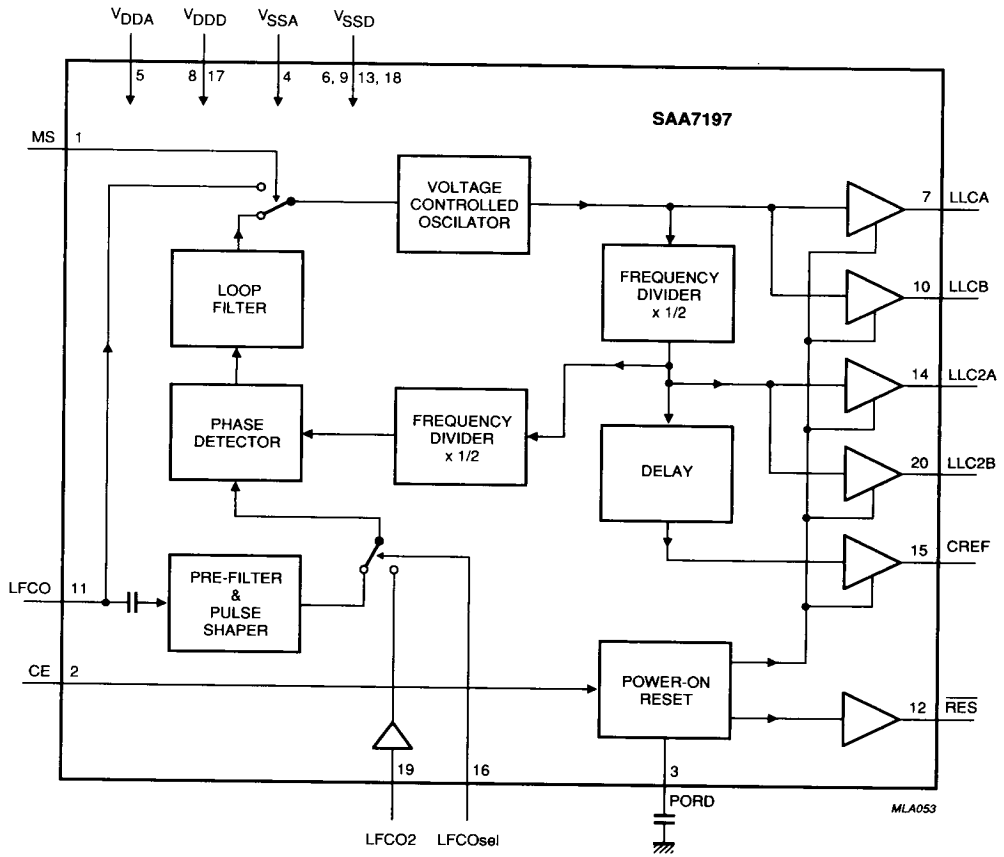

Fig.1 Block diagram.

Clock signal generation circuit (SCGC) for Desktop Video systems

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PIN CONFIGURATION

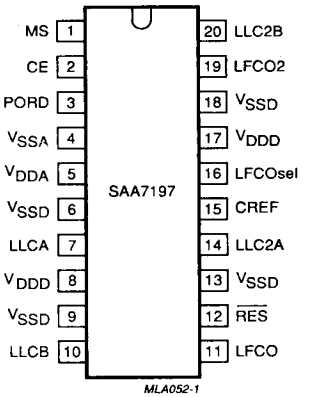

Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	Mode Select input. Usually this input is LOW and the SCGC generates the different clocks using the LFCO or LFCO2 as reference frequency
CE	2	Chip Enable input. A HIGH level at CE enables the output buffers; a LOW level sets the clock buffers to HIGH and $\overline{RES}$ to LOW. The VCO operates on an internally adjusted frequency
PORD	3	Power-On Reset Delay. An external capacitor at this pin determines the duration of the reset state (see $\overline{RES}$)
V_{SSA}	4	Analog ground
V_{DDA}	5	Analog power supply
V_{SSD}	6	Digital ground
LLCA	7	LLCA is a line-locked clock output signal of 4 times the LFCO or LFCO2 input frequency. The waveform is rectangular
V_{DDD}	8	Digital power supply
V_{SSD}	9	Digital ground
LLCB	10	LLCB is a line-locked clock output signal of 4 times the LFCO or LFCO2 input frequency. The waveform is rectangular
LFCO	11	Line Frequency COntrol input. This signal received from the DMSD-SQP, is a multiple of the line frequency. It is the reference frequency for all clocks generated by the SCGC
$\overline{RES}$	12	RESET output (active LOW). This output indicates the reset state. After a power-ON or power failure $\overline{RES}$ goes LOW and remains in this state for a period that is determined by the external capacitor connected to pin PORD. If the supply voltage decreases below the operating range (power failure)*, $\overline{RES}$ goes LOW. After the power supply returns within the operating range and the POR delay is completed, $\overline{RES}$ goes HIGH. This signal can be used to reset the entire digital TV system. When CE is LOW, the $\overline{RES}$ output will be set LOW
V_{SSD}	13	Digital ground
LLC2A	14	LLC2A is a line-locked clock output signal of 2 times the LFCO or LFCO2 input frequency. The waveform is rectangular
CREF	15	CLocK reference signal for Desktop Video system. This output is a clock qualifier signal of 2 times the LFCO or LFCO2 input frequency for bus clock generation
LFCOsel	16	Line Frequency COntrol select. This input signal selects either the LFCO signal from the DMSD (LFCOsel = LOW) or a TTL-compatible LFCO2 signal (LFCOsel = HIGH)
V_{DDD}	17	Digital power supply
V_{SSD}	18	Digital ground
LFCO2	19	Line Frequency COntrol 2 input. This signal received from an external line reference source, is a multiple of the line frequency. It is the TTL-compatible reference frequency for all clocks generated by the SCGC
LLC2B	20	LLC2B is a line-locked clock output signal of 2 times the LFCO or LFCO2 input frequency. The waveform is rectangular

* See section "**APPLICATION INFORMATION**"; Fig.4, reset waveform.

Clock signal generation circuit (SCGC) for Desktop Video systems

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FUNCTIONAL DESCRIPTION

The SAA7197 generates all clock signals required for a desktop video system utilizing the SAA719X family of devices. These consist of the ADC8 (8-bit Analog-to-Digital Converter), DMSD-SQP (Digital Multi-Standard Decoder - for Square Pixel applications), and DCSC (Digital Colour Space Converter) and optional extensions. In conjunction with memory controllers this completes a system for desktop video applications.

The main function of the SCGC is a PLL which multiplys an incoming reference signal (LFCO or LFCO2) by the factors 2 and 4. The LFCO signal is a digital-to-analog converted signal provided by the DMSD-SQP's horizontal PLL. It is a multiple of the line frequency of 360 x f_H (6.14 MHz) with 60 Hz standards or 472 x f_H (7.38 MHz) with 50 Hz standards. Alternatively, the LFCO2 input can be used for TTL compatible signals from an external reference source.

The output signals from the PLL are LLCA and LLCB (4 x f_{LFCO}) and LLC2A and LLC2B (2 x f_{LFCO}). The waveforms are rectangular with a duty factor of 50%. The CREF output at 2 x f_{LFCO} is for controlling the internal clock dividers of the DMSD2-SQP chip family. The clock outputs of equal frequencies may be connected together externally.

The $\overline{RES}$ output signal indicates a stable power supply. This output can be used to drive other power-on reset circuits. An external capacitor, connected to pin 3 (PORD), determines the reset time. The clock signal output lines go HIGH during an internal power-on reset period.

The internal reset cycle is shorter than the external reset cycle. This is to ensure that the clock signals are delivered before $\overline{RES}$ goes HIGH. If the clock signals must be within a specified range before $\overline{RES}$ goes HIGH, it is important to apply the LFCO signal before the LOW-to-HIGH transition.

The power-on reset circuit is combined with a power failure detector.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}/V_{DDA}	supply voltage		−0.5	7.0	V
V_I	input voltage		−0.5	7.0	V
V_O	output voltage	I_{OM} = 20 mA	−0.5	7.0	V
P_{tot}	total power dissipation		-	1.1	W
T_{stg}	storage temperature range		-55	+150	°C
T_{amb}	operating ambient temperature range		0	+70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; $f_{LFCO} = 5.5$ to 8.0 MHz; $T_{amb} = 0$ to +70 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DDD}	digital supply voltage		4.5	5.5	V
I_{DDD}	digital supply current		10	60	mA
V_{DDA}	analog supply voltage		4.5	5.5	V
I_{DDA}	analog supply current		3	*	mA
Inputs MS, CE, LFCO and LFC02					
I_{IL}	input leakage current		-	10	µA
MS, CE, LFCOsel and LFCO2					
C_I	input capacitance		-	5	pF
LFCO					
C_I	input capacitance		-	10	pF
CE, LFCOsel and LFCO2					
V_{IL}	input voltage LOW		0	0.8	V
V_{IH}	input voltage HIGH		2.0	V_{DDD}	V
LFCO2					
f_{LFCO2}	input frequency		5.5	8.0	MHz
LFCO					
V_{LFCO}	input voltage		0	V_{DDA}	V
f_{LFCO}	input frequency		5.5	8.0	MHz
$V_{LFCO(p-p)}$	input signal amplitude (peak-to-peak value)		1.0	V_{DDA}	V
Outputs LLCA, LLCB, LLC2A, LLC2B and CREF					
V_{OH}	output voltage HIGH	CE = LOW; $I_{OH} = -0.5$ mA	2.6	V_{DDD}	V
RES					
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	V_{DDD}	V
V_{OL}	output voltage LOW	$I_{OL} = 2.0$ mA	0	0.4	V
t_d	delay time (see Fig.4)	$C_{PORD} = 100$ nF	20	200	ms
CREF					
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	V_{DDD}	V
V_{OL}	output voltage LOW	$I_{OL} = 2.0$ mA	0	0.6	V
C_L	output load capacitance		15	40	pF
t_{HD}	output hold time	note 1	4	-	ns
t_{SU}	output set-up time		12	-	ns

* Value to be fixed.

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Outputs (continued) LLCA, LLCB, LLC2A and LLC2B					
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.6	V_{DDD}	V
V_{OL}	output voltage LOW	$I_{OL} = 2.0$ mA	0	0.6	V
	output frequency				
f_{LLCA}	LLCA		-	$4f_{LFCO}$ or $4f_{LFCO2}$	MHz
f_{LLCB}	LLCB		-	$4f_{LFCO}$ or $4f_{LFCO2}$	MHz
f_{LLC2A}	LLC2A		-	$2f_{LFCO}$ or $2f_{LFCO2}$	MHz
f_{LLC2B}	LLC2B		-	$2f_{LFCO}$ or $2f_{LFCO2}$	MHz
t_r	rise time	0.6 V to 2.6 V	-	5	ns
t_f	fall time	2.6 V to 0.6 V	-	5	ns
t_{comp}	composite rise time	note 2	-	8	ns
LLCA, LLCB, LLC2A and LLC2B					
	duty factor	notes 1 and 3			
K_{CLK1}	LLCA and LLCB		0.43	0.57	
K_{CLK3}	LLC2A and LLC2B		0.43	0.57	

Notes to the characteristics

1. $f_{LFCO} = 8$ MHz, with a 40 pF output load (typically 6.75 MHz); see Fig.3.

2. The composite rise time is the time duration from all clocks = LOW to all clocks = HIGH (within 0.6 V to 2.6 V, includes rise time, skew and jitter). Skew between two LLX - clocks will not deviate more than ± 2 ns if the output loads are matched within 20%.

3. The duty factor is mean value and defined at 1.5 V.

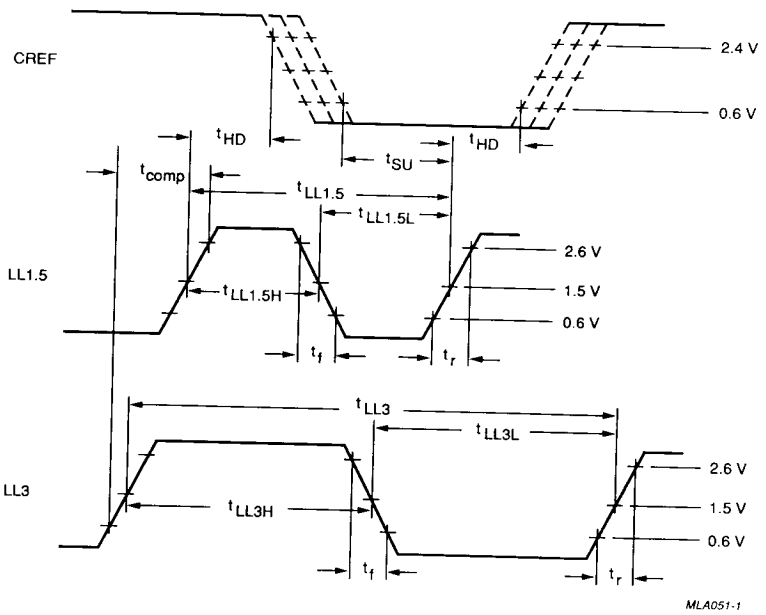

Fig.3 Timing waveform.

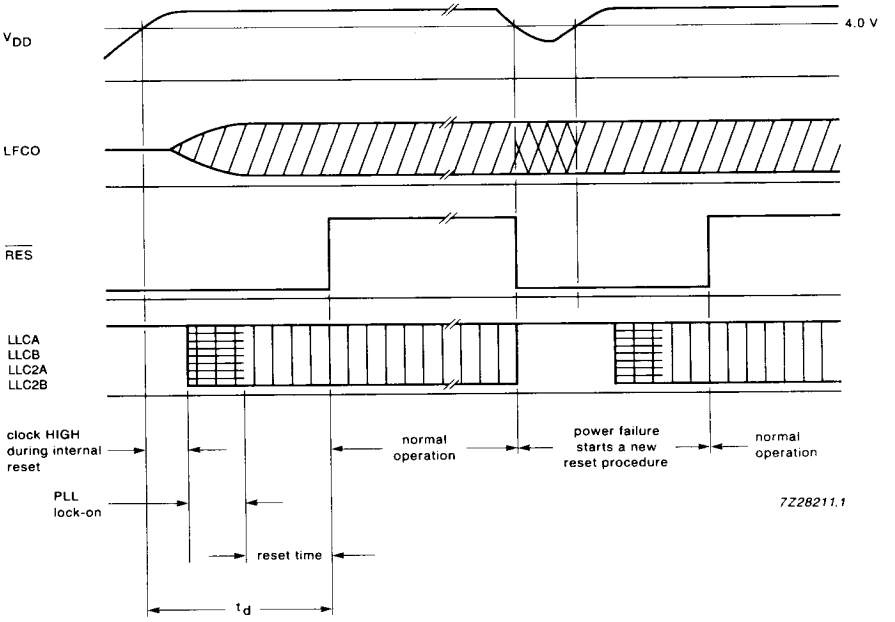

Fig.4 Reset waveform.