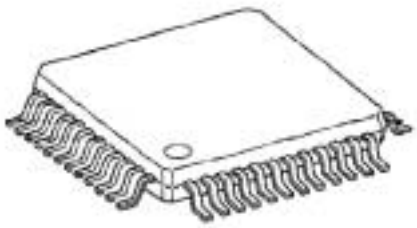
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA1375FG

Single Conversion Tuner for Digital TV / CATV

The TA1375FG is a single chip which integrates a PLL and Mixer, Oscillator, IF amplifier and IF GCA for Digital TV and CATV.
This oscillator and PLL circuits are low phase noise.
The control data conforms to I²C-bus formats.
Flat, compact small package : LQFP48(0.5mm pitch)



LQFP48-P-0707-0.5

Weight: 0.17g (typ.)

Features

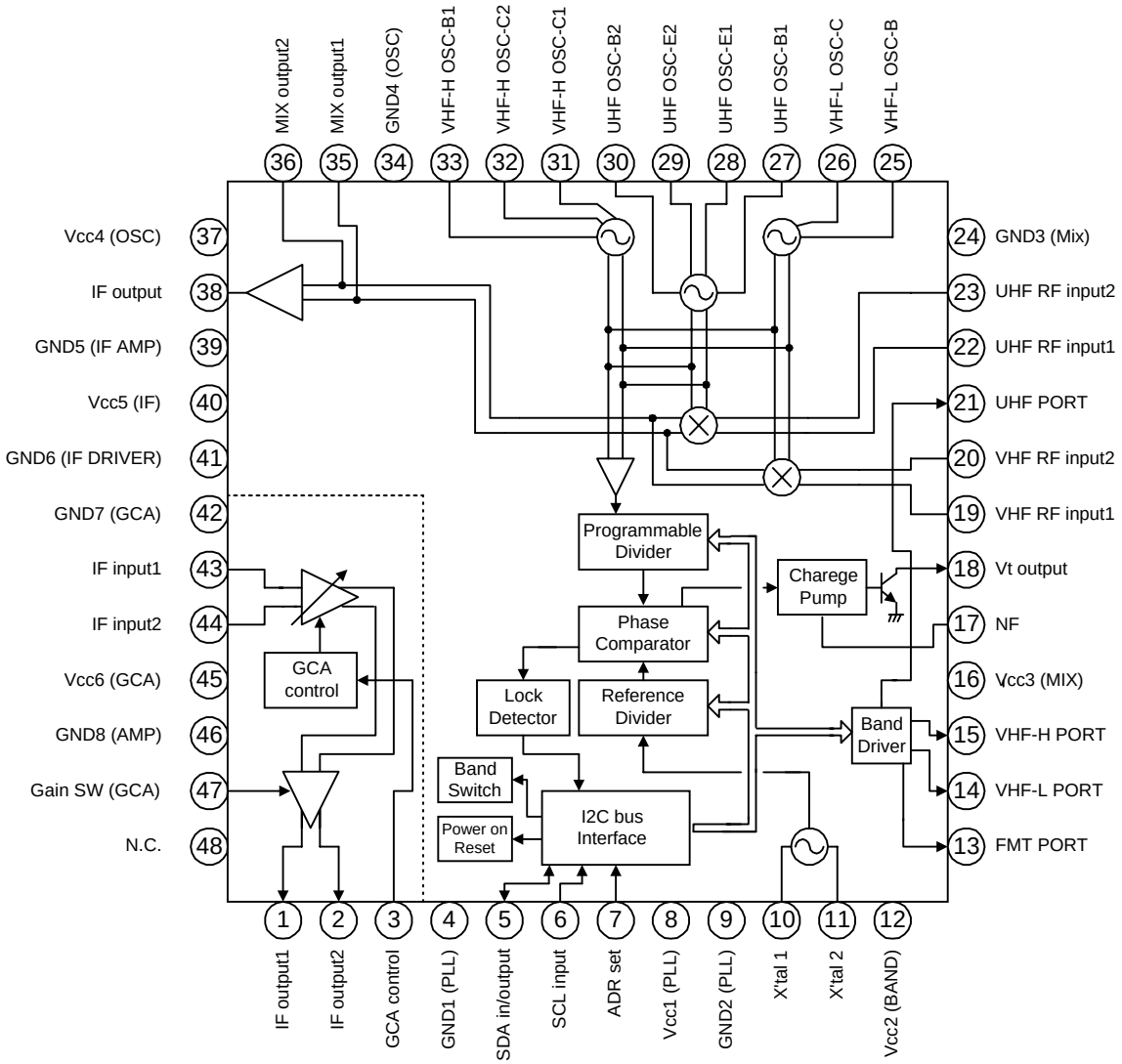
- Vcc: 5V（typ.）
- 2 band mixer
- 3 band oscillator
- Low phase noise oscillator circuit
- Built-In IF GCA circuit
- IF output driver
- GCA block: Gain changeover switch (3dB shift possible)
- Direct 2 modulus type frequency synthesizer
- I²C bus format control
- 33V high voltage tuning amplifier built-in
- 4-bit bandswitch drive transistor
- Frequency step : 50kHz, 62.5kHz, 142.86kHz, 166.67kHz (at 4MHz X'tal used)
- 4 programmable chip address
- Power on reset circuit

Power on reset status

- Frequency step : [62.5kHz]
- Charge pump current: [Low]
- Counter data: ALL [0]
- Band driver: [OFF]
- Tuning amplifier: [OFF]
- Local oscillator and mixer: ALL [OFF]

(note1)These devices are easy to be damaged by high voltage or electric fields. In regards to this, please handle with care.

Block Diagram



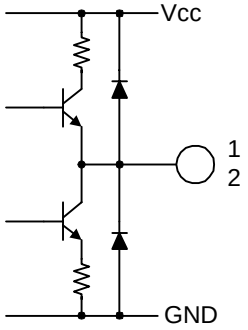
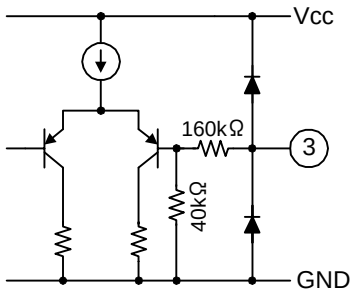
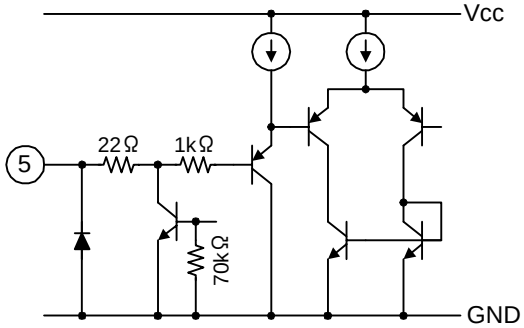
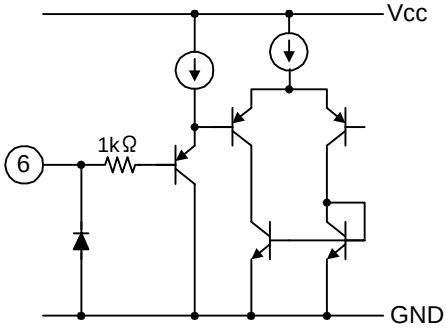
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purpose.

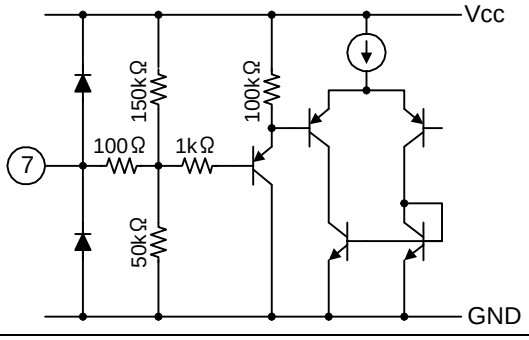
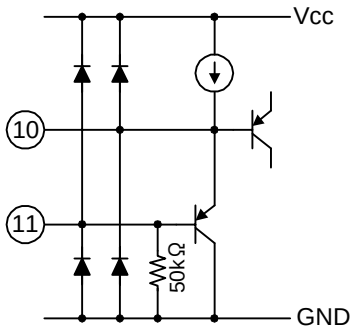
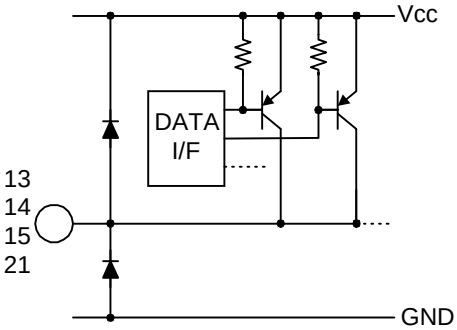
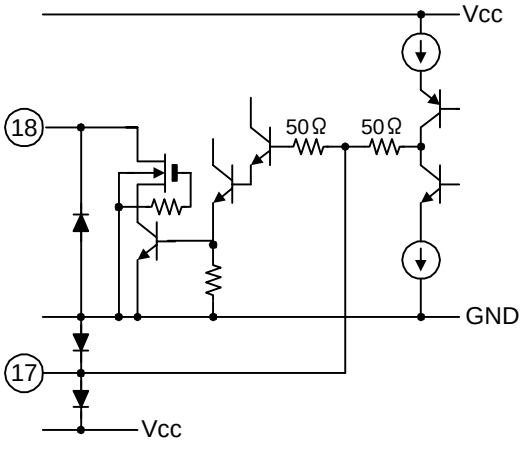
Terminal Name

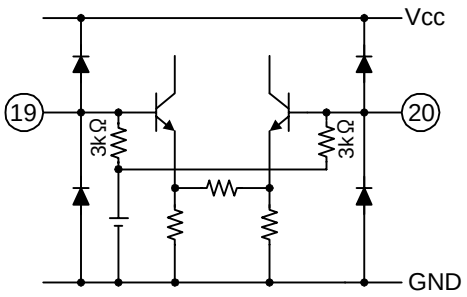
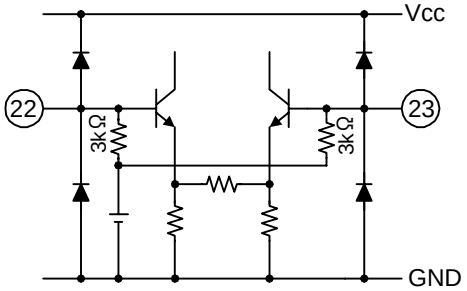
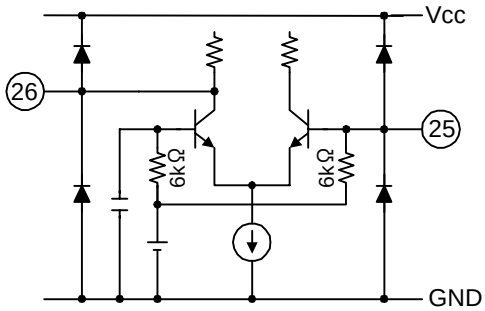
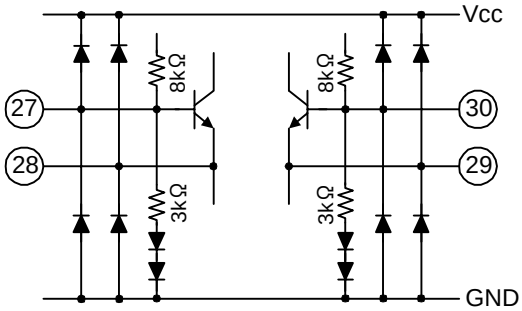
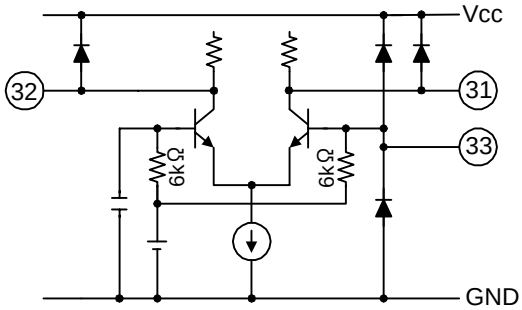
Pin No.	Pin name
1	IF output 1
2	IF output 2
3	GCA control terminal
4	GND 1 (PLL)
5	SDA In/out
6	SCL In
7	ADR set
8	Vcc 1 (PLL)
9	GND 2 (PLL)
10	X'tal
11	X'tal
12	Vcc 2 (BAND)
13	FMT port (NPN-Tr)
14	VHF-L port (NPN-Tr)
15	VHF-H port (NPN-Tr)
16	Vcc 3 (MIX)
17	NF
18	Vt output
19	VHF RF Input 1
20	VHF RF Input 2
21	UHF port (NPN-Tr)
22	UHF RF Input 1
23	UHF RF Input 2
24	GND 3 (MIX)
25	VHF-L OSC-base
26	VHF-L OSC-collector
27	UHF OSC-base1
28	UHF OSC-emitter1
29	UHF OSC-emitter2
30	UHF OSC-base2
31	VHF-H OSC-collector1
32	VHF-H OSC-collector2
33	VHF-H OSC-base1
34	GND 4 (OSC)
35	MIX output 1
36	MIX output 2
37	Vcc 4 (OSC)
38	IF out
39	GND 5 (IF AMP)
40	Vcc 5 (IF)
41	GND 6 (IF DRIVER)
42	GND 7 (GCA)
43	IF Input 1
44	IF Input 2
45	Vcc 6 (GCA)
46	GND 8 (AMP)
47	Gain SW（GCA） （Open: typ / GND:＋3dB gain up）
48	N.C. （This pin does not connect the Inside circuit.）

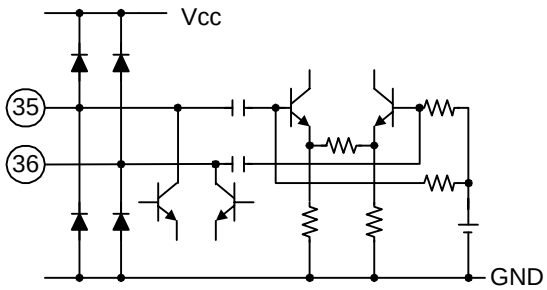
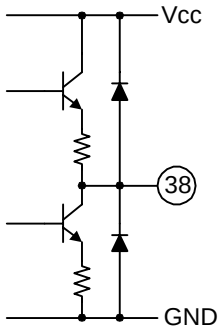
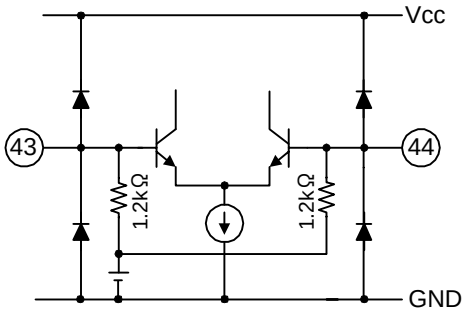
Terminal Function

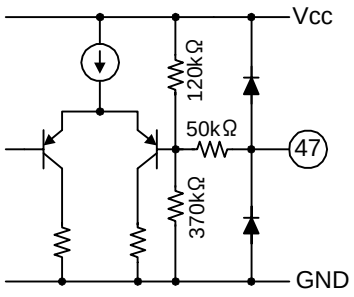
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purpose.

Pin No.	Pin Name.	Function	Interface
1 2	IF output	Symmetrical output of IF signal	
3	GCA control	Gain control pin of GCA block. The gain of GCA block Is controllable by the voltage given to this pin.	
4	GND1	This Is the ground pin for PLL circuit.	–
5	SDA	Serial data Input and output pin	
6	SCL	Serial clock Input pin	

Pin No.	Pin Name.	Function	Interface
7	ADR set	Address setting pin The address of PLL block Is set up with the voltage given to this pin.	
8	Vcc1	This Is power supply for PLL circuit.	–
9	GND2	This Is the ground pin for PLL circuit.	–
10 11	X'tal	Usually, Crystal unit of 4MHz Is connected to this pin.	
12	Vcc2	This Is power supply for Band circuit.	–
13 14 15 21	Band driver Output port	The output port of Band block can be set up with the control data. Keep In my mind each band drive port that drive current differs.	
16	Vcc3	This Is power supply for Mixer circuit.	–
17	NF	Please to sure connect a resistance (about 33kΩ) with a pin18 between the 33V external power supplies for tuning.	
18	Vt output	Please connect with a pin18 between GND the capacity element which does not affect a PLL loop for unusual oscillation prevention.	

Pin No.	Pin Name.	Function	Interface
19 20	VHF RF input	RF singanl Input pin for VHF band. It can be symmetrical Input, asymmetrical Input by grounding of one pins with a capacity element.	
22 23	UHF RF input	RF singanl Input pin for UHF band. It can be symmetrical Input, asymmetrical Input by grounding of one pins with a capacity element.	
24	GND3	This Is the ground pin for Mixer circuit.	–
25 26	VHF-L band Local oscillator	Local oscillator for VHF-L band The oscillator type Is symmetrical amplifier.	
27 28 29 30	UHF band Local oscillator	Local oscillator for UHF band The oscillator type Is balanced clap.	
31 32 33	VHF-H band Local oscillator	Local oscillator for VHF-H band The oscillator type Is symmetrical amplifier.	

Pin No.	Pin Name.	Function	Interface
34	GND4	This Is the ground pin for Local oscillator circuit.	–
35 36	Mixer ouytput	Mixer output pins A tank circuit Is connected between pins for tuning. Since these open collector output, please connect with a power supply through load(resistance, coil).	
37	Vcc4	This Is power supply for Local oscillator circuit.	–
38	IF output (MOP)	IF output pin for MOP block	
39	GND5	This Is the ground pin for IF amplifier circuit.	–
40	Vcc5	This Is power supply for IF circuit.	–
41	GND6	This Is the ground pin for IF output circuit.	–
42	GND7	This Is the ground pin for GCA circuit.	–
43 44	IF Input	Symmetrical Input of GCA block	

Pin No.	Pin Name.	Function	Interface
45	Vcc6	This Is power supply for GCA circuit.	–
46	GND8	This Is the ground pin for GCA output circuit.	–
47	Gain SW (GCA)	It Is the voltage gain changeover SW. It changes by setting this pin to Open or GND. When based on an open state, about 3dB voltage gain can be increased by setting a pin to GND.	
48	N.C.	This pin does not connect the Inside circuit.	–

Maximum Ratings

CHARACTERISTIC	PIN No	SYMBOL	RATING	UNIT
Vcc	8	Vcc1	6	V
	12	Vcc2	6	
	16	Vcc3	6	
	37	Vcc4	6	
	40	Vcc5	6	
	45	Vcc6	6	
GCA control pin	3	GCA cont.	6	V
RF signal Input level for Mixer	19,20,22,23	fin	120	dBuV
Tuning amplifier apply voltage	18	VBT	38	V
Power Dissipation	-	PD	1190 (note3)	mW
Operating Temparature	-	Topr	-20～85	℃
Storage Temparature	-	Tstg	-55～150	℃

(note2) The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.
If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed.
Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment.
Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions.
Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents.

(note3) 50 × 50 × 1.6mm, Cu36% board used.
When using the device at above Ta=25℃, decrease the power dissipation by 9.6mW for each Increase of 1℃

Operating Supply Voltage

Pin No.	SYMBOL	MIN.	TYP.	MAX.	UNIT
8	Vcc1 (PLL)	4.5	5.0	5.25	V
12	Vcc2 (BAND)	4.5	5.0	5.25	
16	Vcc3 (MIX)	4.5	5.0	5.25	
37	Vcc4 (OSC)	4.5	5.0	5.25	
40	Vcc5 (IF)	4.5	5.0	5.25	
45	Vcc6 (GCA)	4.5	5.0	5.25	

Electric Characteristics

DC Characteristics

(Unless otherwise specified,Vcc1 = Vcc2 = Vcc3 = Vcc4 = Vcc5 = Vcc6 = 5V, Ta = 25℃)

CHARACTERISTICS	SYMBOL	TEST CIRCUIT	BAND	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply and current 1 (PLL BLOCK)	Icc1	1	-	Bus data : band all [0]	-	15	-	mA
Power Supply and current 2 (BAND BLOCK)	Icc2	1	-	Pin13 and 14 : ON (IBD=0mA)	-	3.5	-	
				Pin14 or 15 (VHF) : ON (IBD=0mA)	-	3	-	
				Pin21 (UHF) : ON (IBD=0mA)	-	2	-	
Power Supply and current 3 (MIX BLOCK)	Icc3	1	VHF	Bus data :B1 or B2 : ON(IBD=0mA)	-	20	-	
			UHF	Bus data :B3 or B4 : ON(IBD=0mA)	-	14	-	
Power Supply and current 4 (OSC BLOCK)	Icc4	1	VHF-L	Bus data :B1 : ON(IBD=0mA)	-	6.5	-	
			VHF-H	Bus data :B2 : ON(IBD=0mA)	-	6.5	-	
			UHF	Bus data :B3 or B4 : ON(IBD=0mA)	-	16.5	-	
Power Supply and current 5 (IF BLOCK)	Icc5	1	-	-	-	15	-	
Power Supply and current 6 (GCA BLOCK)	Icc6	1	-	-	-	28.5	-	
Power Supply and current (TOTAL)	Icc Total	1	VHF-L	Bus data :B1 : ON(IBD=0mA)	73	88	108	
			VHF-H	Bus data :B2 : ON(IBD=0mA)	73	88	108	
			UHF	Bus data :B3 or B4 : ON(IBD=0mA)	76	91	111	

MIX / OSC / IF Block

(Unless otherwise specified,Vcc1 = Vcc2 = Vcc3 = Vcc4 = Vcc5 = Vcc6 = 5V, Ta = 25℃)

CHARACTERISTICS	SYMBOL	TEST CIRCUIT	BAND	TEST CONDITION (note4), (note5)	MIN.	TYP.	MAX.	UNIT
Conversion Gain (see1)	CG	3	VHF-L	RF=90MHz -30dBmWin	19.0	21.5	24.0	dB
			VHF-H	RF=465MHz -30dBmWin	20.5	23.0	25.5	
			UHF	RF=471MHz -30dBmWin	22.0	24.5	27.0	
			UHF	RF=855MHz -30dBmWin	21.5	24.0	26.5	
Noise Figure (see2)	NF	3, 4	VHF-L	RF=90MHz	-	13.5	15.0	dB
			VHF-H	RF=465MHz	-	11.0	12.5	
			UHF	RF=471MHz	-	11.5	13.0	
			UHF	RF=855MHz	-	11.0	12.5	
IF Output Power Level (see3)	Ifp	3	VHF-L	RF=90MHz	9	10	-	dBmW
			VHF-H	RF=465MHz	9	10	-	
			UHF	RF=471MHz	9	10	-	
			UHF	RF=855MHz	9	10	-	
Conversion Gain Shift (see4)	CGs	3	VHF-L	RF=90MHz –30dBmWin	-	-	±0.5	dB
			VHF-H	RF=465MHz -30dBmWin	-	-	±0.5	
			UHF	RF=471MHz -30dBmWin	-	-	±1.0	
			UHF	RF=855MHz -30dBmWin	-	-	±1.0	
Frequency Shift (The PLL Is not operating) (see5)	△fB	3	VHF-L	OSC=133.75MHz	-	-	±200	kHz
			VHF-H	OSC=508.75MHz	-	-	±500	
			UHF	OSC=514.75MHz	-	-	±500	
			UHF	OSC=898.75MHz	-	-	±500	
SW－ON Drift (The PLL Is not operating) (see6)	△fs	3	VHF-L	OSC=133.75MHz	-	-	±500	kHz
			VHF-H	OSC=508.75MHz	-	-	±1000	
			UHF	OSC=514.75MHz	-	-	±500	
			UHF	OSC=898.75MHz	-	-	±1000	
1% Cross Modulation (see7)	CM	3, 5	VHF-L	fd=90MHz	86	89	-	dBuV
			VHF-H	fd=465MHz	82	85	-	
			UHF	fd=471MHz	83	86	-	
			UHF	fd=855MHz	79	82	-	
3^{rd} Inter Modulation for MOP block (see8)	IM3-MO	3, 5	VHF-L	fd=90MHz	62	65	-	dB
			VHF-H	fd=465MHz	59	62	-	
			UHF	fd=471MHz	57	60	-	
			UHF	fd=855MHz	55	58	-	
Phase Noise (1kHz offset) (see9) freq-step=62.5kHz CP=Hi mode	PN1k	3	VHF-L	OSC=133.75MHz	-	-75	-68	dBc/Hz
			VHF-L	OSC=238.75MHz	-	-65	-58	
			VHF-H	OSC=244.75MHz	-	-72	-64	
			VHF-H	OSC=508.75MHz	-	-62	-58	
			UHF	OSC=514.75MHz	-	-65	-58	
			UHF	OSC=898.75MHz	-	-64	-58	
Phase Noise (10kHz offset) (see10) freq-step=62.5kHz CP=Hi mode	PN10k	3	VHF-L	OSC=133.75MHz	-	-89	-86	dBc/Hz
			VHF-L	OSC=238.75MHz	-	-89	-86	
			VHF-H	OSC=244.75MHz	-	-90	-86	
			VHF-H	OSC=508.75MHz	-	-88	-86	
			UHF	OSC=514.75MHz	-	-89	-86	
			UHF	OSC=898.75MHz	-	-90	-86	

(note4) IF output frequency: 43.75MHz (note5) IF output load: 75Ω

GCA Block (pin47=Open status)

(Unless otherwise specified,Vcc1 = Vcc2 = Vcc3 = Vcc4 = Vcc5 = Vcc6 = 5V, Ta = 25℃)

CHARACTERISTICS	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Voltage Gain	VGmax	3	VGCA=3V, RF=-60dBmW	45.0	47.0	49.0	dB
Typical Voltage Gain	VGtyp	3	VGCA=1.7V, RF=-37.5dBmW	21.5	23.5	25.5	
Minimum Voltage Gain	VGmin	3	VGCA=0.5V, RF=-15dBmW	-5.0	-3.0	-1.0	
Gain Variable Range	GR	3	VGCA=0.5～3V	46	50	54	dB
Gain Control Sensitivity	Sgain	3	VGCA=1.7V	27	30	33	dB/V
Lineality	LGCA	3	VGCA=1.1～2.3V	-	-	±1	dB
Output Signal Amplitude	Vout	3	-	-	0.35	-	Vpp
Maximum Output Signal Amplitude	Vomax	3	-	1.5	-	-	Vpp
Flow Into Current of GCA control pin.	Cont-I	3	Pin3 (Supply voltage range: 0～Vcc6)	-	-	50	uA
Noise Figure for GCA	NFgca	3, 6	GR=0dB, DSB	-	4.7	6.2	dB
			GR=10dB, DSB	-	5.2	6.7	
			GR=20dB, DSB	-	7.0	8.0	
			GR=30dB, DSB	-	12.0	13.0	
			GR=40dB, DSB	-	20.5	21.5	
3rd Inter Modulation for GCA	IM3-GCA	3, 7	f1=43.75MHz, f2=44.75MHz VGCA=3V(MAX Gain) V-out=0.5Vpp (2wave output) IF out =1.5kΩ+12pF(parallel)load	42	50	-	dB
			f1=43.75MHz, f2=44.75MHz VGCA=1.25V(Gain=10dB) V-out=0.5Vpp (2wave output) IF out =1.5kΩ+12pF(parallel)load	42	50	-	dB
2rd Inter Modulation for GCA	IM2-GCA	3, 8	f1=43.75MHz, f2=44.75MHz VGCA=3V(MAX Gain) V-out=1.0Vpp (2wave output) Between pin1,2=3kΩ+6pF(parallel)load	27	35	-	dB
			f1=43.75MHz, f2=44.75MHz VGCA=1.25V(Gain=10dB) V-out=1.0Vpp (2wave output) Between pin1,2=3kΩ+6pF(parallel)load	37	45	-	dB

(note6) The voltage value of VGCA shows the voltage value supplied to a terminal 3.
(note7) The voltage gain of GCA block can be Increased by 3dB by setting a pin47 to GND.

PLL / Band Block

(Unless otherwise specified,Vcc1 = Vcc2 = Vcc3 = Vcc4 = Vcc5 = Vcc6 = 5V, Ta = 25℃)

CHARACTERISTICS	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Band Port Drive Current	IBD-FMT	1	Pin13 (FMT port)	-	-	5	mA
	IBD-VHF		Pin14,15 (VHF port)	-	-	20	
	IBD-UHF		Pin21 (UHF port)	-	-	15	
Band Port Drive Maximum Current	IBDmax	1	Maximum drive current / 2 port ON	-	-	25	mA
Band Port Drive Voltage Drop	VBDsat	1	When each port maximum current drive	-	0.15	0.2	V
Tuning Amplifier Output Voltage (Close Loop)	Vt out	3	VBT = 33V, RL=33KΩ	0.3	-	33	V
Tuning Amplifier Maximum Current	Ivt	3	VBT = 33V	-	-	3	mA
X'tal Negative Resistance	XtR	1	-	1.2	1.5	-	kΩ
X'tal Operating Range	Xo fin	1	-	2	-	6	MHz
X'tal External Input Level	Xo extl	2	Ref freq. = 4MHz	300	-	1000	mVp-p
X'tal External Input Frequency Range	Xo extf	1	D/U>10dB (desire signal / un-desire signal)	2		20	MHz
Ratio Setting Range	N	-	15 bits counter	1024	-	32767	Ratio
Logic Input Low Voltage	VBsL	1	Pin5,6	-0.3	-	1.1	V
Logic Input High Voltage	VBsH	1	Pin5,6	2.0	-	Vcc2 +0.3	V
Logic Input Current (Low)	I BsL	1	Pin5,6	-20	-	10	uA
Logic Input Current (High)	I BsH	1	Pin5,6	-10	-	20	uA
Charge Pump Output Current	Ichg	1	CP = 0	±115	±145	±175	uA
			CP = 1	±165	±210	±255	
ACK Output Voltage	VACK	1	ISINK=3mA	-	-	0.2	V

I²C Bus Line Characteristic

CHARACTERISTICS	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SCL Clock Frequency	fscl	–	0	-	400	kHz
Bus Free Time Between a STOP and Start Condition	tBUF		1.3	-	-	us
Hold Time (Repeated) START Condition	tHD;STA		0.6	-	-	us
Low Period of the SCL Clock	tLOW		1.3	-	-	us
High Period of the SCL Clock	tHIGH		0.6	-	-	us
Set up Time for a Repeated START Condition	tSU;STA		0.6	-	-	us
Data Hold Time	tHD;DAT		0	-	0.9	us
Data Set up Time	tSU;DAT		100	-	-	ns
Rise Time of both SDA and SCL Signal	tR		-	-	300	ns
Fall Time of both SDA and SCL Signals	tF		-	-	300	ns
Set up Time for STOP Condition	tsU;STO		0.6	-	-	us

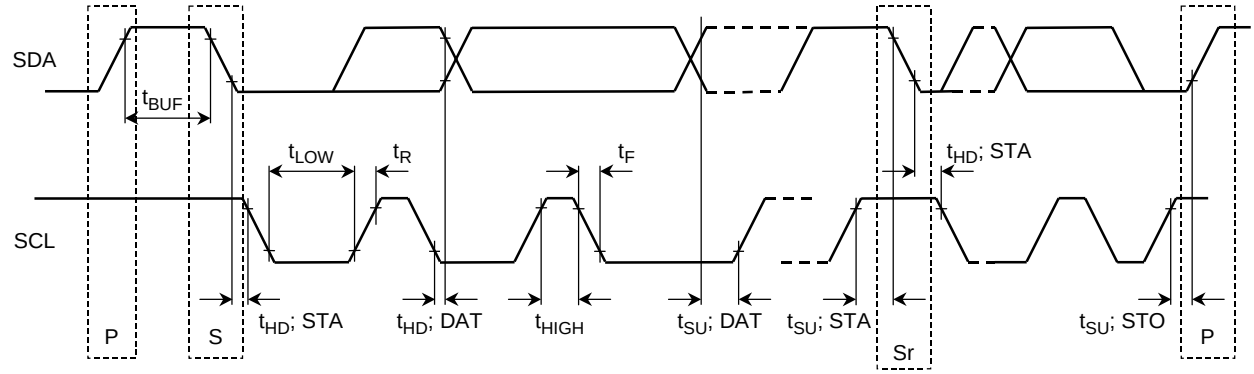


Fig.1 I²C-bus data timing chart (Rising edge timing)

Timing charts may be simplified for explanatory purpose.

Test Circuit

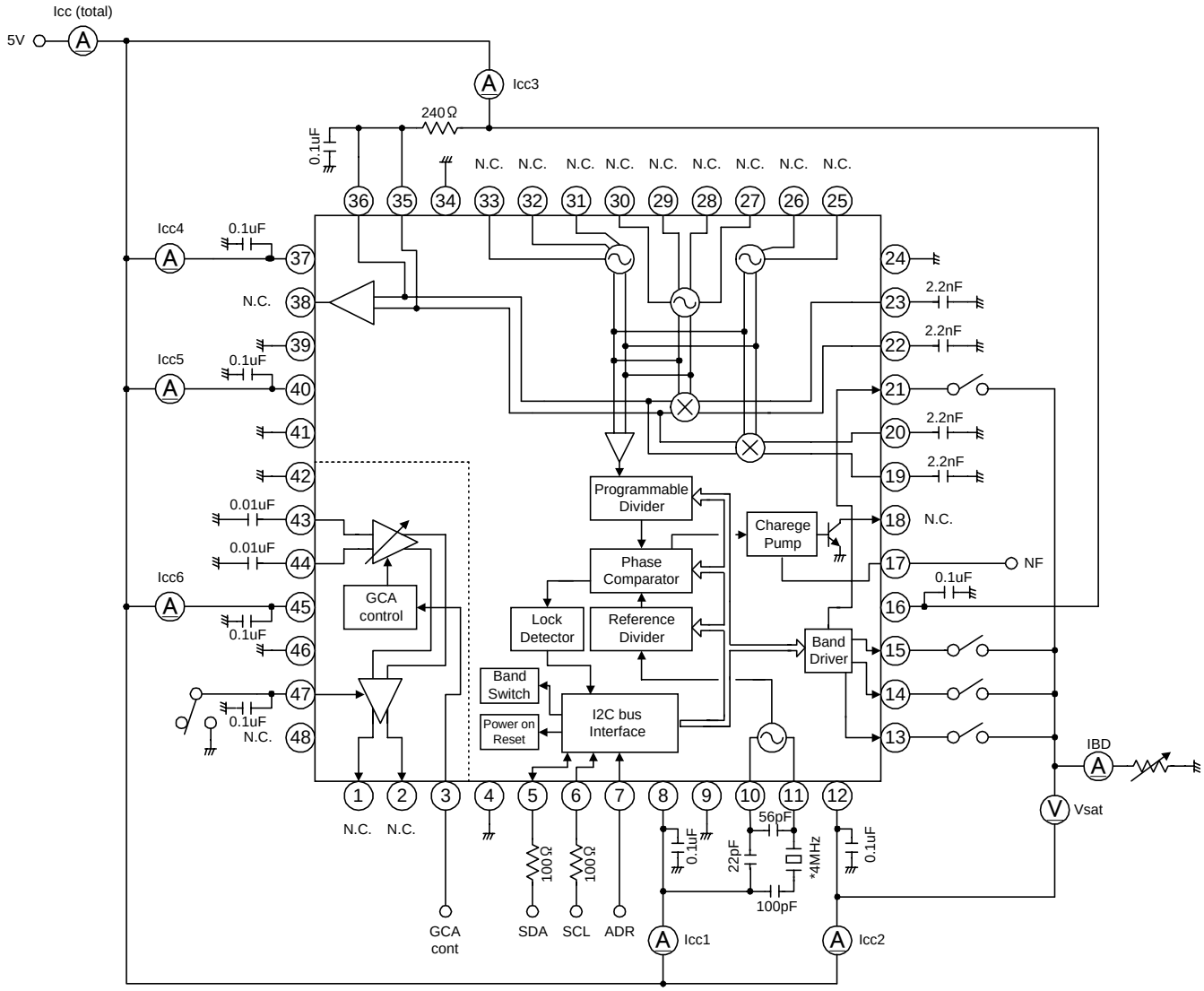


Fig.2 Test Circuit 1

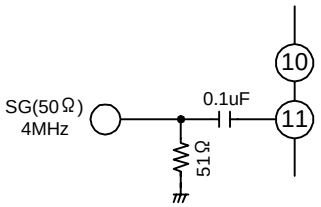


Fig.3 Test Circuit 2 (X'tal :4MHz External Input)

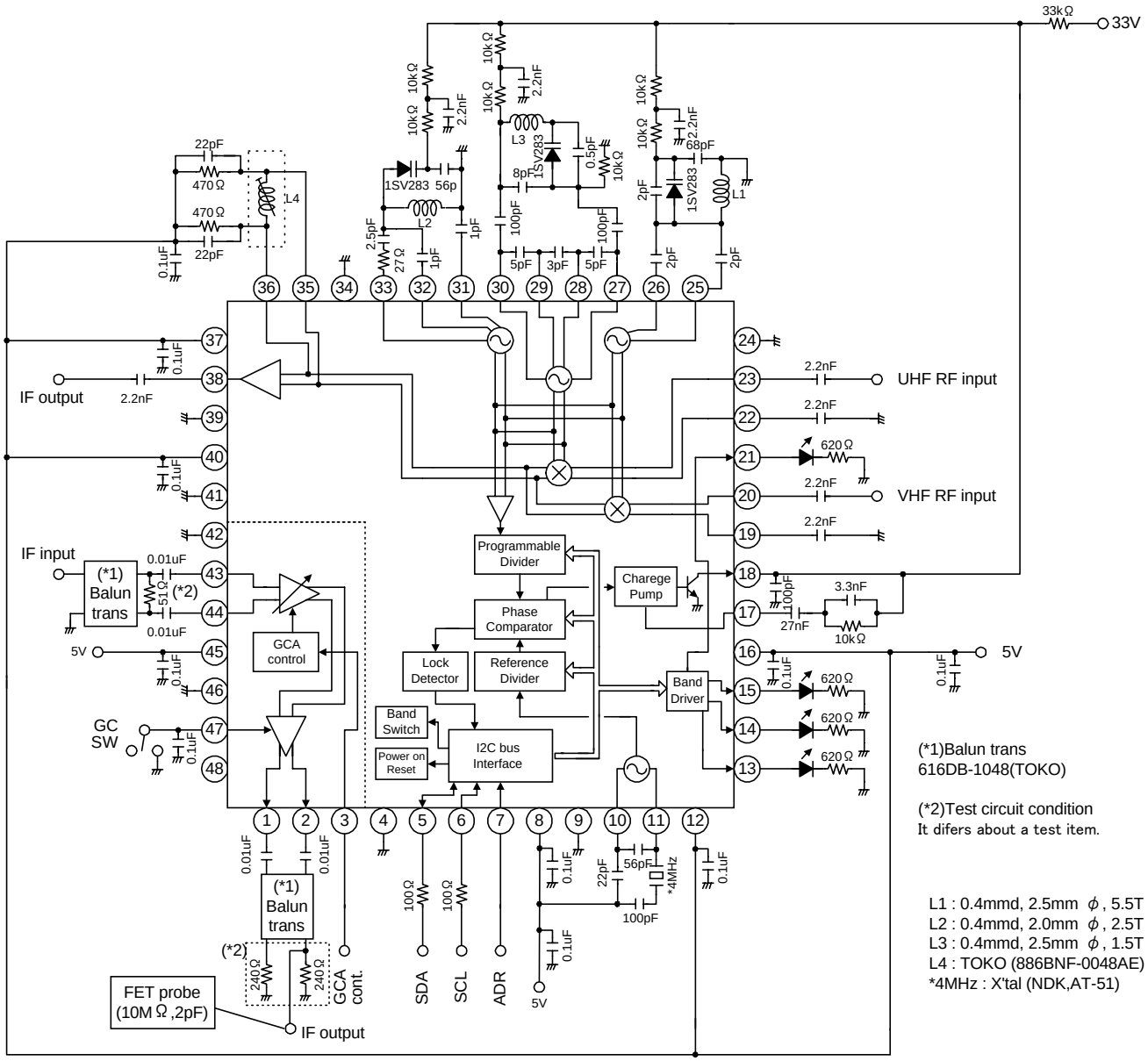
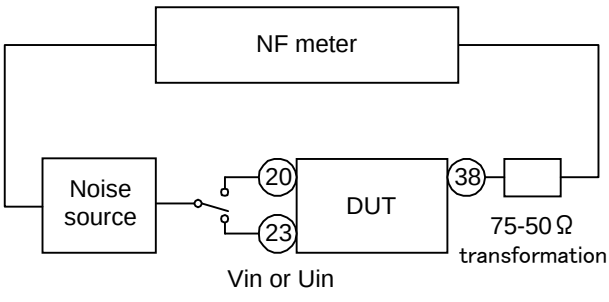


Fig.4 Test Circuit 3



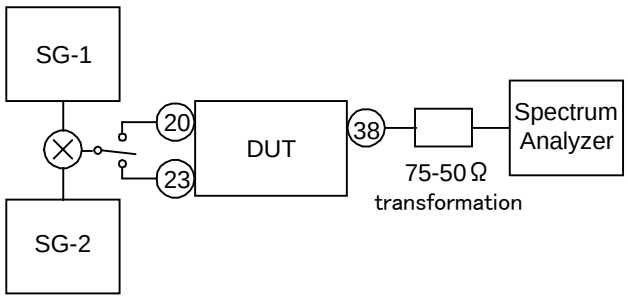


Fig.5 Test Circuit 4 (MOP Block : NF) **Fig.6 Test Circuit 5 (MOP Block : IM3 / CM)**

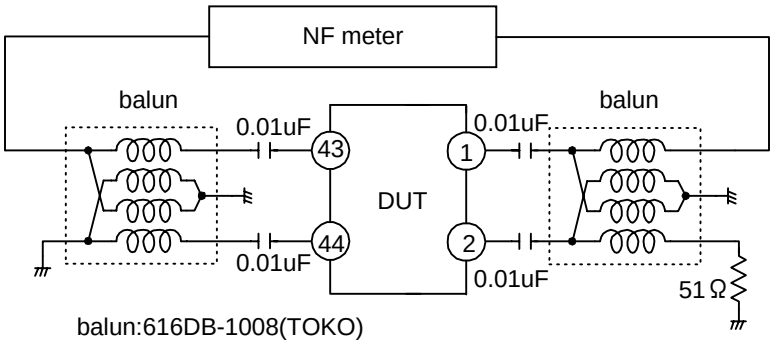


Fig.7 Test Circuit 6 (GCA Block : NF)

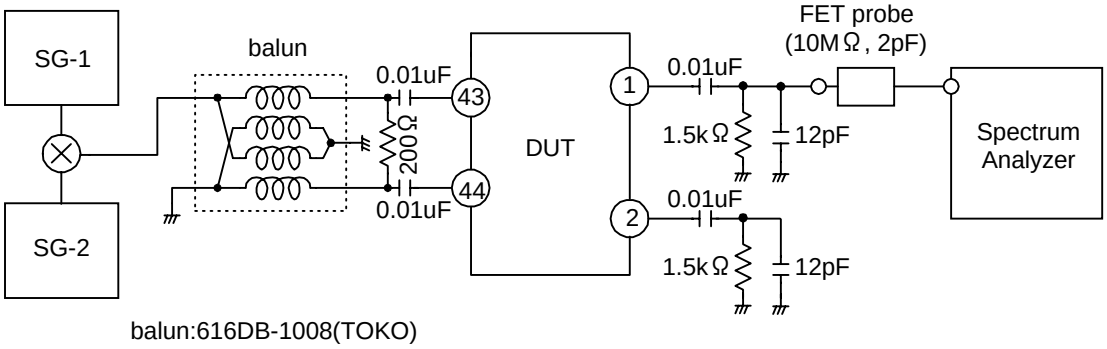


Fig.8 Test Circuit 7 (GCA Block : IM3)

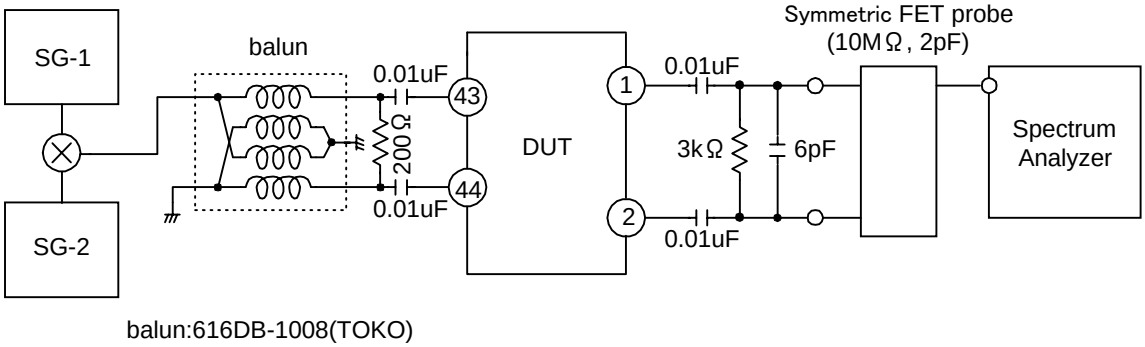


Fig.9 Test Circuit 8 (GCA Block : IM2)

MOP Block Test Conditions

(see1) Conversion Gain
RF Input level = -30dBmW (untuned)

(see2) Noise Figure
Noise figure meter used. Direct reading.

(see3) IF Output Power Level
Measure IF output level when It Is maximum level.

(see4) Conversion Gain Shift
The conversion gain shift Is defined as a change In conversion gain when supply voltage varies from Vcc=5V to 4.5V or From Vcc=5V to 5.25V.

(see5) Frequency Shift (The PLL Is not operating)
The frequency shift Is defined as a change In oscillator frequency when supply voltage varies from Vcc=5V to 4.5V or From Vcc=5V to 5.25V.

(see6) SW-ON Drift (The PLL Is not operating)
Measure frequency change from 2 seconds after switching on to 3 minutes.

(see7) 1% Cross Modulation
- fd = fp : (fd Input level = -30dBmW)
- fud = fp ±12MHz, 100kHz AM30%

Input two signals, and Increase the fud Input level.
Measure the fud Input level when the suppression level reaches 56.5dB.

(see8) 3rd Internal Modulation
- fd = fp : (fd Input level = -30dBmW)
- fud = fp ±1MHz : (fud Input level = -30dBmW)

Input two signals, measure the suppression level.

(see9) Phase Noise (1kHz offset)
Measure the phase noise at 1kHz offset. (PLL setting; frequency step = 62.5kHz / charge pump current = High mode)
RF Input level = -30dBmW

(see10) Phase Noise (10kHz offset)
Measure the phase noise at 10kHz offset. (PLL setting; frequency step = 62.5kHz / charge pump current = High mode)
RF Input level = -30dBmW

PLL Block (Explanation For The Operation)

- I²C bus control -

The TA1375FG conform to I²C-bus format.
The I²C-bus mode enables two-way bus communications with the WRITE MODE, which receives data, and READ MODE, which status data.
WRITE and READ MODE are set using the last bit (R/W bit) of the address byte.
If the last address bit is set to [0], WRITE MODE is set ; if set to [1] ,READ MODE is set.
Address can be set using the hardware bits. 4 programmable address can be programmed.
With this setting, multiple frequency synthesizers can be used in the same I²C-bus.
The address for the hardware bit setting can be selected by applying voltage to the address setting pin (ADR:pin7).An address is selected according to the set bits.
When the correct address byte is received, during acknowledgment, serial data (SDA) line is `Low`.
If WRITE mode is set at this time, when the data byte is programmed, the serial data (SDA) line is `Low` during the next acknowledgment.

A) WRITE MODE (setting command)

When WRITE mode is set, byte 1 segment the address data ; byte 2, byte 3 segment the frequency data ; byte 4 segment the divider ratio setting and function setting data ; and byte 5 segment the output port data.
Data are latched and transferred at the end of byte 3,byte 4 and byte 5.
Byte 2 and byte 3 are latched and transferred is done with a two bytes set (byte 2 + byte 3).
Once a correct address is received and acknowledged, the data type is determined according to [0] or [1] set in the first bit of the next byte. That is, if the first bit is [0], the data are frequency data ; if [1], function setting or output data.
Until the I²C-bus STOP CONDITION is detected, the additional data can be input without transmitting the address data again. (EX: Frequency sweep is possible with additional frequency data.)
If data transmission is aborted, data programmed before the abort are valid.

[[BYTE 1]]

Byte 1 can be set the hardware bit with address data.
The hardware bit is set with voltage applied to the address setting pin (ADR:pin7).

[[BYTE 2 , BYTE 3]]

Byte 2 , byte 3 are stored in the 15-bit shift register with counter data for the frequency setting, and control the 15-bit programmable counter ratio.
The program frequency can be calculated in the following formula :

$fosc = fr \times N$

fosc : Program frequency
fr : Phase comparator reference frequency (Step frequency)
N : Counter total divider ratio

fr is calculated using the crystal oscillator and the reference frequency divider ratio set in byte 4 (control byte).
(fr=X'tal oscillator frequency / reference divider ratio)
The reference frequency divider ratio can be set to 1/64 , 1/80, 1/24 and 1/28.
When using a 4MHz crystal oscillator, fr=62.5kHz , 50.0kHz , 166.67kHz and 142.86kHz.
The step frequency are 62.5kHz , 50.0kHz , 166.67kHz and 142.86kHz.

[[BYTE 4]]

Byte4 is a control byte used to set function. Bit 2 (CP) and controls the output current of the charge-pump circuit. When bit 2 is set to [0] : the output current is set to $\pm$145uA ; when set to [1] , $\pm$210uA.
Bit 3 (T2), bit 4 (T1), bit 5 (T0) are used to set test mode. They are used to set the phase comparator reference signal output, and counter divider output. (For details of test mode, see the test mode setting table.)
Bit 6 (Rsa) and bit 7 (Rsb) are used to set the X'tal reference frequency divider ratio.(For details of the X'tal reference frequency divider ratio, see the table for X'tal reference frequency divider ratios.)
Bit 8 (OS) is used to set the charge-pump driver amplifier output setting. When bit 8 is set to [0] the output is ON (normal used) ; when set to [1] the output is OFF.

[[BYTE 5]]

Byte 5 is used to set the test mode and control the output port (VHF-L, VHF-H, UHF and FMT).
When an output port set to [0] is OFF ; when set to [1] is ON.
As setting the band switch data, It can be control change of VHF or UHF, band switch driver.

No.	Band SW Data (setting data)				Mixer		Oscillator			Band Drive Port			
-	B4	B3	B2	B1	VHF	UHF	VL	VH	U	VL	VH	U	FMT
1	0	0	0	0	×	×	×	×	×	×	×	×	×
2	0	0	0	1	○	×	○	×	×	○	×	×	×
3	0	0	1	0	○	×	×	○	×	×	○	×	×
4	0	1	0	0	×	○	×	×	○	×	×	○	×
5	1	0	0	0	×	○	×	×	○	×	×	○	×
6	0	1	0	1	○	×	○	×	×	○	×	×	○
7	1	0	0	1	○	×	○	×	×	○	×	×	○

○: Operation
×: Not operation

When It Is setting the band sw data excepts from No.1 to No.7, this Is not operating mixer, oscillator and band switch driver.

Please give the following currents to band switch driver respectively as the maximum value. If the band switch driver operates 2-port 'ON'(when setting data Is No.6 and No.7) , total band driver curent Is below 25mA.

VHF-L band switch driver (pin14) output current : 20mA(maximum)
VHF-H band switch driver (pin15) output current : 20mA(maximum)
UHF band switch driver (pin21) output current : 15mA(maximum)
VHF-L and FMT band switch driver (pin13 and 14) output total current : 25mA(maximum)

B) READ MODE (status request)

When READ mode is set, power-on reset operation status, phase comparator lock detector output status are output to the master device.
Bit 1 (POR) indicates the power-on reset operation status. When the power supply of Vcc1 stops, bit is set to [1]. The condition for reset to [0], voltage supplied to Vcc1 is 3V or higher, transmission is requested in READ MODE, and the status is output. (when Vcc1 is turned on, bit 1 is also set to [1].)
Bit 2 (FL) indicates the phase comparator lock status. When locked, [1] is output ; when unlocked, [0] is output.
The power-on reset circuit is built In this product, and the detection voltage Is designed about 1.5V.
If It raises to voltage of operation after making It stop for a while near the voltage of a power-on reset circuit of operation at the time of starting of a power supply, a power-on reset circuit may not operation normally.

DATA FORMAT

A) WRITE MODE

		MSB							LSB	
1	Address Byte	1	1	0	0	0	MA1	MA0	R/W=0	ACK
2	Divider Byte 1	0	N14	N13	N12	N11	N10	N9	N8	ACK
3	Divider Byte 2	N7	N6	N5	N4	N3	N2	N1	N0	ACK(L)
4	Control Byte	1	CP	T2	T1	T0	Rsa	Rsb	OS	ACK(L)
5	Band SW Byte	×	×	×	×	B4	B3	B2	B1	ACK(L)

× :DON'T CARE
ACK :Acknowledged
(L) :Latch and transfer timing

B) READ MODE

		MSB							LSB	
1	Address Byte	1	1	0	0	0	MA1	MA0	R/W=1	ACK
2	Status Byte	POR	FL	1	1	1	1	1	1	-

ACK :Acknowledged

DATA SPECIFICATIONS

●MA1,MA0 : programmable hardware address bits

MA1	MA0	ADDRESS PIN APPLIED VOLTAGE
0	0	0 to 0.1Vcc1
0	1	OPEN or 0.2Vcc1 to 0.3Vcc1
1	0	0.4Vcc1 to 0.6Vcc1
1	1	0.9Vcc1 to Vcc1

●N14 – N0 : programmable counter data

● CP : charge pump output current setting
[0] : ± 145uA(typ.)
[1] : ± 210uA(typ)

●T2,T1,T0 : test mode setting bits

CHARACTERISTIC		T2	T1	T0	NOTE
Normal operation		0	0	×	-
Charge-pump	OFF	0	1	×	Charge pump is OFF (check output : NF)
	SINK	1	1	0	Only charge pump sink current is ON (check output : NF)
	SOURCE	1	1	1	Only charge pump source current is ON (check output : NF)
Reference signal output		1	0	0	Reference signal output (check output : pin21)
1/2 counter divider output		1	0	1	1/2 counter output (check output : pin15)

(note8) When testing the counter divider output, programmable counter data input is necessary.

●Rsa,Rsb : reference frequency divider ratio select bit.

Rsa	Rsb	DIVIDER RATIO	STEP FREQUENCY
0	0	1/80	50.0kHz
0	1	1/28	142.86kHz
1	0	1/24	166.67kHz
1	1	1/64	62.5kHz

●OS : tuning amplifier control bit
[0] : tuning amplifier ON (normal operation)
[1] : tuning amplifier OFF

●POR : power on reset flag
[0] : normal operation
[1] : reset operation

●FL : lock detect flag
[0] : unlocked
[1] : locked

●× : don't care

-EXAMPLE OF BUS DATA TRANSMITTER-

S : Start
ADR : Address Byte
DIV1 : Divider Byte 1 (frequency data)
DIV2 : Divider Byte 2 (frequency data)
CONT : Control Byte
BAND : Band SW Byte
A : Acknowledge
P : Stop

[1] Transmitter - 1

S	ADR	A	DIV1	A	DIV2	A	CONT	A	BAND	A	P

[2] Transmitter - 2

S	ADR	A	CONT	A	BAND	A	DIV1	A	DIV2	A	P

[3] Transmitter – 3 (It applies when it already is set control and band data.)

S	ADR	A	DIV1	A	DIV2	A	P

[4] Transmitter – 4 (It applies when it already is set frequency data.)

S	ADR	A	CONT	A	BAND	A	P

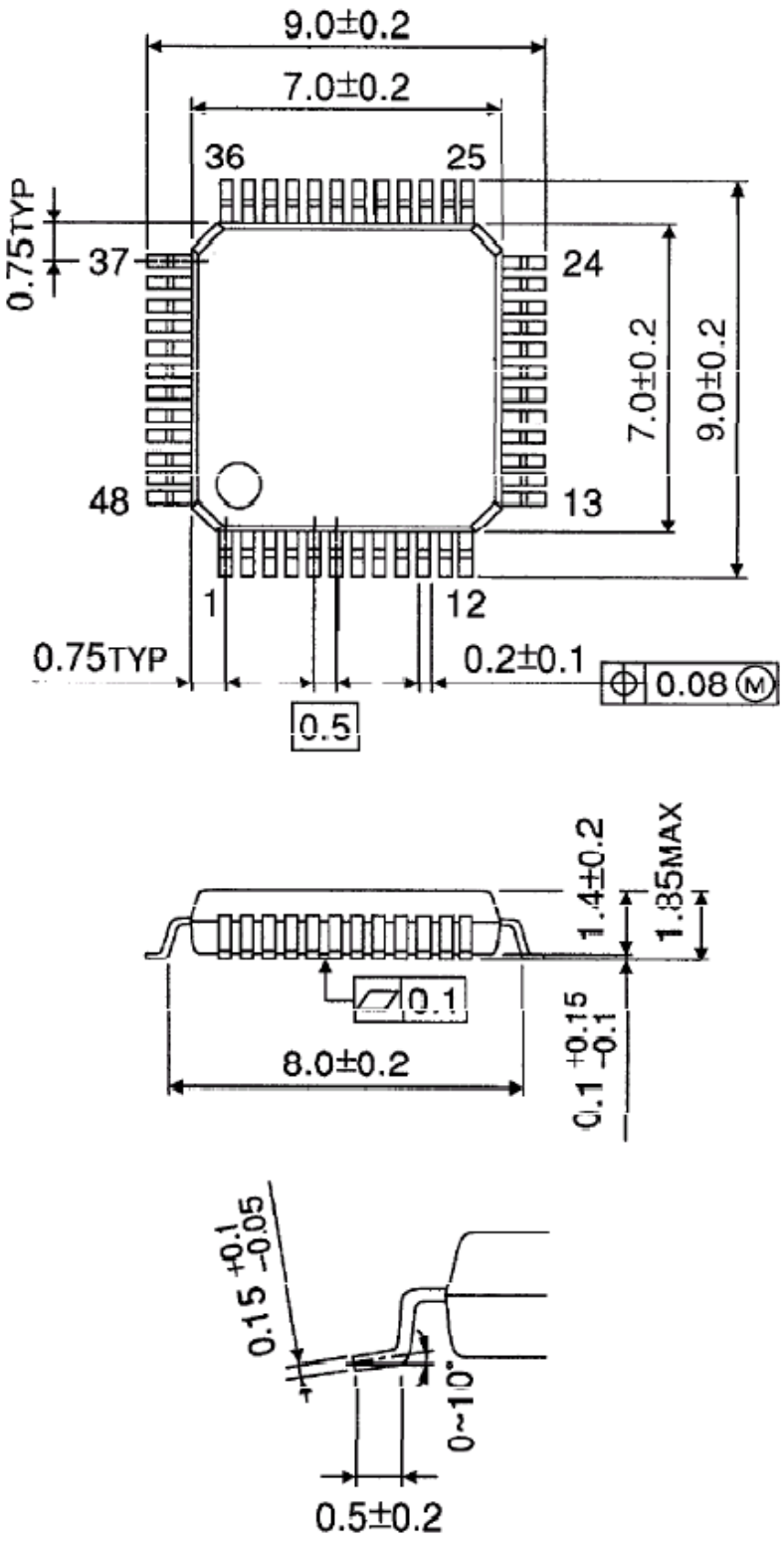
[5] Transmitter – 5 (It applies when it already is set frequency and band data.)

S	ADR	A	CONT	A	P

The I²C-bus STOP CONDITION is detected, the additional data can be input without transmitting the address data again.
(EX: Frequency sweep is possible with additional frequency data.)
If data transmission is aborted, data programmed before the abort are valid.

OUTLINE DRAWING

LQFP48-P-0707-0.50 Unit : mm



Weight: 0.17g (typ.)

HANDLING PRECAUTIONS

1.The device should not be inserted into or removed from the test jig while the voltage is being applied: otherwise the device may be degraded or break down.
Do not abruptly increase or decrease the power supply to the device either.
Overshoot or chattering of the power supply may cause the IC to be degraded.
To avoid this filters should be incorporated on the power supply line.

2.The peripheral circuits described in this datasheet are given only as system examples for evaluating the device's performance. Toshiba Intend neither to recommend the configuration or related values of the peripheral circuits nor to manufacture such application system in large quantities.
Please note that high-frequency characteristics of the device may vary depending on the external components, mounting method and other factors relating to the application design. Therefore, the characteristics of application circuits must be evaluated at the responsibility of the users incorporating the device into their design.
Toshiba only guarantee the quality and characteristics of the device as described in this datasheet and do not assume any responsibility for the customer's application design.

3.In order to better understand the quality and reliability of Toshiba semiconductor products and to incorporate them into design in an appropriate manner, please refer to the latest Semiconductor Reliability Handbook (Integrated Circuit) published by Toshiba Semiconductor Company.
The handbook can also be viewed online at " http://www.semicon.toshiba.co.jp/ "