BURR - BROWN®

DAC7644

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16-Bit, Quad Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 10mW
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 10µs to 0.003%
- 15-BIT LINEARITY AND MONOTONICITY: –40°C to +85°C
- PROGRAMMABLE RESET TO MID-SCALE OR ZERO-SCALE
- DATA READBACK
- DOUBLE-BUFFERED DATA INPUTS

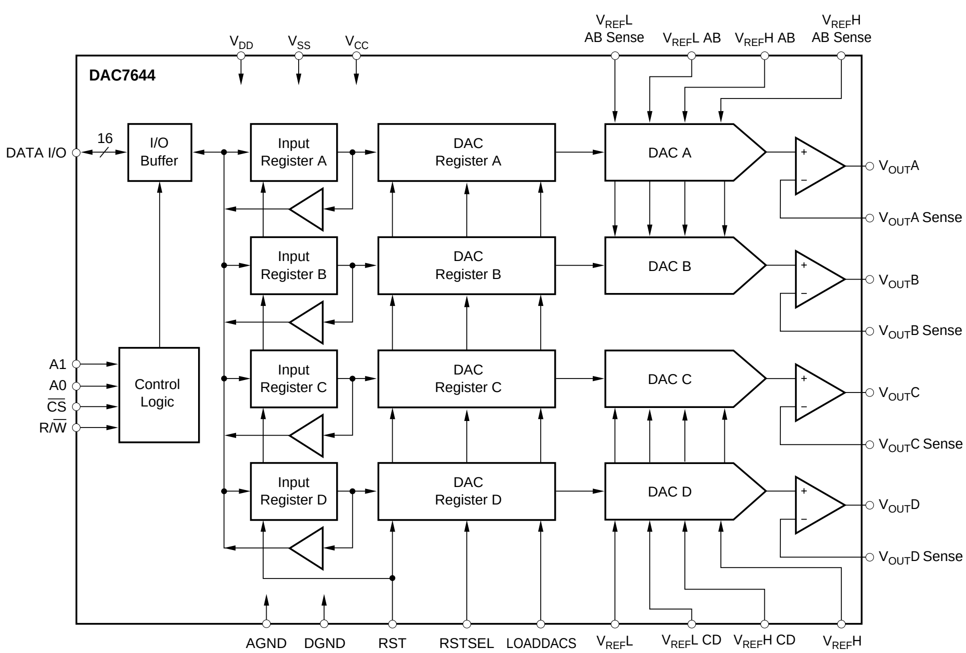
APPLICATIONS

- PROCESS CONTROL
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS
- DAC-PER-PIN PROGRAMMERS

DESCRIPTION

The DAC7644 is a 16-bit, quad voltage output digital-to-analog converter with guaranteed 15-bit monotonic performance over the specified temperature range. It accepts 16-bit parallel input data, has double-buffered DAC input logic (allowing simultaneous update of all DACs), and provides a readback mode of the internal input registers. Programmable asynchronous reset clears all registers to a mid-scale code of 8000_H or to a zero-scale of 0000_H. The DAC7644 can operate from a single +5V supply or from +5V and –5V supplies.

Low power and small size per DAC make the DAC7644 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7644 is available in a 48-lead SSOP package and offers guaranteed specifications over the –40°C to +85°C temperature range.



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SBAS121

SPECIFICATIONS (Dual Supply)

At $T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = V_{CC} = +5V$, $V_{SS} = –5V$, $V_{REF}H = +2.5V$, and $V_{REF}L = –2.5V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7644E MIN	DAC7644E TYP	DAC7644E MAX	DAC7644EB MIN	DAC7644EB TYP	DAC7644EB MAX	UNITS
ACCURACY								
Linearity Error			±3	±4		±2	±3	LSB
Linearity Match			±4			±2		LSB
Differential Linearity Error			±2	±3		±1	±2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			Bits
Bipolar Zero Error			±1	±2		*	*	mV
Bipolar Zero Error Drift			5	10		*	*	ppm/°C
Full-Scale Error			±1	±2		*	*	mV
Full-Scale Error Drift			5	10		*	*	ppm/°C
Bipolar Zero Matching	Channel-to-Channel Matching		±1	±2		±1	±2	mV
Full Scale Matching	Channel-to-Channel Matching		±1	±2		±1	±2	mV
Power Supply Rejection Ratio (PSRR)	At Full Scale		10	100		*	*	ppm/V
ANALOG OUTPUT								
Voltage Output	$V_{REF} = –2.5V$, $R_L = 10k\Omega$, $V_{SS} = –5V$	$V_{REF}L$		$V_{REF}H$	*		*	V
Output Current		–1.25		+1.25	*		*	mA
Maximum Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			–10, +30			*		mA
Short-Circuit Duration	GND or V_{CC} or V_{SS}		Indefinite			*		
REFERENCE INPUT								
Ref High Input Voltage Range		$V_{REF}L + 1.25$		+2.5	*		*	V
Ref Low Input Voltage Range		–2.5		$V_{REF}H – 1.25$	*		*	V
Ref High Input Current			500			*		µA
Ref Low Input Current			–500			*		µA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.003%, 5V Output Step		8	10		*	*	µs
Channel-to-Channel Crosstalk	See Figure 5.		0.5			*		LSB
Digital Feedthrough			2			*		nV-s
Output Noise Voltage	f = 10kHz		60			*		$nV/\sqrt{Hz}$
DAC Glitch	$7FFF_H$ to 8000_H or 8000_H to $7FFF_H$		40			*		nV-s
DIGITAL INPUT								
V_{IH}		$0.7 \bullet V_{DD}$			*			V
V_{IL}				$0.3 \bullet V_{DD}$			*	V
I_{IH}				±10			*	µA
I_{IL}				±10			*	µA
DIGITAL OUTPUT								
V_{OH}	$I_{OH} = –0.8mA$	3.6	4.5		*	*		V
V_{OL}	$I_{OL} = 1.2mA$		0.3	0.4		*	*	V
POWER SUPPLY								
V_{DD}		+4.75	+5.0	+5.25	*	*	*	V
V_{CC}		+4.75	+5.0	+5.25	*	*	*	V
V_{SS}		–5.25	–5.0	–4.75	*	*	*	V
I_{CC}			1.5	2		*	*	mA
I_{DD}			50			*		µA
I_{SS}		–2.3	–1.5		*	*		mA
Power			15	20		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Specifications same as DAC7644E.

SPECIFICATIONS (Single Supply)

At $T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REF}H = +2.5V$, and $V_{REF}L = 0V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7644E MIN	DAC7644E TYP	DAC7644E MAX	DAC7644EB MIN	DAC7644EB TYP	DAC7644EB MAX	UNITS
ACCURACY								
Linearity Error[1]			±3	±4		±2	±3	LSB
Linearity Match			±4			±2		LSB
Differential Linearity Error			±2	±3		±1	±2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			Bits
Zero Scale Error			±1	±2		*	*	mV
Zero Scale Error Drift			5	10		*	*	ppm/°C
Full-Scale Error			±1	±2		*	*	mV
Full-Scale Error Drift			5	10		*	*	ppm/°C
Zero Scale Matching	Channel-to-Channel Matching		±1	±2		±1	±2	mV
Full-Scale Matching	Channel-to-Channel Matching		±1	±2		±1	±2	mV
Power Supply Rejection Ratio (PSRR)	At Full Scale		10	100		*	*	ppm/V
ANALOG OUTPUT								
Voltage Output	$V_{REF}L = 0V$, $V_{SS} = 0V$, $R_L = 10k\Omega$	0		$V_{REF}H$	*		*	V
Output Current		–1.25		+1.25	*		*	mA
Maximum Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			±30			*		mA
Short-Circuit Duration	GND or V_{CC}		Indefinite			*		
REFERENCE INPUT								
Ref High Input Voltage Range		$V_{REF}L + 1.25$		+2.5	*		*	V
Ref Low Input Voltage Range		0		$V_{REF}H – 1.25$	*		*	V
Ref High Input Current			250			*		µA
Ref Low Input Current			–250			*		µA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.003%, 2.5V Output Step		8	10		*	*	µs
Channel-to-Channel Crosstalk	See Figure 6.		0.5			*		LSB
Digital Feedthrough			2			*		nV-s
Output Noise Voltage, f = 10kHz			60			*		$nV/\sqrt{Hz}$
DAC Glitch	$7FFF_H$ to 8000_H or 8000_H to $7FFF_H$		40			*		nV-s
DIGITAL INPUT								
V_{IH}		$0.7 \cdot V_{DD}$			*			V
V_{IL}				$0.3 \cdot V_{DD}$			*	V
I_{IH}				±10			*	µA
I_{IL}				±10			*	µA
DIGITAL OUTPUT								
V_{OH}	$I_{OH} = –0.8mA$	3.6	4.5		*	*		V
V_{OL}	$I_{OL} = 1.2mA$		0.3	0.4		*	*	V
POWER SUPPLY								
V_{DD}		+4.75	+5.0	+5.25	*	*	*	V
V_{CC}		+4.75	+5.0	+5.25	*	*	*	V
V_{SS}		0	0	0	*	*	*	V
I_{CC}			1.5	2		*	*	mA
I_{DD}			50			*		µA
Power			7.5	10		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

NOTE: (1) If $V_{SS} = 0V$ specification applies at Code 0040_H and above due to possible negative zero-scale error.

* Specifications same as DAC7644E.

ABSOLUTE MAXIMUM RATINGS(1)

V_{CC} and V_{DD} to V_{SS} .... –0.3V to 11V
V_{CC} and V_{DD} to GND .... –0.3V to 5.5V
$V_{REF}L$ to V_{SS} .... –0.3V to (V_{CC} – V_{SS})
V_{CC} to $V_{REF}H$ .... –0.3V to (V_{CC} – V_{SS})
$V_{REF}H$ to $V_{REF}L$ .... –0.3V to (V_{CC} – V_{SS})
Digital Input Voltage to GND .... –0.3V to V_{DD} + 0.3V
Digital Output Voltage to GND .... –0.3V to V_{DD} + 0.3V
Maximum Junction Temperature .... +150°C
Operating Temperature Range .... –40°C to +85°C
Storage Temperature Range .... –65°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

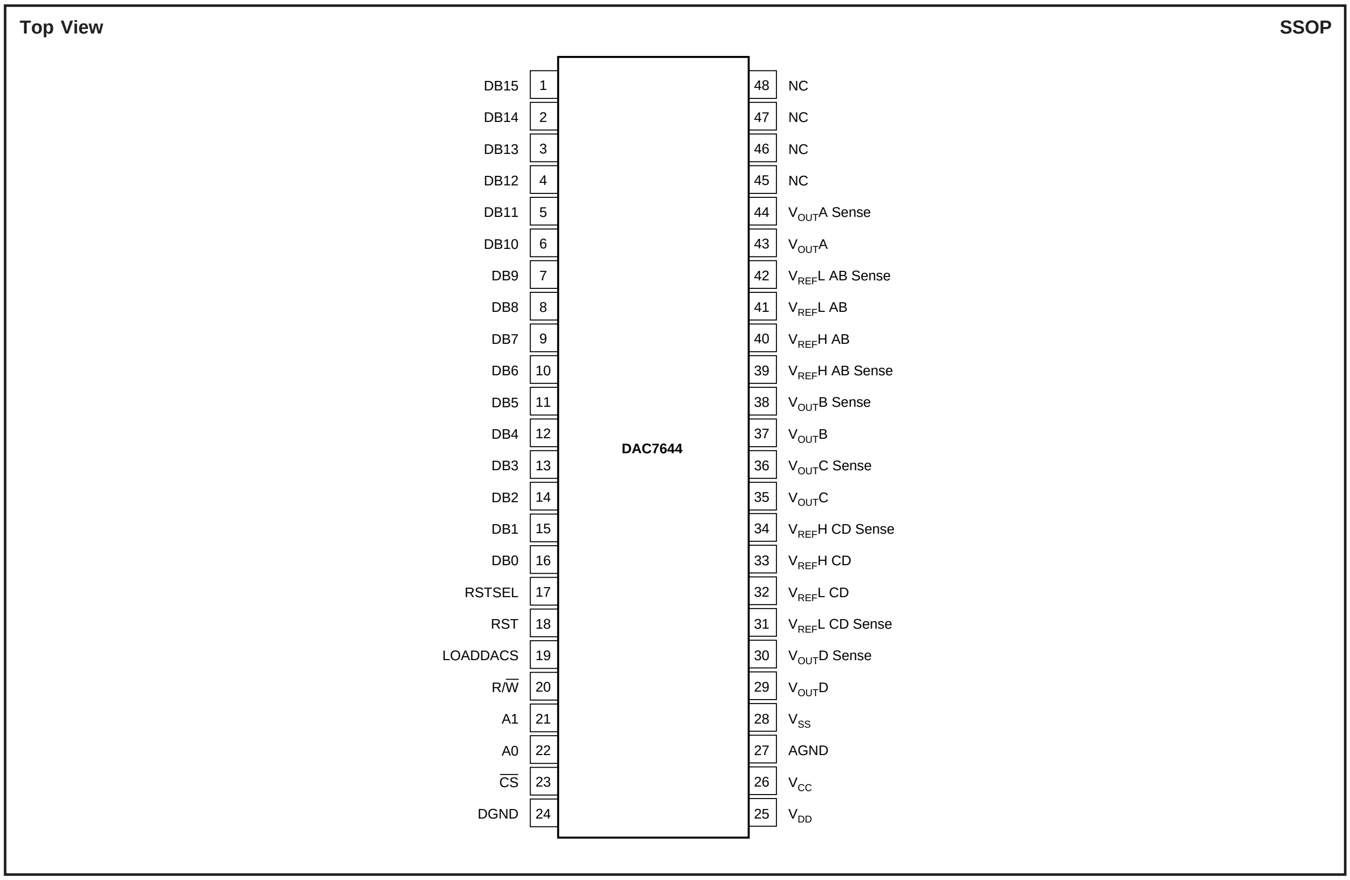
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	LINEARITY ERROR (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER(2)	TRANSPORT MEDIA
DAC7644E	±4	±3	48-Lead SSOP	333	–40°C to +85°C	DAC7644E	Rails
"	"	"	"	"	"	DAC7644E/1K	Tape and Reel
DAC7644EB	±3	±2	48-Lead SSOP	333	–40°C to +85°C	DAC7644EB	Rails
"	"	"	"	"	"	DAC7644EB/1K	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DAC7644/1K" will get a single 1000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

PIN CONFIGURATION



PIN DESCRIPTIONS

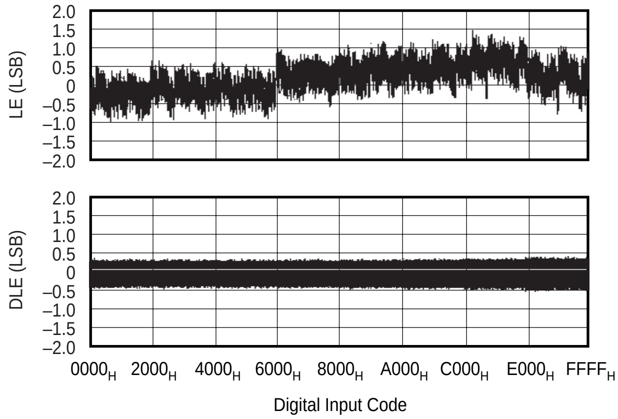
PIN	NAME	DESCRIPTION
1	DB15	Data Bit 15, MSB
2	DB14	Data Bit 14
3	DB13	Data Bit 13
4	DB12	Data Bit 12
5	DB11	Data Bit 11
6	DB10	Data Bit 10
7	DB9	Data Bit 9
8	DB8	Data Bit 8
9	DB7	Data Bit 7
10	DB6	Data Bit 6
11	DB5	Data Bit 5
12	DB4	Data Bit 4
13	DB3	Data Bit 3
14	DB2	Data Bit 2
15	DB1	Data Bit 1
16	DB0	Data Bit 0, LSB
17	RSTSEL	Reset Select. Determines the action of RST. If HIGH, a RST command will set the DAC registers to mid-scale. If LOW, a RST command will set the DAC registers to zero.
18	RST	Reset, Rising Edge Triggered. Depending on the state of RSTSEL, the DAC registers are set to either mid-scale or zero.
19	LOADDACS	DAC Output Registers Load Control. Rising edge triggered.
20	R/$\overline{W}$	Enabled by the $\overline{CS}$, Controls Data Read and Write from the Input Registers.
21	A1	Enabled by the $\overline{CS}$, in Combination With A0 Selects the Individual DAC Input Registers.
22	A0	Enabled by the $\overline{CS}$, in Combination With A1 Selects the Individual DAC Input Registers.
23	$\overline{CS}$	Chip Select. Active LOW.
24	DGND	Digital Ground
25	V_{DD}	Positive Power Supply (digital)
26	V_{CC}	Positive Power Supply (analog)
27	AGND	Analog Ground
28	V_{SS}	Negative Power Supply
29	V_{OUT}D	DAC D Voltage Output
30	V_{OUT}D Sense	DAC D's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
31	V_{REF}L CD Sense	DAC C and D Reference Low Sense Input
32	V_{REF}L CD	DAC C and D Reference Low Input
33	V_{REF}H CD	DAC C and D Reference High Input
34	V_{REF}H CD Sense	DAC C and D Reference High Sense Input
35	V_{OUT}C	DAC C Voltage Output
36	V_{OUT}C Sense	DAC C's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
37	V_{OUT}B	DAC B Voltage Output
38	V_{OUT}B Sense	DAC B's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
39	V_{REF}H AB Sense	DAC A and B Reference High Sense Input
40	V_{REF}H AB	DAC A and B Reference High Input
41	V_{REF}L AB	DAC A and B Reference Low Input
42	V_{REF}L AB Sense	DAC A and B Reference Low Sense Input
43	V_{OUT}A	DAC A Voltage Input
44	V_{OUT}A Sense	DAC A's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
45	NC	No Connection
46	NC	No Connection
47	NC	No Connection
48	NC	No Connection

TYPICAL PERFORMANCE CURVES: V_{SS} = 0V

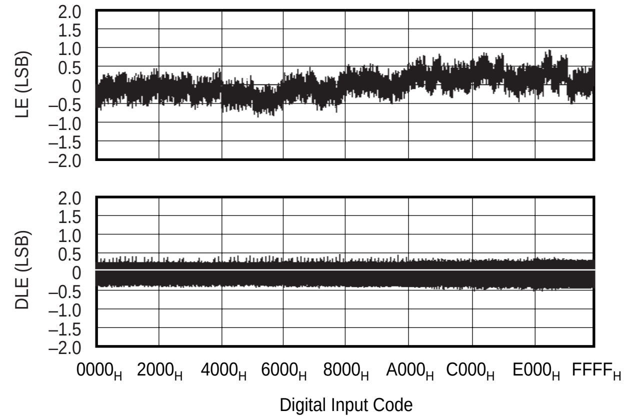
At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.

+25°C

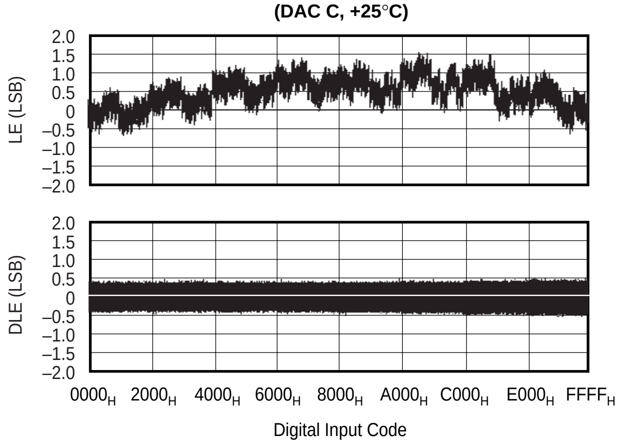
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +25°C)



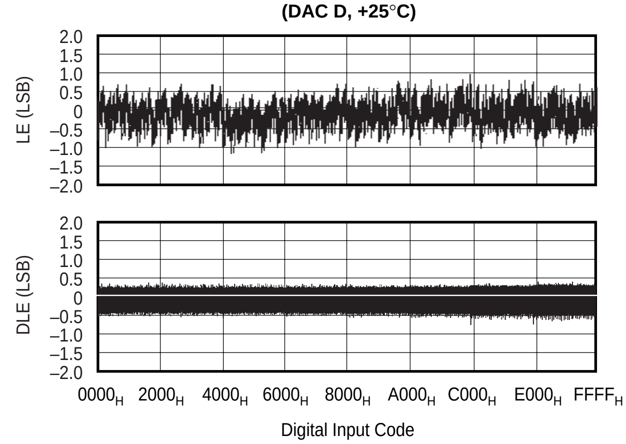
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +25°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +25°C)

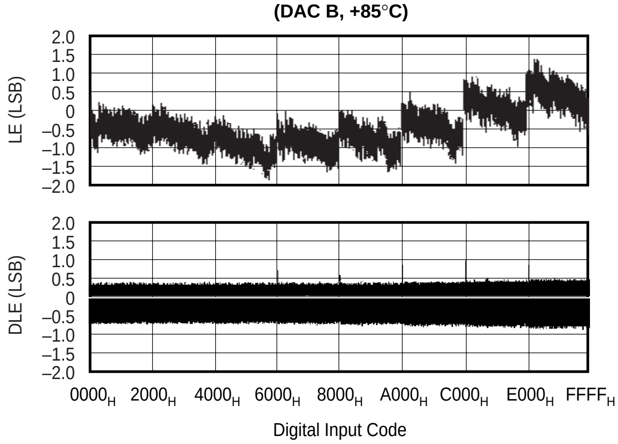


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +25°C)

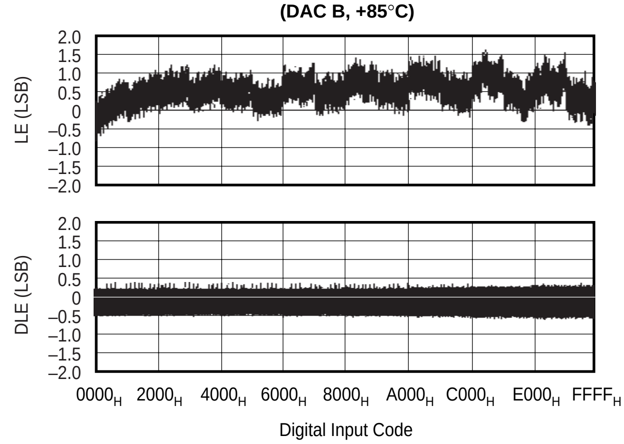


+85°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +85°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +85°C)

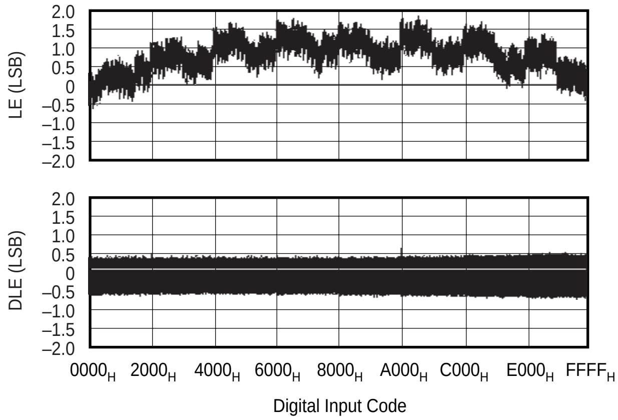


TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (CONT)

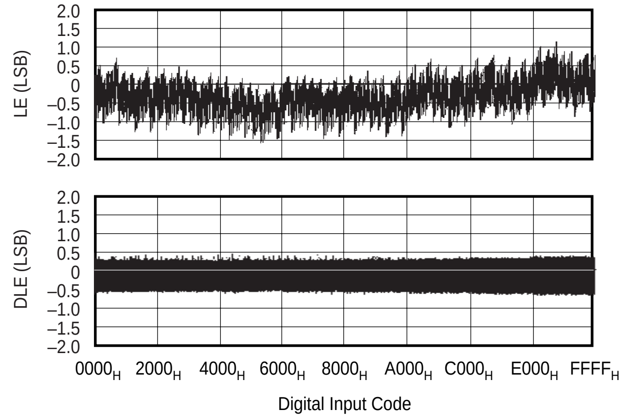
At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.

+85°C (cont)

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +85°C)

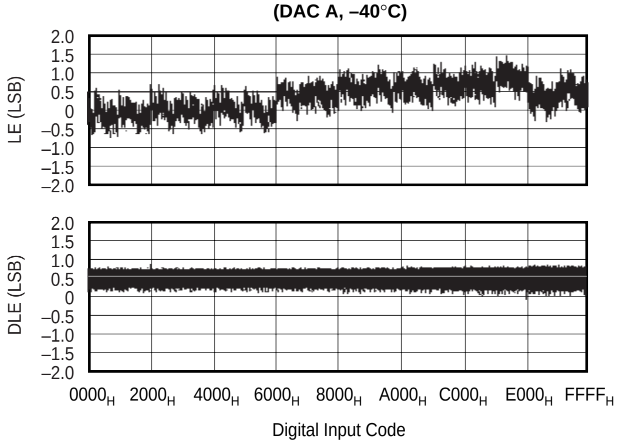


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +85°C)

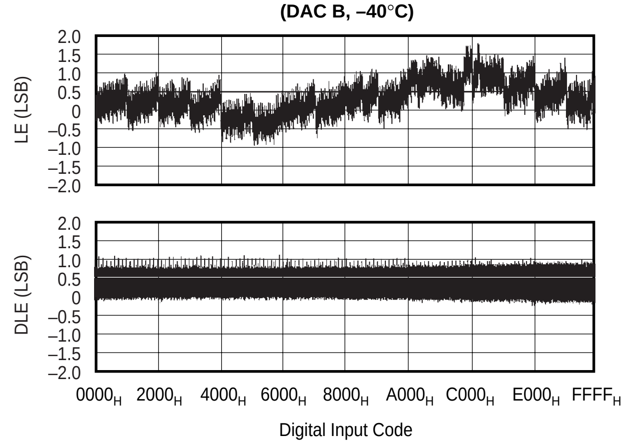


–40°C

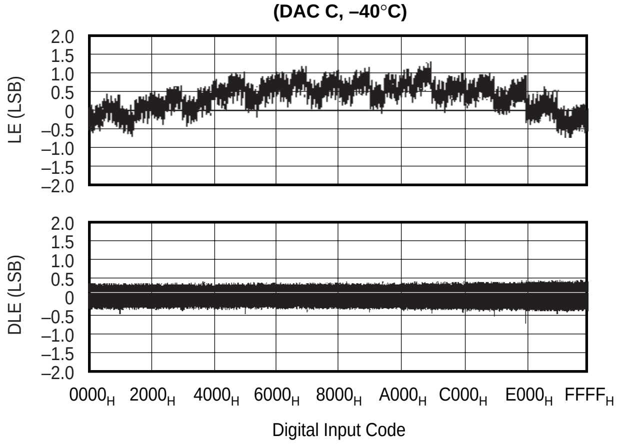
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, –40°C)



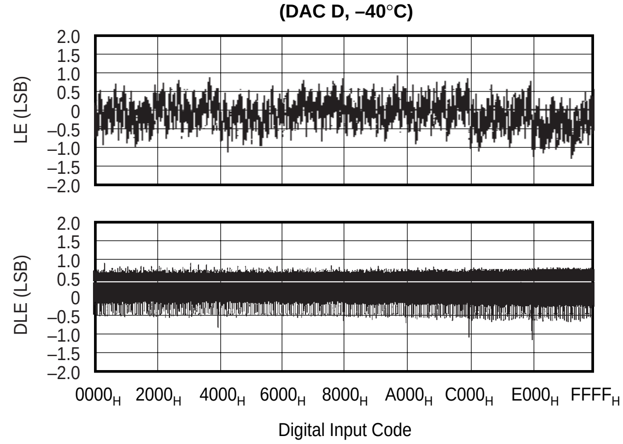
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, –40°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, –40°C)



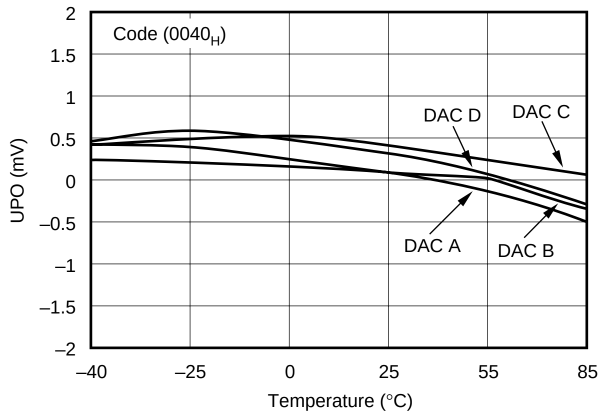
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, –40°C)



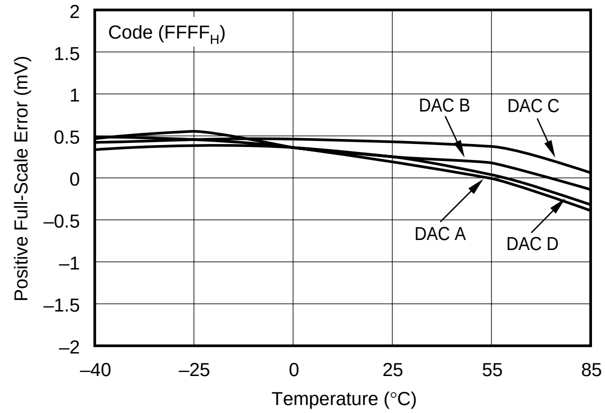
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (CONT)

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.

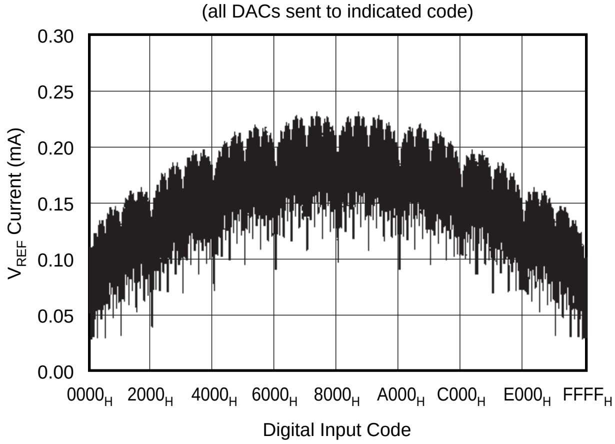
ZERO-SCALE ERROR vs TEMPERATURE



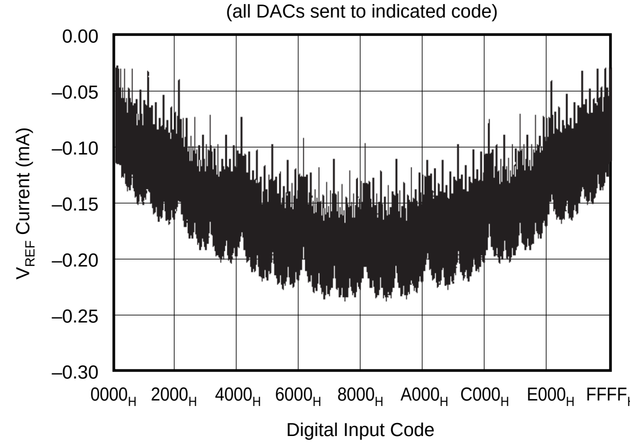
FULL-SCALE ERROR vs TEMPERATURE



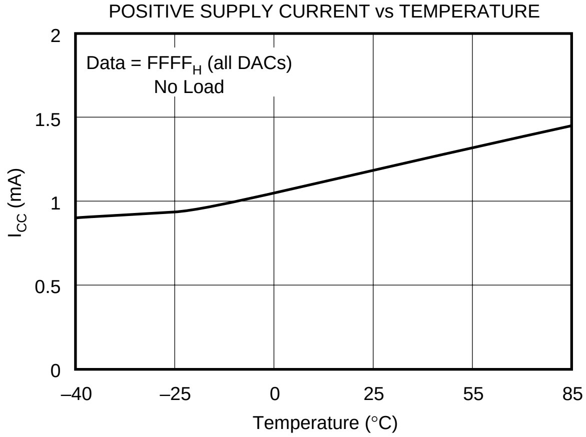
V_{REFH} CURRENT vs CODE
(all DACs sent to indicated code)



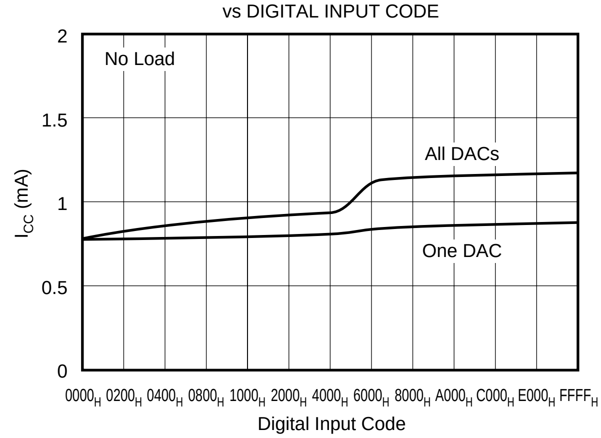
V_{REFL} CURRENT vs CODE
(all DACs sent to indicated code)



POSITIVE SUPPLY CURRENT vs TEMPERATURE



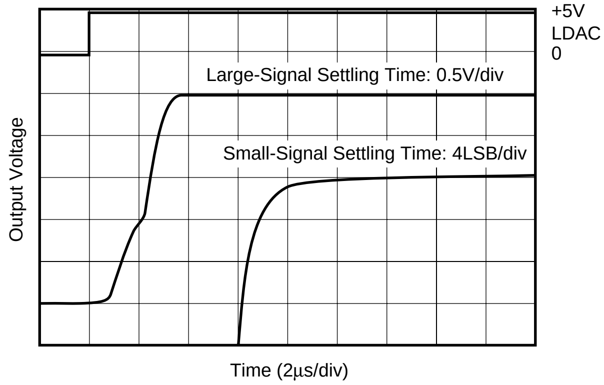
POSITIVE SUPPLY CURRENT
vs DIGITAL INPUT CODE



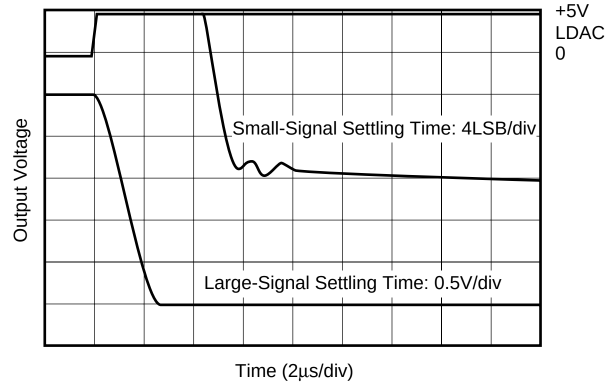
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (CONT)

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.

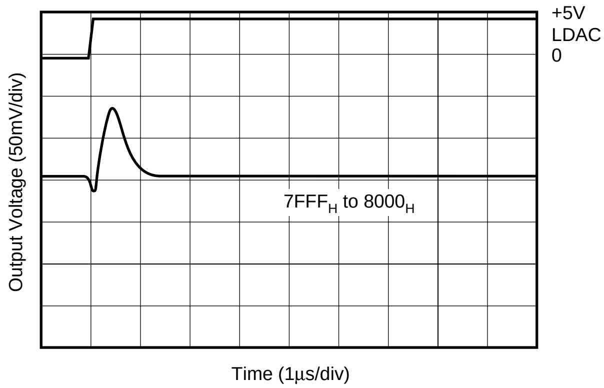
OUTPUT VOLTAGE vs SETTLING TIME
(0V to +2.5V)



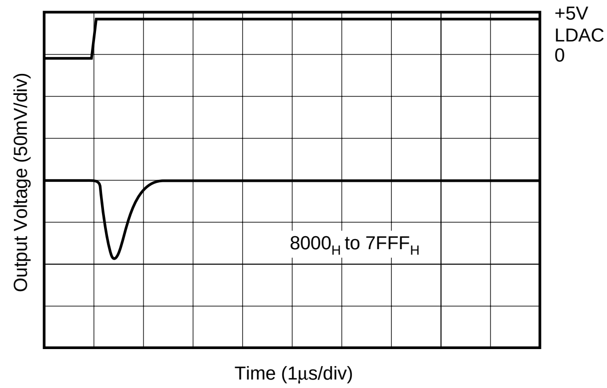
OUTPUT VOLTAGE vs SETTLING TIME
(+2.5V to 2mV)



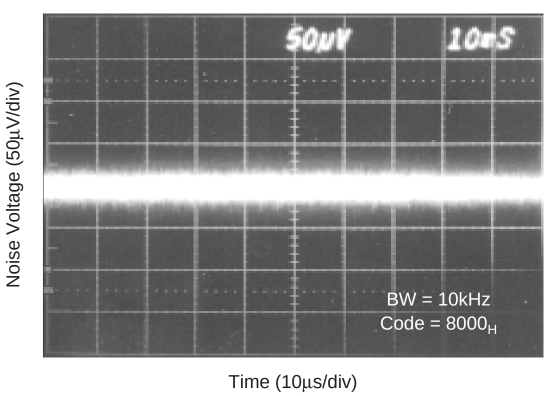
OUTPUT VOLTAGE
vs MIDSCALE GLITCH PERFORMANCE



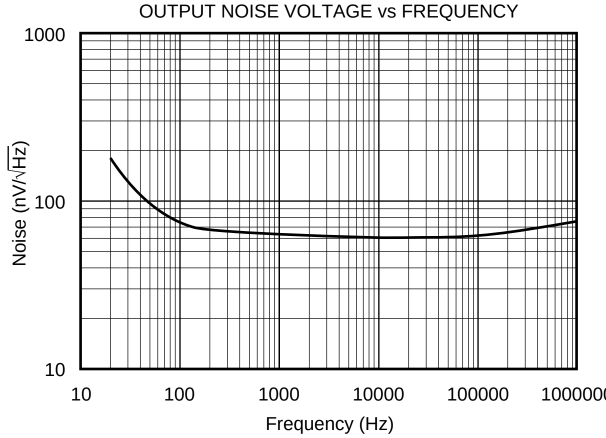
OUTPUT VOLTAGE
vs MIDSCALE GLITCH PERFORMANCE



BROADBAND NOISE

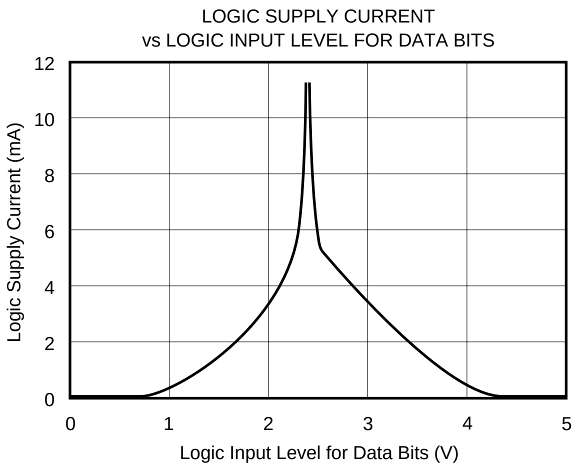


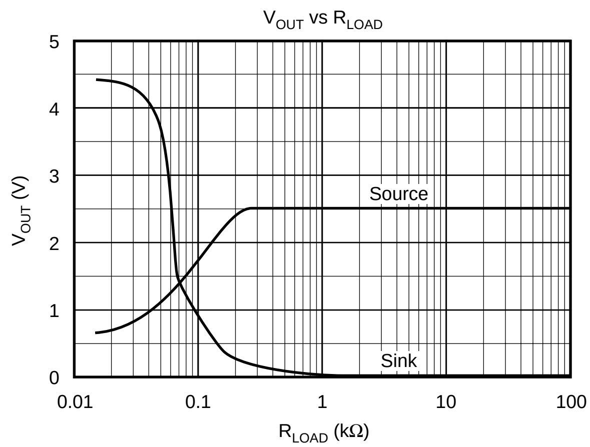
OUTPUT NOISE VOLTAGE vs FREQUENCY



TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (CONT)

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.



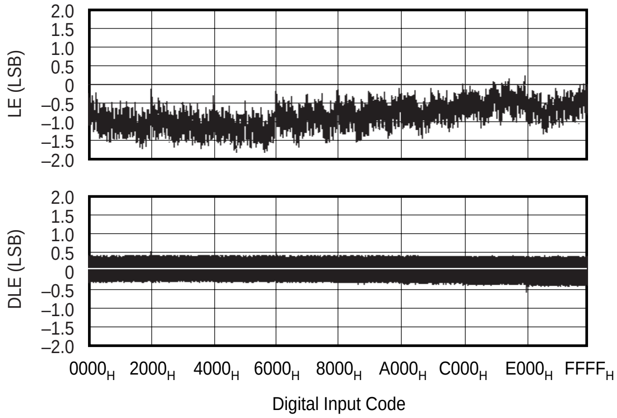


TYPICAL PERFORMANCE CURVES: V_{SS} = –5V

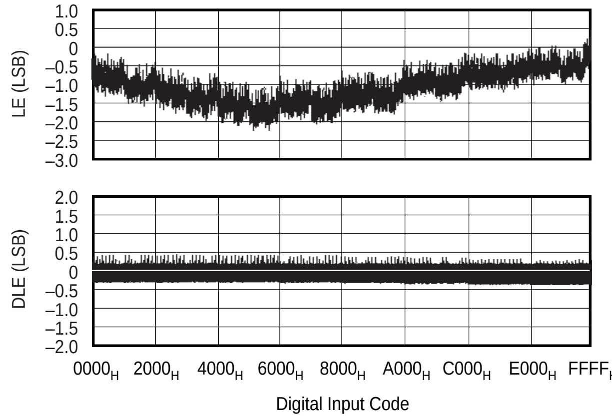
At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, representative unit, unless otherwise specified.

+25°C

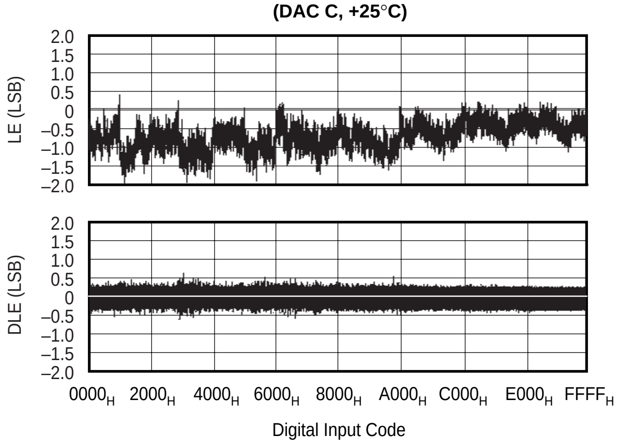
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +25°C)



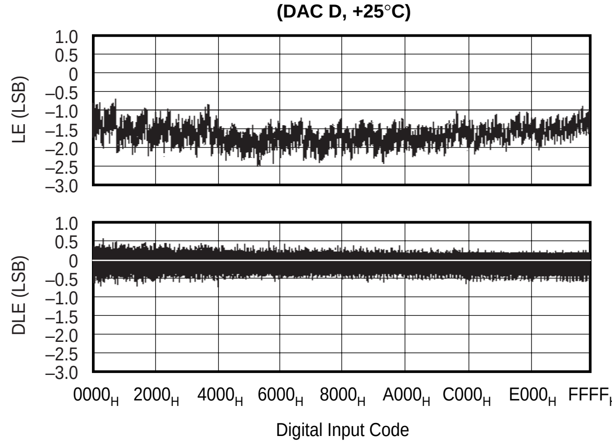
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +25°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +25°C)

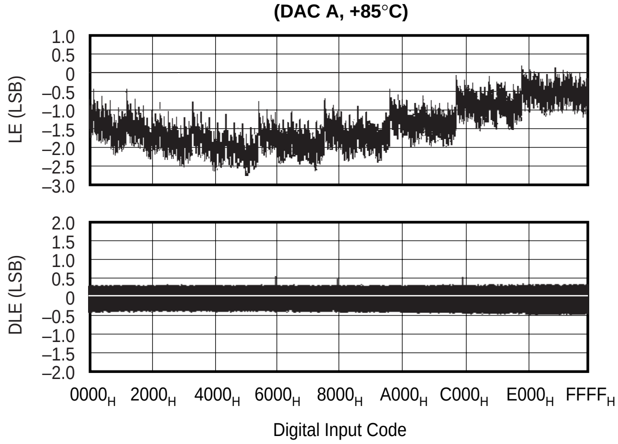


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +25°C)

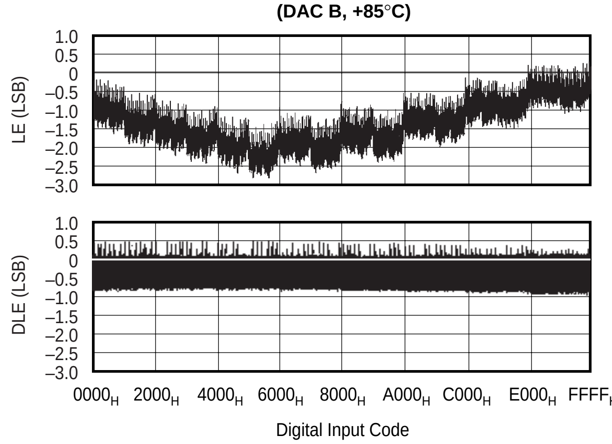


+85°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +85°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +85°C)

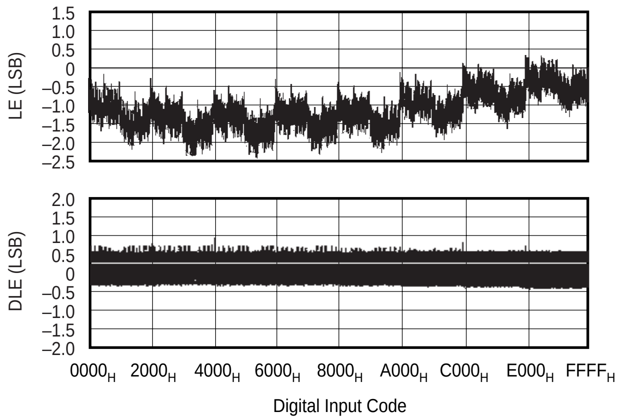


TYPICAL PERFORMANCE CURVES: V_{SS} = –5V (CONT)

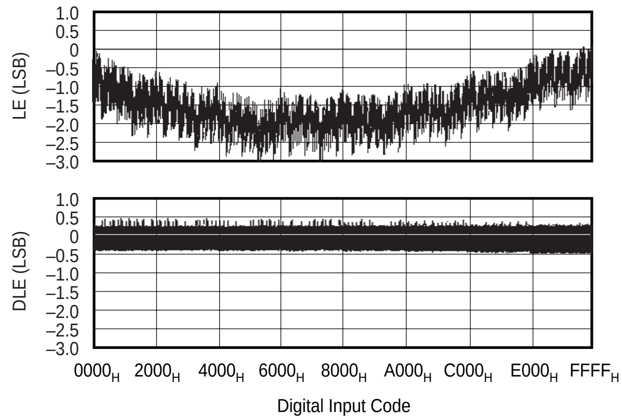
At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, representative unit, unless otherwise specified.

+85°C (cont)

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +85°C)

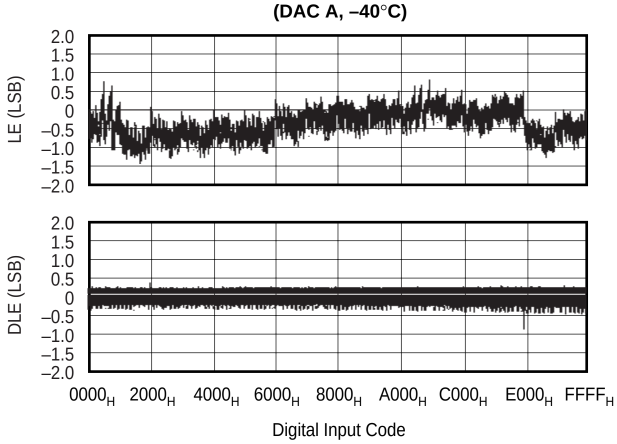


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +85°C)

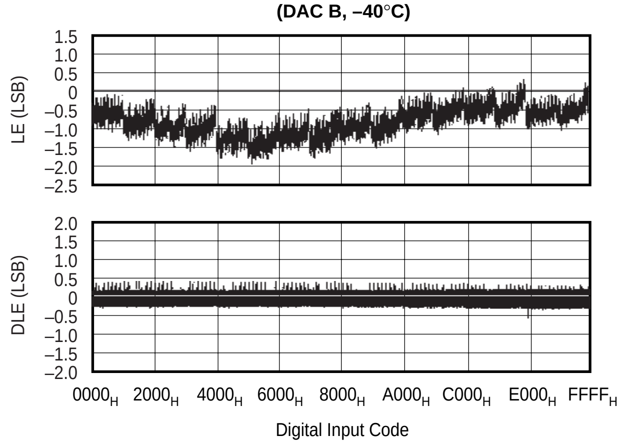


–40°C

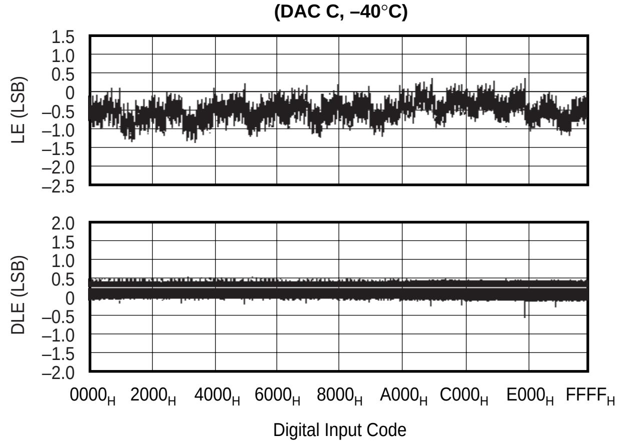
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, –40°C)



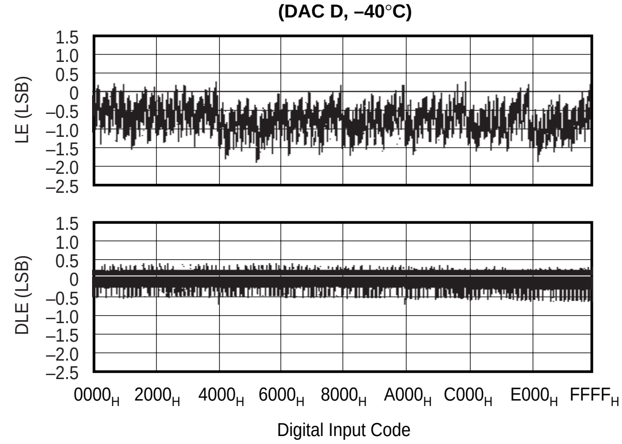
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, –40°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, –40°C)

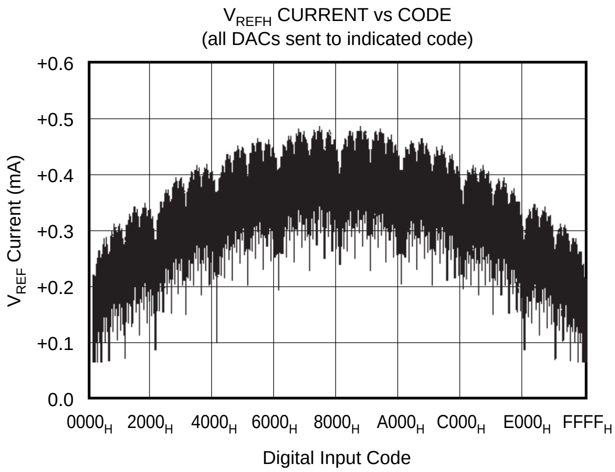


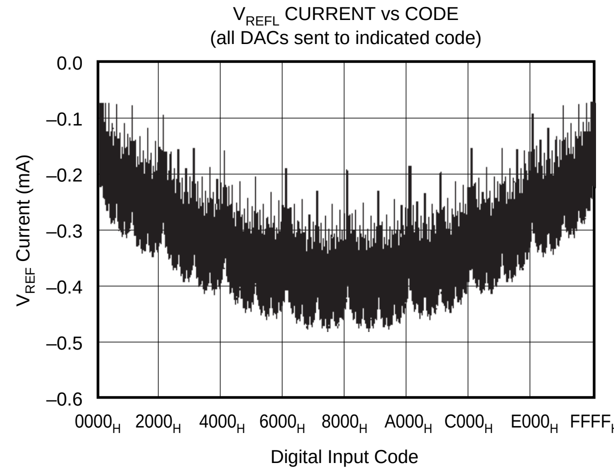
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, –40°C)

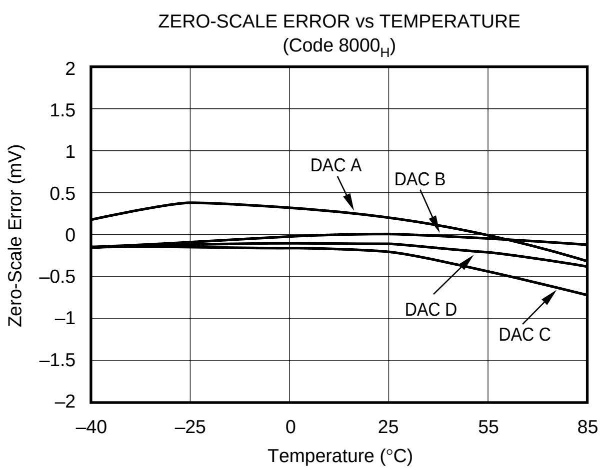


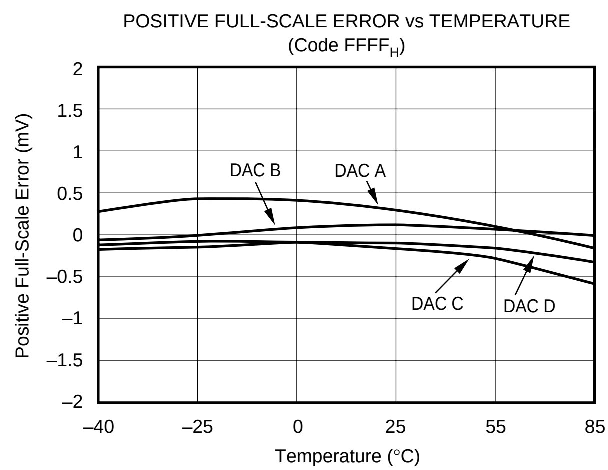
TYPICAL PERFORMANCE CURVES: V_{SS} = –5V (CONT)

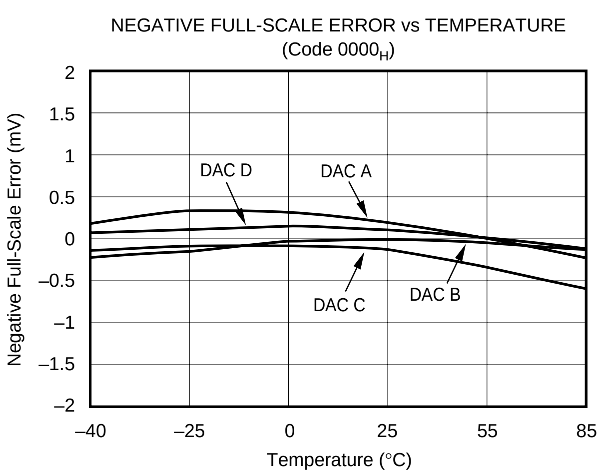
At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, representative unit, unless otherwise specified.

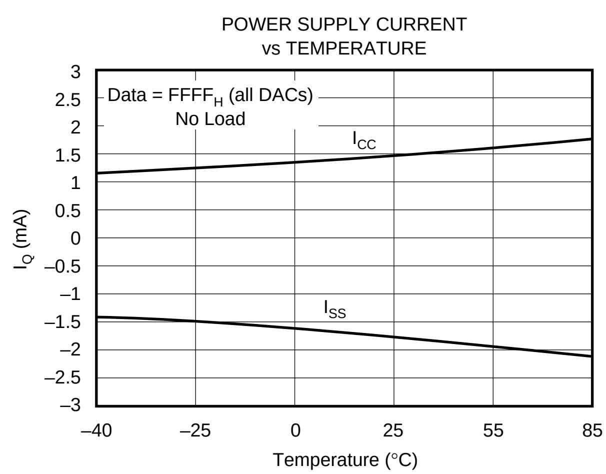






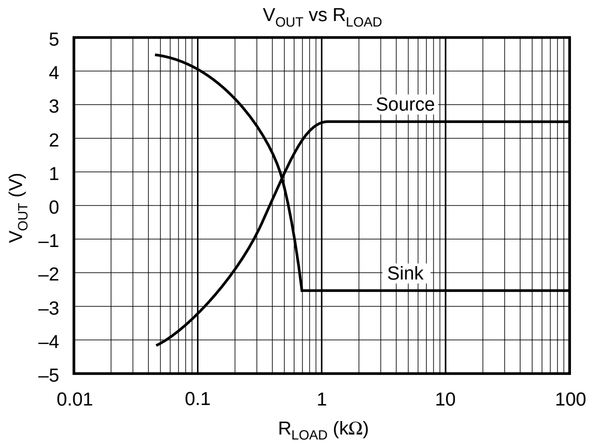


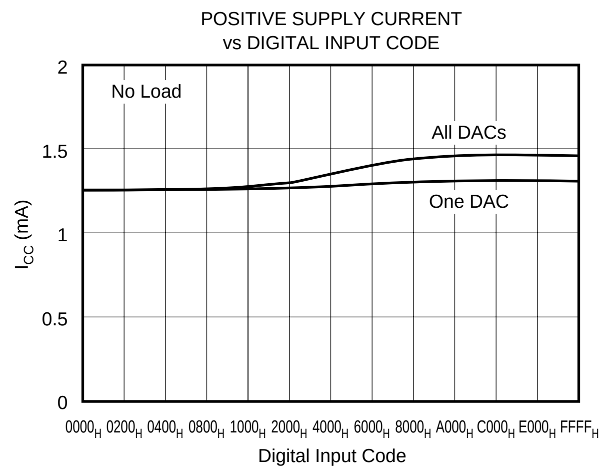


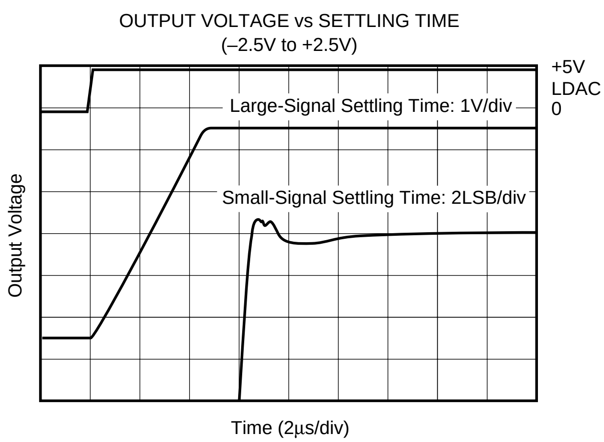


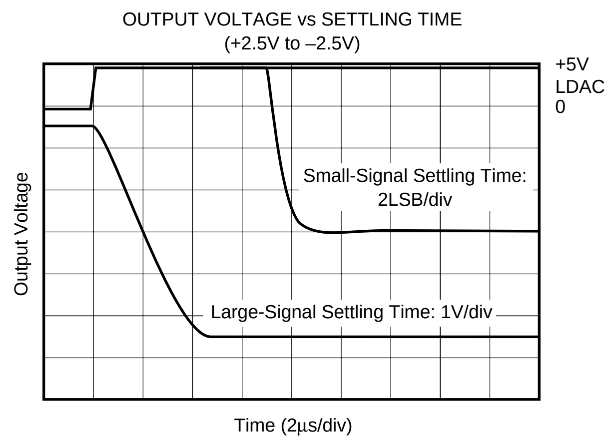
TYPICAL PERFORMANCE CURVES: V_{SS} = –5V (CONT)

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, representative unit, unless otherwise specified.









THEORY OF OPERATION

The DAC7644 is a quad voltage output, 16-bit digital-to-analog converter (DAC). The architecture is an R-2R ladder configuration with the three MSB's segmented followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network, segmented MSBs and output op amp (see Figure 1). The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by the external voltage references ($V_{REF}L$ and $V_{REF}H$, respectively). The digital input is a 16-bit parallel word and the DAC input registers offer a readback capability. The converters can be powered from either a single +5V supply or a dual ±5V supply. The device offers a reset function which immediately sets all DAC output voltages and DAC registers to mid-scale code 8000_H or to zero-scale, code 0000_H. See Figures 2 and 3 for the basic operation of the DAC7644.

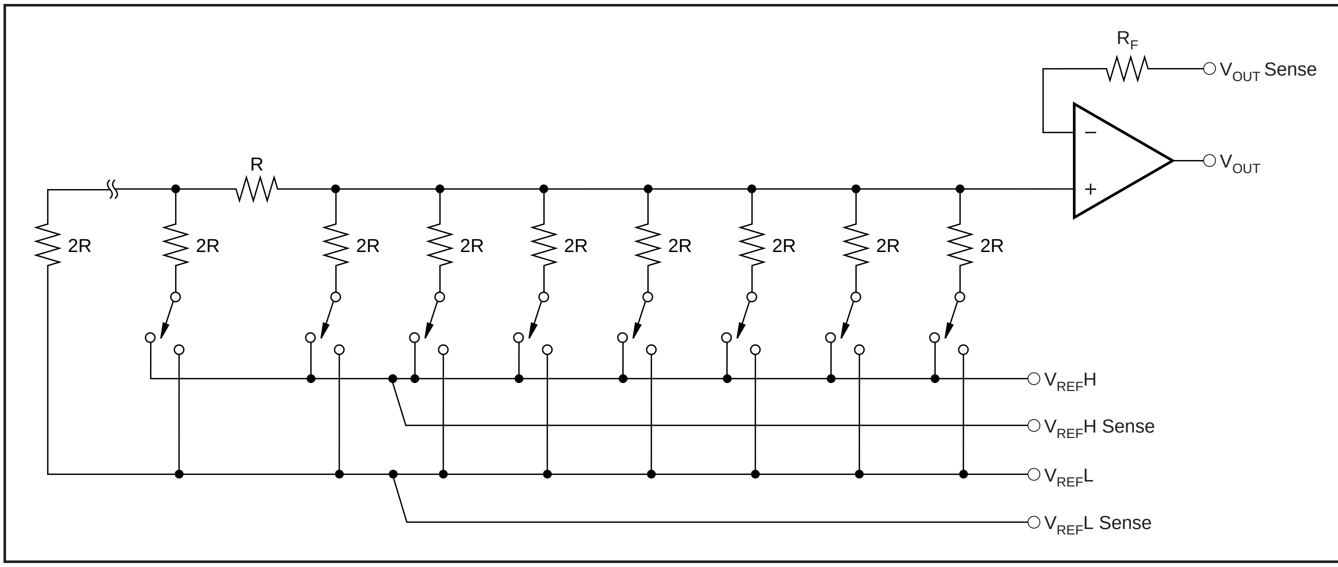


FIGURE 1. DAC7644 Architecture.

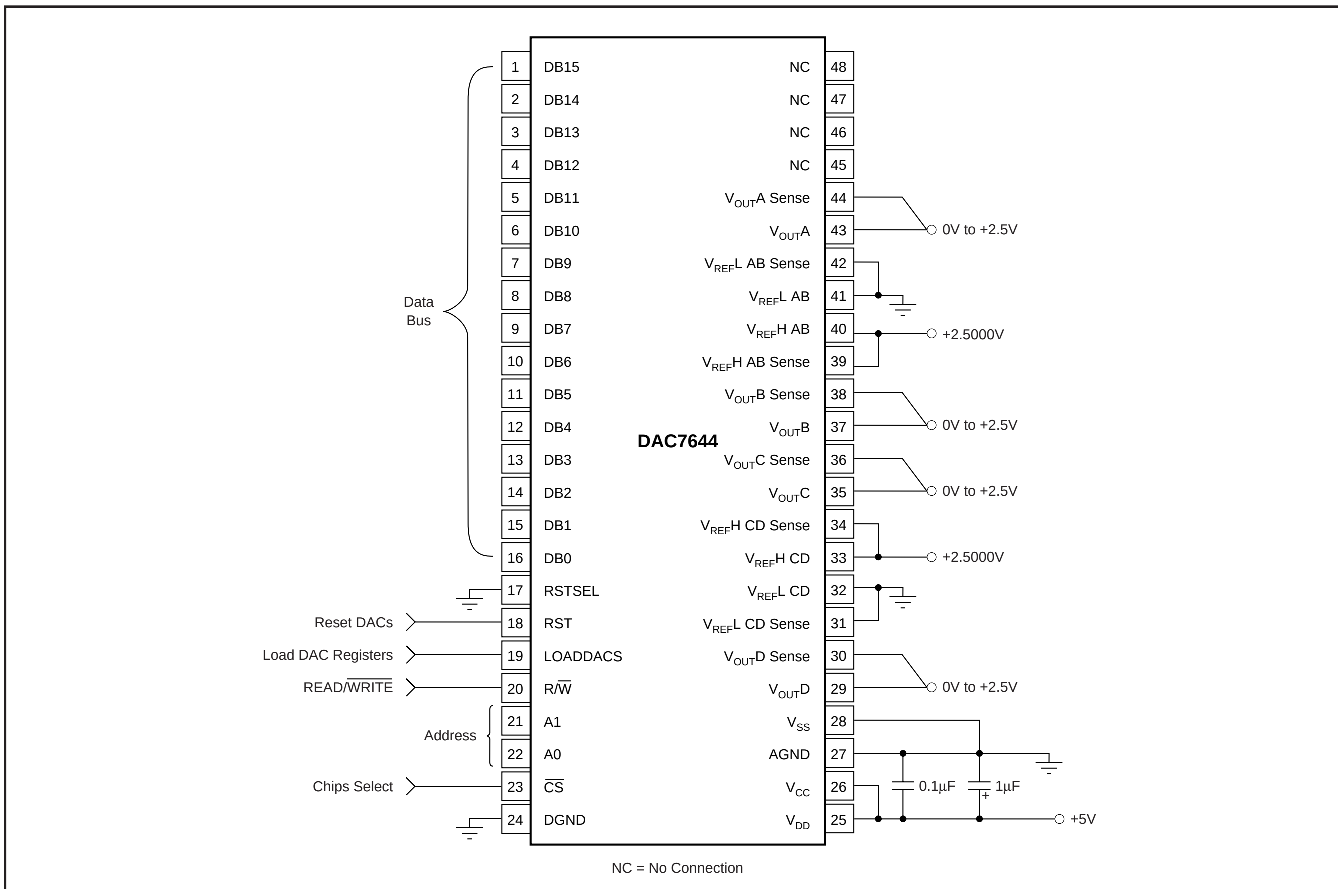


FIGURE 2. Basic Single-Supply Operation of the DAC7644.

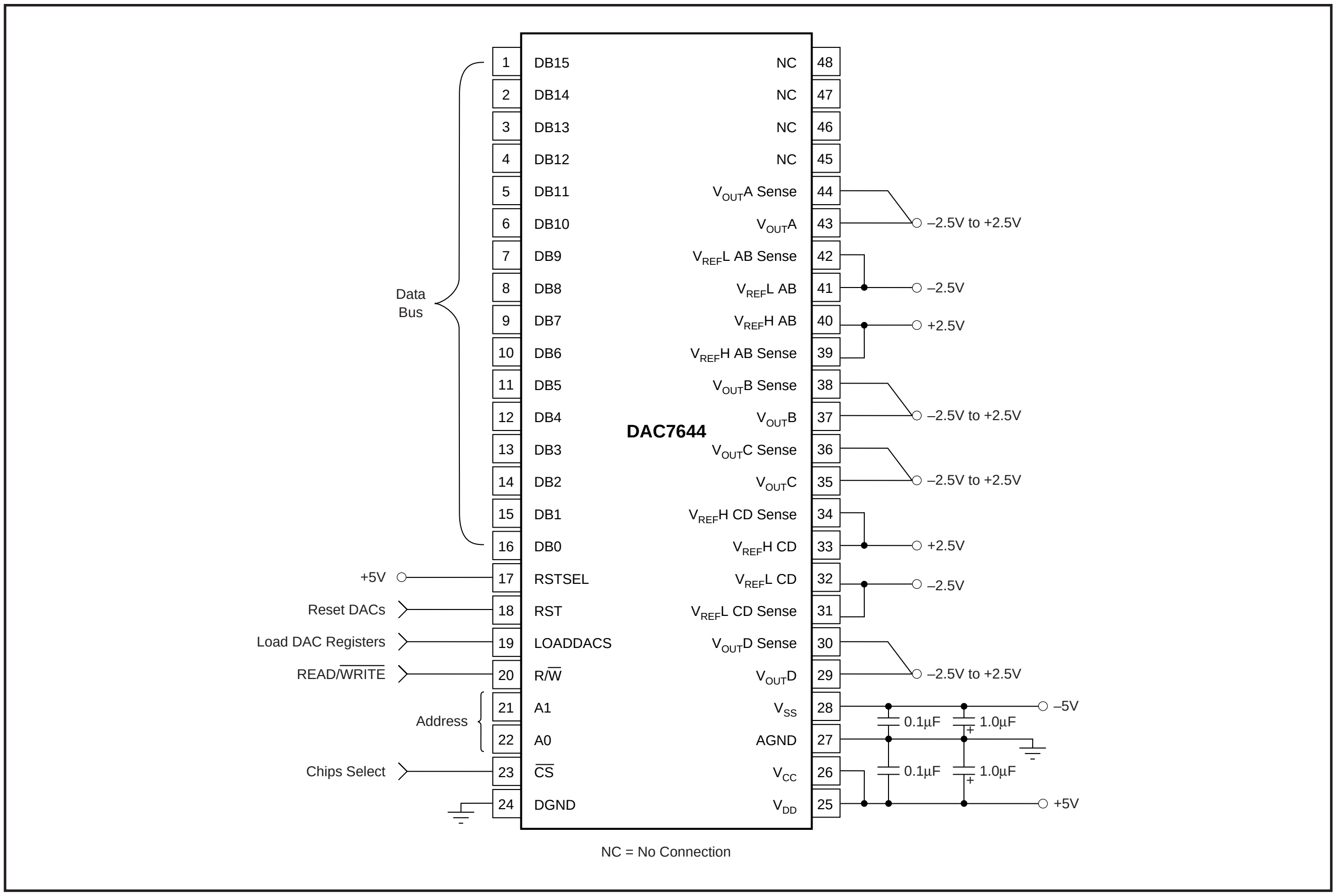


FIGURE 3. Basic Dual-Supply Operation of the DAC7644.

ANALOG OUTPUTS

When V_{SS} = –5V (dual supply operation), the output amplifier can swing to within 2.25V of the supply rails, guaranteed over the –40°C to +85°C temperature range. With V_{SS} = 0V (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to ground. Care must also be taken when measuring the zero-scale error when V_{SS} = 0V. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000_H, 0001_H, 0002_H, etc.) if the output amplifier has a negative offset. At the negative limit of –2mV, the first specified output starts at code 0040_H.

Due to the high accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 2.5V full-scale range has a 1LSB value of 38µV. With a load current of 1mA, series wiring and connector resistance (see Figure 4) of only 40mΩ (R_{W2}) will cause a voltage drop of 40µV. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 1mA load, a 10 milli-inch wide printed circuit conductor 600 milli-inches long will result in a voltage drop of 30µV.

The DAC7644 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (see Figure 4), thus ensuring an accurate output voltage.

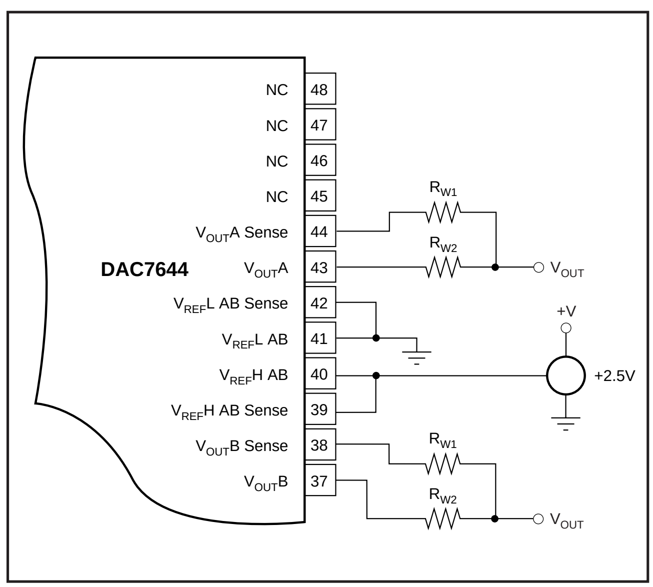


FIGURE 4. Analog Output Closed-Loop Configuration (1/2 DAC7644). R_W represents wiring resistances.

REFERENCE INPUTS

The reference inputs, $V_{REF}L$ and $V_{REF}H$, can be any voltage between V_{SS} + 2.5V and V_{CC} – 2.5V provided that $V_{REF}H$ is at least 1.25V greater than $V_{REF}L$. The minimum output of each DAC is equal to $V_{REF}L$ plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to $V_{REF}H$ plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of –4.75V to –5.25V. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the $V_{REF}H$ input and out of $V_{REF}L$ depends on the DAC output voltages and can vary from a few microamps to approximately 0.5mA. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. The DAC7644 features a reference drive and sense connection such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figures 5 through 12 show different reference configurations and the effect on the linearity and differential linearity.

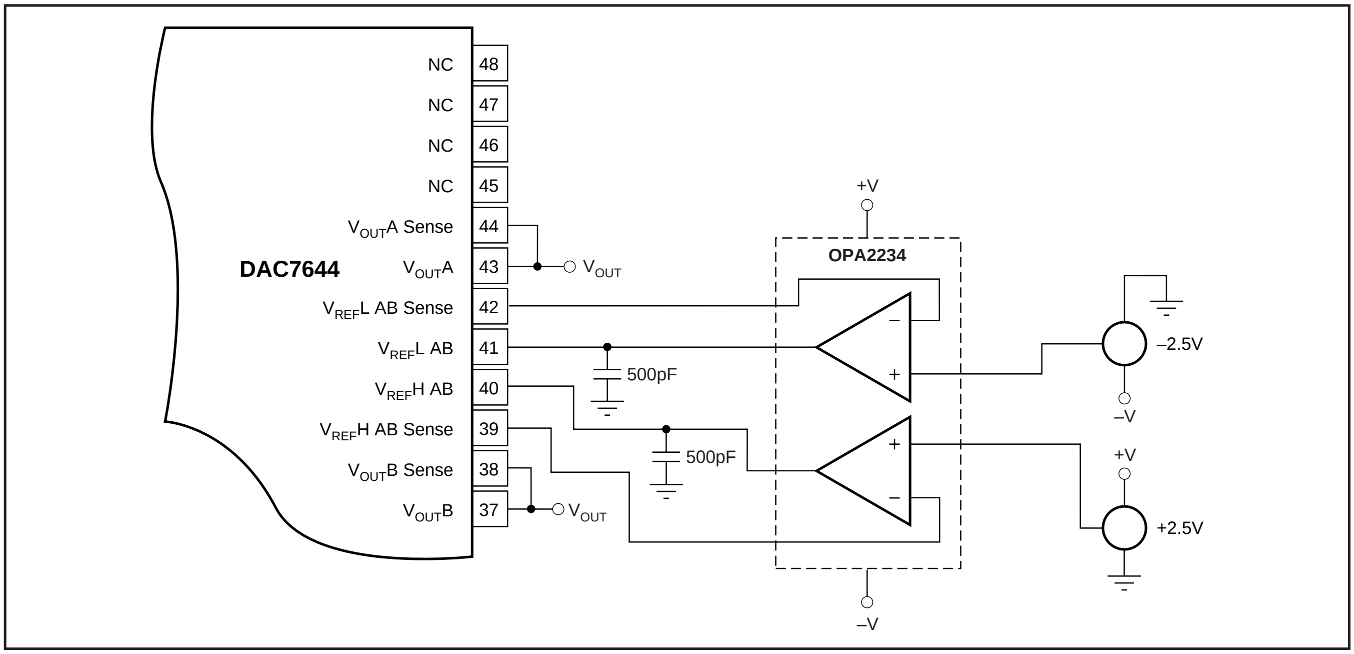


FIGURE 5. Dual Supply Configuration-Buffered References, used for Dual Supply Performance Curves (1/2 DAC7644).

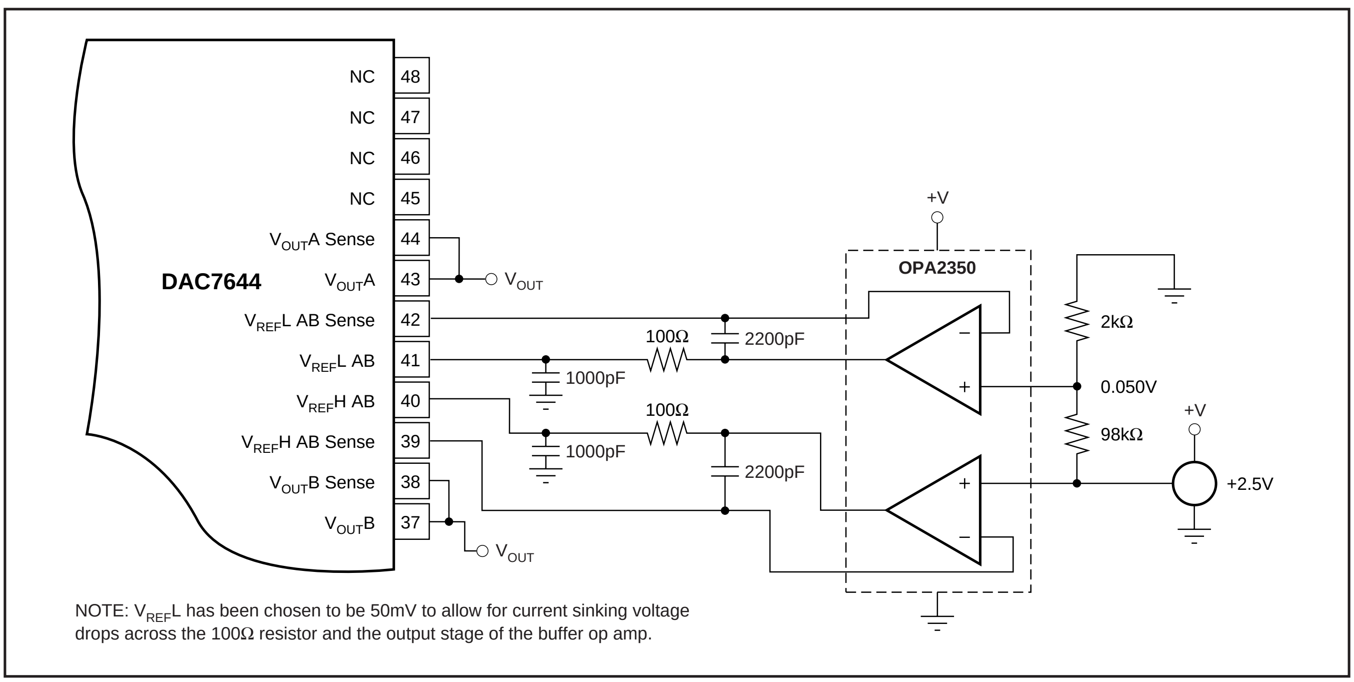


FIGURE 6. Single-Supply Buffered Reference with a Reference Low of 50mV (1/2 DAC7644).

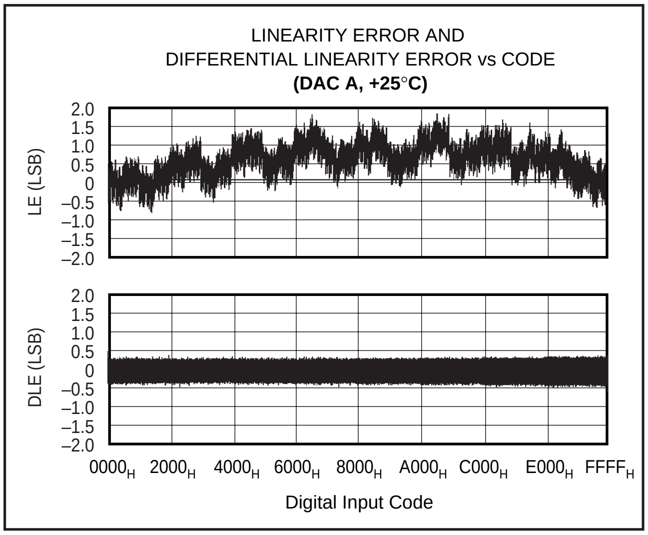


FIGURE 7. Integral Linearity and Differential Linearity Error Curves for Figure 6.

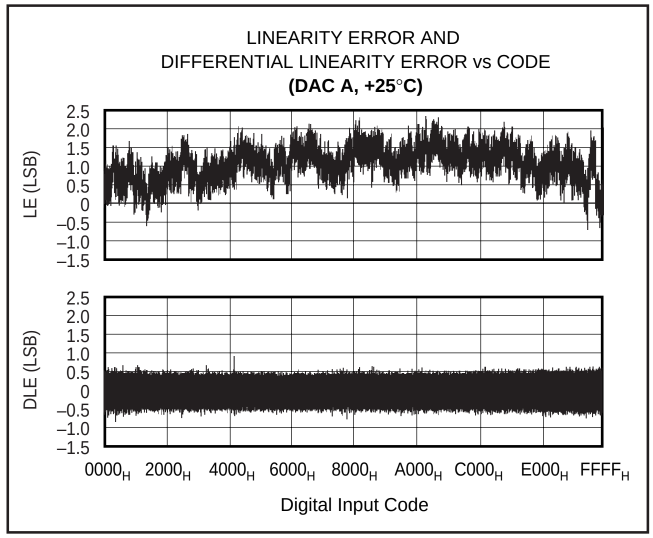


FIGURE 8. Integral Linearity and Differential Linearity Error Curves for Figure 9.

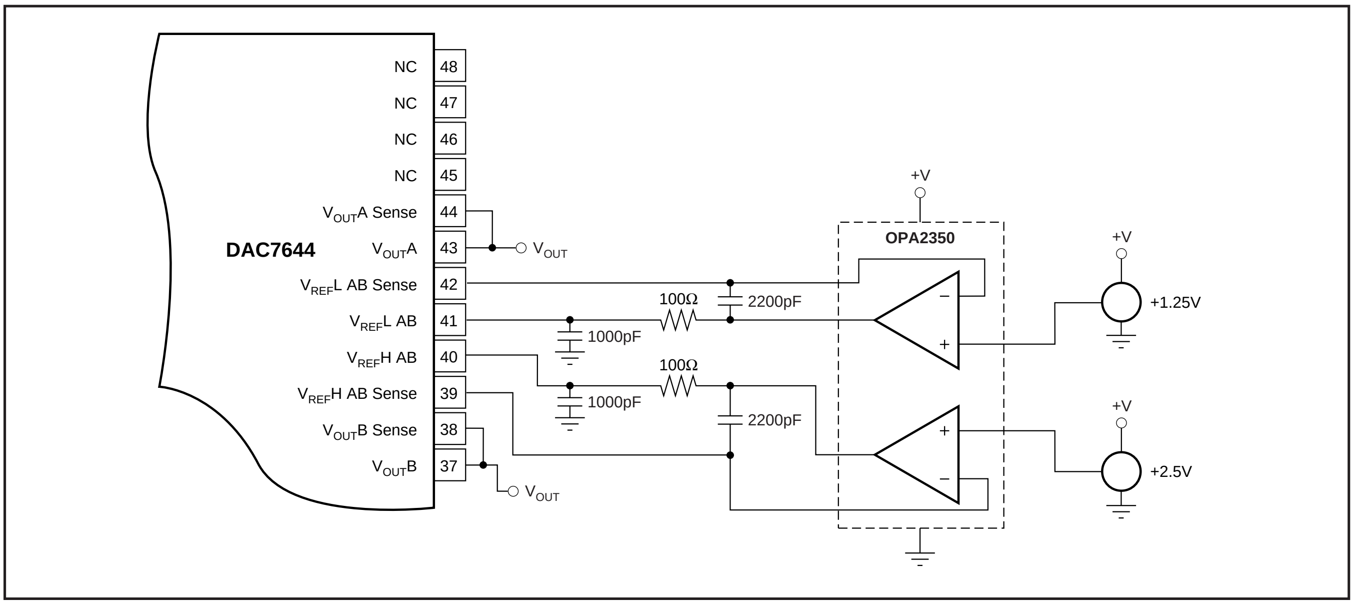


FIGURE 9. Single-Supply Buffered Reference with $V_{REF}L = +1.25V$ and $V_{REF}H = +2.5V$ (1/2 DAC7644).

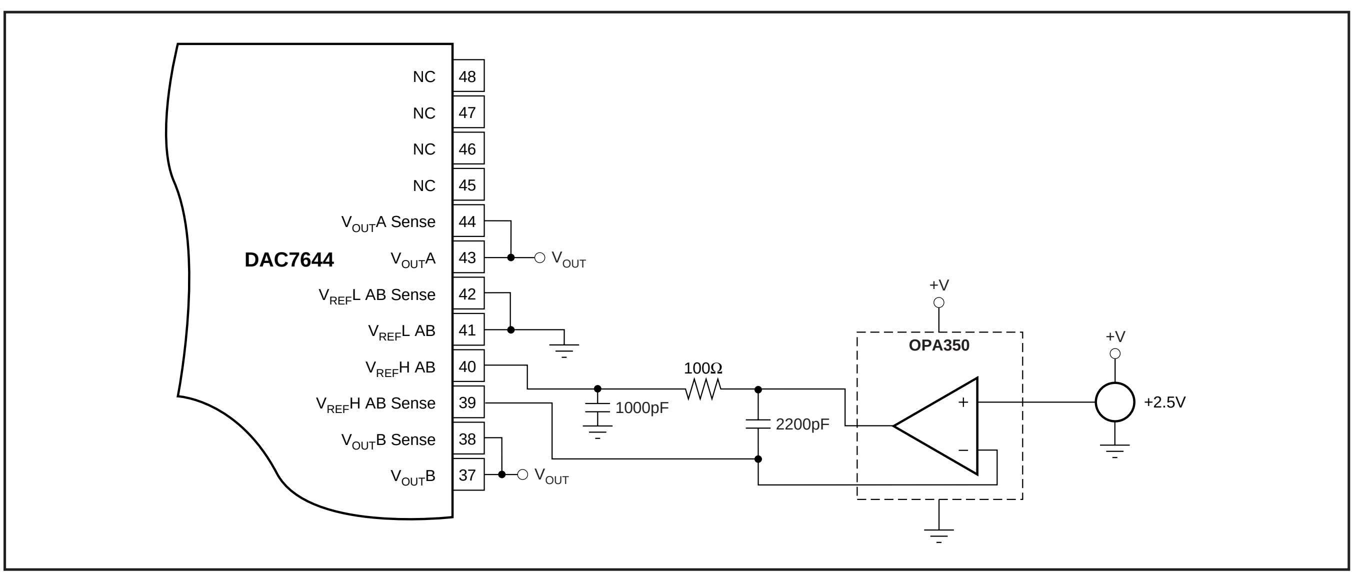


FIGURE 10. Single-Supply Buffered $V_{REF}H$ (1/2 DAC7644).

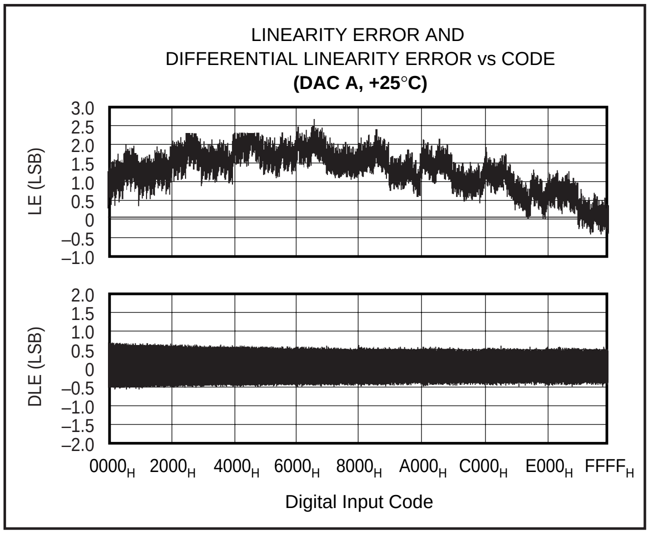


FIGURE 11. Linearity and Differential Linearity Error Curves for Figure 10.

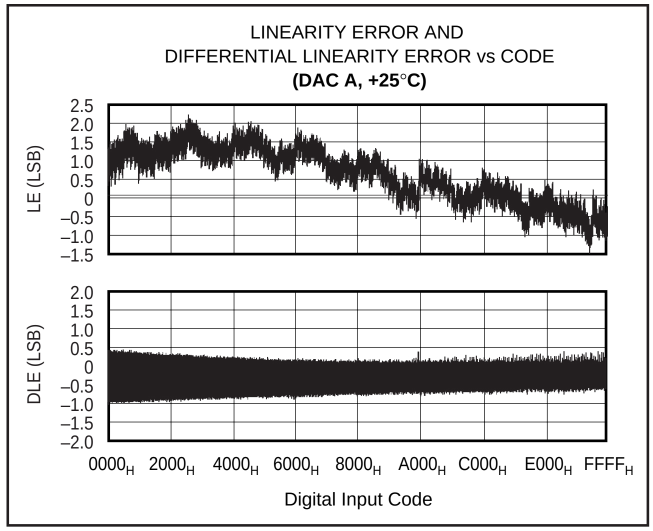


FIGURE 13. Linearity and Differential Linearity Error Curves for Figure 12.

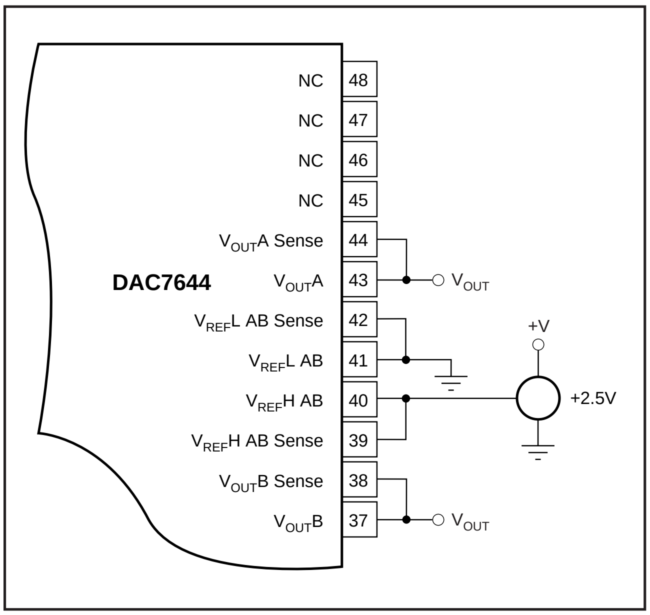


FIGURE 12. Low Cost Single-Supply Configuration.

DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7644. Note that each internal register is edge triggered and not level triggered. When the LOADDACS signal is transitioned to HIGH, the digital word currently in the register is latched. The first set of registers (the input registers) are triggered via the A0, A1, R/$\overline{\text{W}}$, and $\overline{\text{CS}}$ inputs. Only one of these registers is transparent at any given time.

The double-buffered architecture is designed mainly so each DAC input register can be written to at any time and then all DAC voltages updated simultaneously by the rising edge of LOADDACS. It also allows a DAC input register to be written to at any point and the DAC voltages to be synchronously changed via a trigger signal connected to LOADDACS.

A1	A0	R/$\overline{\text{W}}$	$\overline{\text{CS}}$	RST	RSTSEL	LOADDACS	INPUT REGISTER	DAC REGISTER	MODE	DAC
L	L	L	L	H	X	X	Write	Hold	Write Input	A
L	H	L	L	H	X	X	Write	Hold	Write Input	B
H	L	L	L	H	X	X	Write	Hold	Write Input	C
H	H	L	L	H	X	X	Write	Hold	Write Input	D
L	L	H	L	H	X	X	Read	Hold	Read Input	A
L	H	H	L	H	X	X	Read	Hold	Read Input	B
H	L	H	L	H	X	X	Read	Hold	Read Input	C
H	H	H	L	H	X	X	Read	Hold	Read Input	D
X	X	X	H	H	X	↑	Hold	Write	Update	All
X	X	X	H	H	X	H	Hold	Hold	Hold	All
X	X	X	X	↑	L	X		Reset to Zero	Reset to Zero	All
X	X	X	X	↑	H	X		Reset to Midscale	Reset to Midscale	All

TABLE I. DAC7644 Logic Truth Table.

DIGITAL TIMING

Figure 14 and Table II provide detailed timing for the digital interface of the DAC7644.

DIGITAL INPUT CODING

The DAC7644 input data is in Straight Binary format. The output voltage is given by Equation 1.

$$V_{OUT} = V_{REF}L + \frac{\left(V_{REF}H - V_{REF}L\right) \bullet N}{65,536} \qquad (1)$$

where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

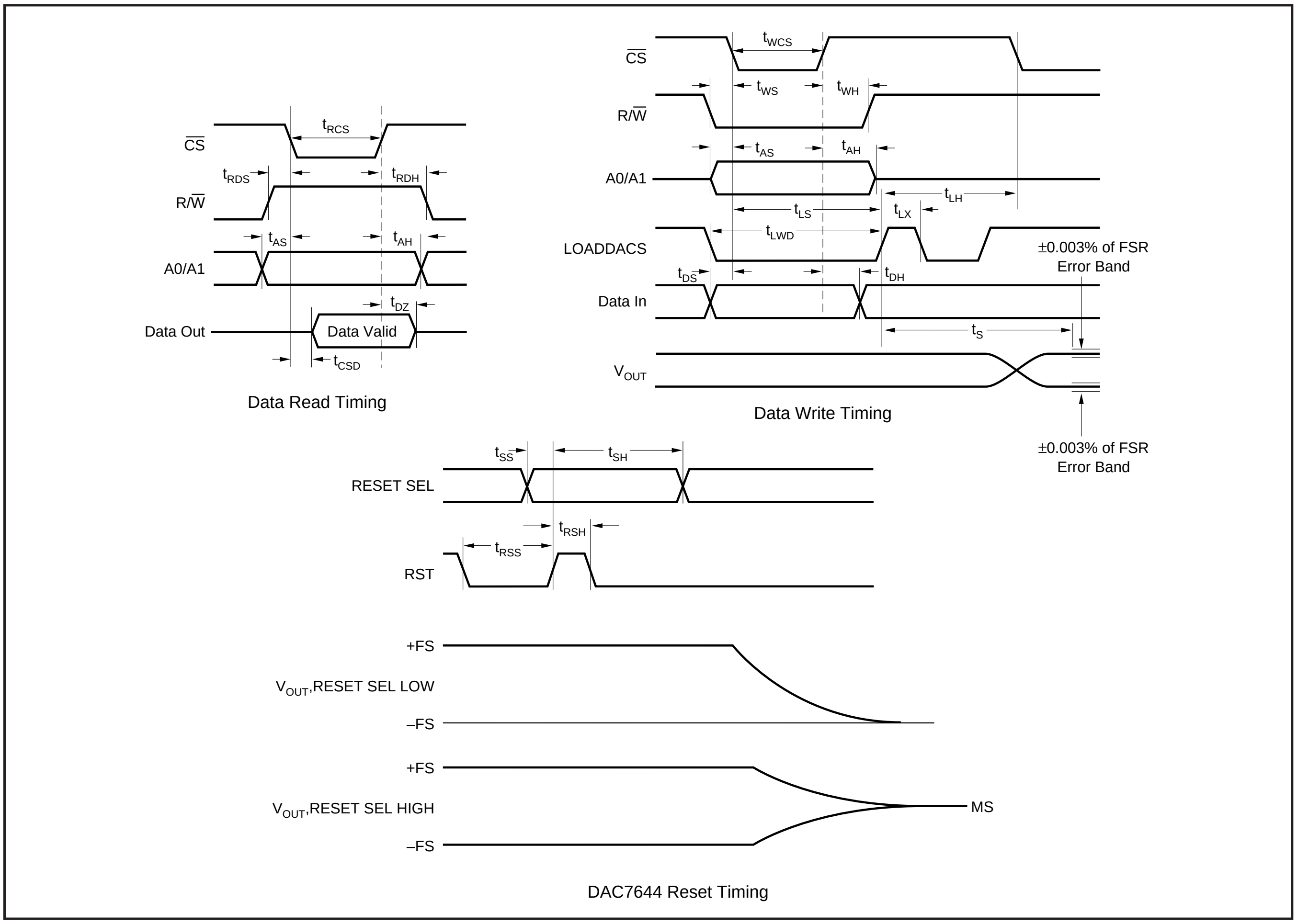


FIGURE 14. Digital Input and Output Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RCS}	$\overline{CS}$ LOW for Read	150			ns
t_{RDS}	R/$\overline{W}$ HIGH to $\overline{CS}$ LOW	10			ns
t_{RDH}	R/$\overline{W}$ HIGH after $\overline{CS}$ HIGH	10			ns
t_{DZ}	$\overline{CS}$ HIGH to Data Bus in High Impedance	10		100	ns
t_{CSD}	$\overline{CS}$ LOW to Data Bus Valid		100	150	ns
t_{WCS}	$\overline{CS}$ LOW for Write	40			ns
t_{WS}	R/$\overline{W}$ LOW to $\overline{CS}$ LOW	0			ns
t_{WH}	R/$\overline{W}$ LOW after $\overline{CS}$ HIGH	10			ns
t_{AS}	Address Valid to $\overline{CS}$ LOW	0			ns
t_{AH}	Address Valid after $\overline{CS}$ HIGH	10			ns
t_{LS}	$\overline{CS}$ LOW to LOADDACS HIGH	30			ns
t_{LH}	$\overline{CS}$ LOW after LOADDACS HIGH	100			ns
t_{LX}	LOADDACS HIGH	100			ns
t_{DS}	Data Valid to $\overline{CS}$ LOW	0			ns
t_{DH}	Data Valid after $\overline{CS}$ HIGH	10			ns
t_{LWD}	LOADDACS LOW	100			ns
t_{SS}	RSTSEL Valid Before RESET HIGH	0			ns
t_{SH}	RSTSEL Valid After RESET HIGH	200			ns
t_{RSS}	RESET LOW Before RESET HIGH	10			ns
t_{RSH}	RESET LOW After RESET HIGH	10			ns
t_S	Settling Time			10	µs

TABLE II. Timing Specifications (T_A = –40°C to +85°C).

DIGITALLY-PROGRAMMABLE CURRENT SOURCE

The DAC7644 offers a unique set of features that allows a wide range of flexibility in designing applications circuits such as programmable current sources. The DAC7644 offers both a differential reference input as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows transistor to be placed within the loop to implement a digitally-programmable, uni-directional current source. The availability of a differential reference also allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

$$I_{OUT} = \left(\left(\frac{V_{REF}H - V_{REF}L}{R_{SENSE}}\right) \cdot \left(\frac{N\ Value}{65,536}\right)\right) + \left(V_{REF}L / R_{SENSE}\right) \quad (2)$$

Figure 15 shows a DAC7644 in a 4mA to 20mA current output configuration. The output current can be determined by Equation 3:

$$I_{OUT} = \left(\left(\frac{2.5V - 0.5V}{125\Omega}\right) \cdot \left(\frac{N\ Value}{65,536}\right)\right) + \left(\frac{0.5V}{125\Omega}\right) \quad (3)$$

At full-scale, the output current is 16mA plus the 4mA for the zero current. At zero scale the output current is the offset current of 4mA (0.5V/125Ω).

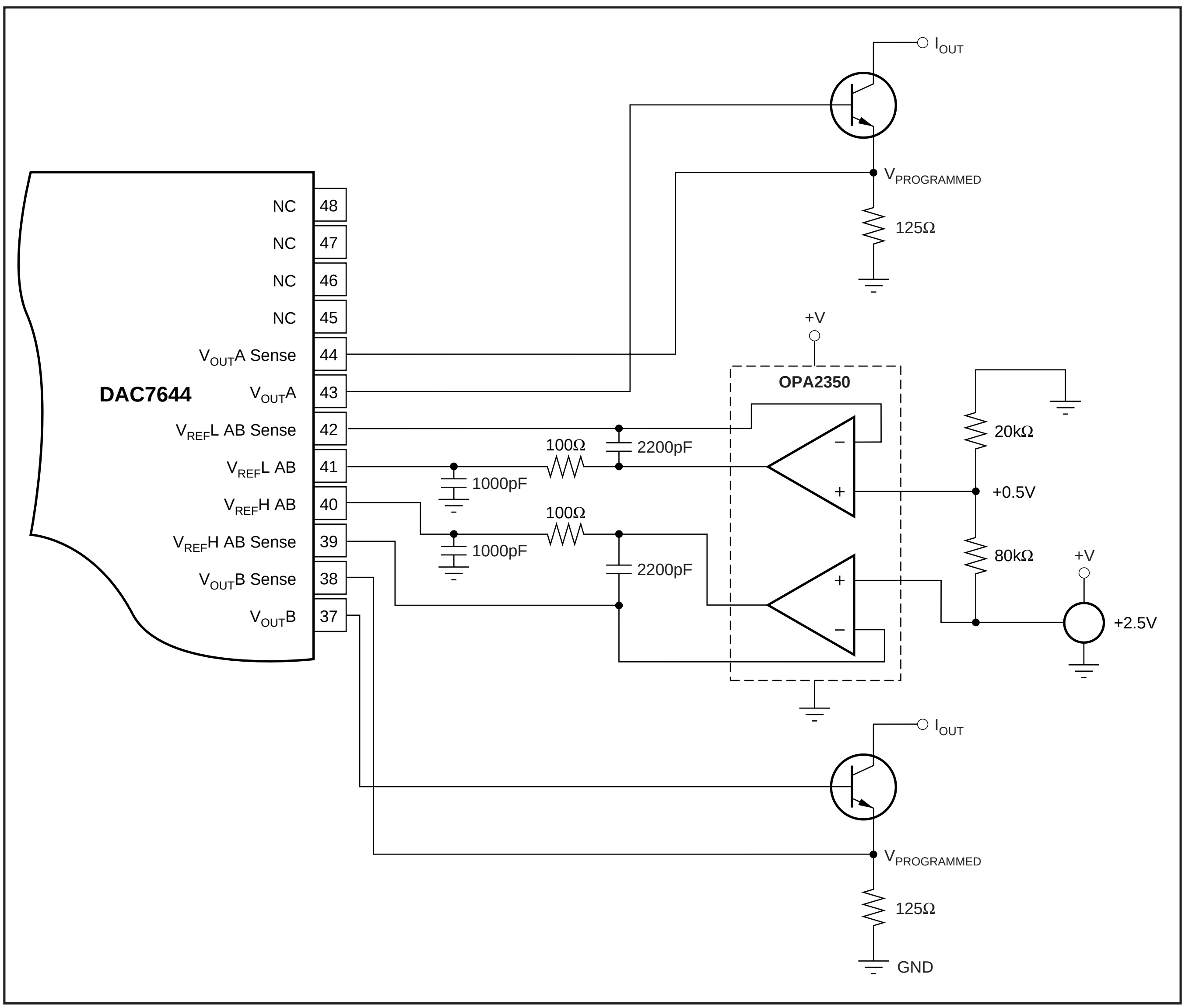


FIGURE 15. 4-to-20mA Digitally Controlled Current Source (1/2 DAC7644).

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
DAC7644E	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7644E/1K	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7644E/1KG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7644EB	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7644EB/1K	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7644EB/1KG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7644EBG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7644EG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

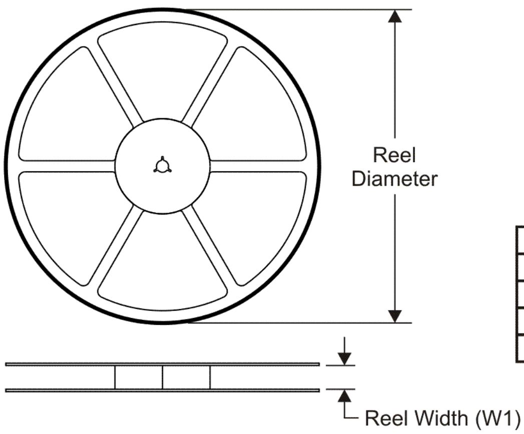
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

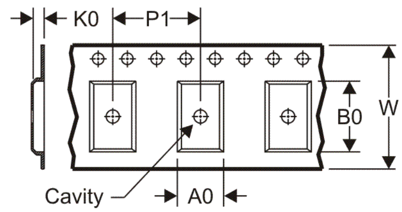
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

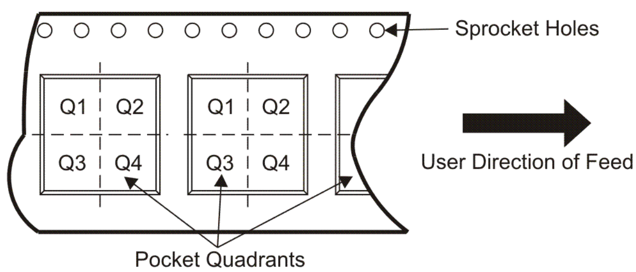


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

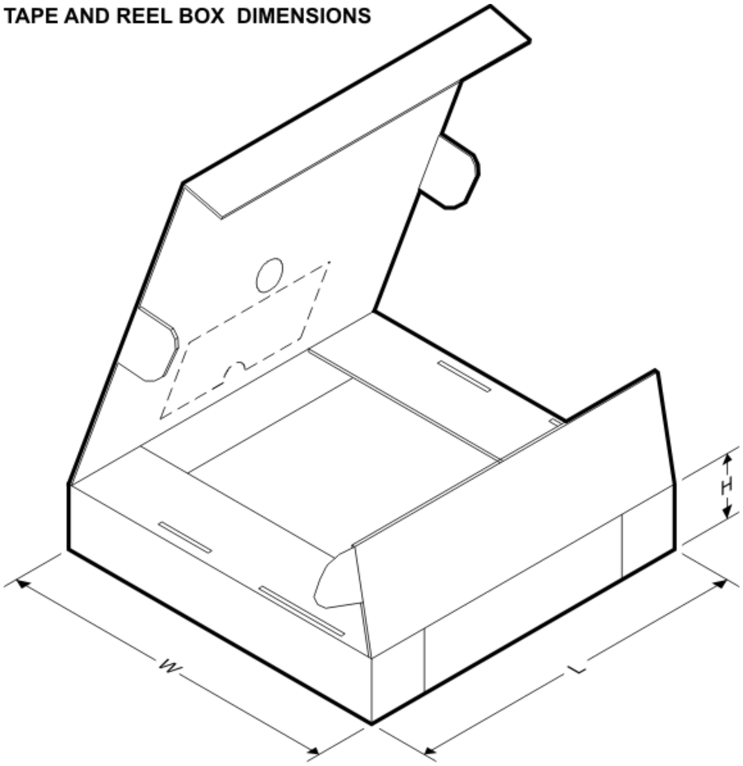
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7644E/1K	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
DAC7644EB/1K	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7644E/1K	SSOP	DL	48	1000	346.0	346.0	49.0
DAC7644EB/1K	SSOP	DL	48	1000	346.0	346.0	49.0

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
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Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
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