

74HC132

Quad 2-Input NAND Gate with Schmitt-Trigger Inputs

High-Performance Silicon-Gate CMOS

The 74HC132 is identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

The HC132 can be used to enhance noise immunity or to square up slowly changing waveforms.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements as Defined by JEDEC Standard No. 7A
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- These are Pb-Free Devices

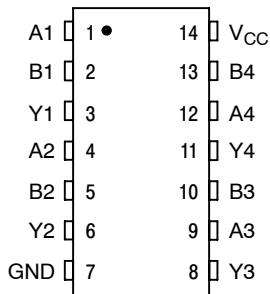


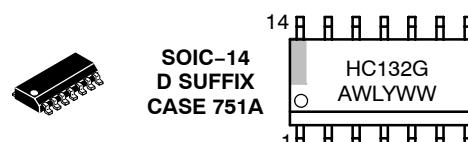
Figure 1. Pin Assignment



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MARKING DIAGRAMS



HC132 = Device Code
A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

FUNCTION TABLE

| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

74HC132

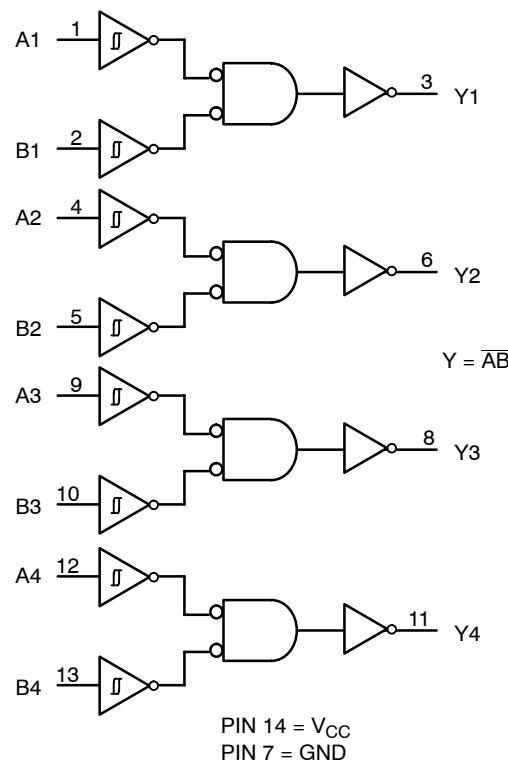


Figure 2. Logic Diagram

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|--------------|----------------------|-----------------------|
| 74HC132DR2G | SOIC-14 (Pb-Free) | 2500 / Tape & Reel |
| 74HC132DTR2G | TSSOP-14* | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---------------|--|---|------|
| V_{CC} | Positive DC Supply Voltage | – 0.5 to + 7.0 | V |
| V_{IN} | Digital Input Voltage | – 0.5 to + 7.0 | V |
| V_{OUT} | DC Output Voltage Output in 3-State High or Low State | – 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5 | V |
| I_{IK} | Input Diode Current | – 20 | mA |
| I_{OK} | Output Diode Current | ± 20 | mA |
| I_{OUT} | DC Output Current, per Pin | ± 25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 75 | mA |
| I_{GND} | DC Ground Current per Ground Pin | ± 75 | mA |
| T_{STG} | Storage Temperature Range | – 65 to + 150 | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T_J | Junction Temperature Under Bias | + 150 | °C |
| θ_{JA} | Thermal Resistance 14-SOIC 14-TSSOP | 125 170 | °C/W |
| P_D | Power Dissipation in Still Air at 85 °C SOIC TSSOP | 500 450 | mW |
| MSL | Moisture Sensitivity | Level 1 | |
| F_R | Flammability Rating Oxygen Index: 30% – 35% | UL 94 V-0 @ 0.125 in | |
| V_{ESD} | ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) | > 2000 > 200 | V |
| $I_{Latchup}$ | Latchup Performance Above V_{CC} and Below GND at 85 °C (Note 3) | ± 300 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to EIA/JESD78.
4. For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|--|------|----------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V_{IN}, V_{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | – 55 | + 125 | °C |
| t_r, t_f | Input Rise and Fall Time (Figure 3) | – | No Limit (Note 5) | ns |

5. When $V_{IN} \sim 0.5 V_{CC}$, $I_{CC} \gg$ quiescent current.

6. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} (V) | Guaranteed Limit | | | Unit |
|----------------------------|---|---|---------------------|--------------------|----------------------|----------------------|------|
| | | | | −55°C to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{T+max} | Maximum Positive-Going Input Threshold Voltage (Figure 5) | V _{OUT} = 0.1 V I _{OUT} ≤ 20 μA | 2.0 4.5 6.0 | 1.5 3.15 4.2 | 1.5 3.15 4.2 | 1.5 3.15 4.2 | V |
| V _{T+min} | Minimum Positive-Going Input Threshold Voltage (Figure 5) | V _{OUT} = 0.1 V I _{OUT} ≤ 20 μA | 2.0 4.5 6.0 | 1.0 2.3 3.0 | 0.95 2.25 2.95 | 0.95 2.25 2.95 | V |
| V _{T-max} | Maximum Negative-Going Input Threshold Voltage (Figure 5) | V _{OUT} = V _{CC} − 0.1 V I _{OUT} ≤ 20 μA | 2.0 4.5 6.0 | 0.9 2.0 2.6 | 0.95 2.05 2.65 | 0.95 2.05 2.65 | V |
| V _{T-min} | Minimum Negative-Going Input Threshold Voltage (Figure 5) | V _{OUT} = V _{CC} − 0.1 V I _{OUT} ≤ 20 μA | 2.0 4.5 6.0 | 0.3 0.9 1.2 | 0.3 0.9 1.2 | 0.3 0.9 1.2 | V |
| V _{Hmax} (Note 7) | Maximum Hysteresis Voltage (Figure 5) | V _{OUT} = 0.1 V or V _{CC} − 0.1 V I _{OUT} ≤ 20 μA | 2.0 4.5 6.0 | 1.2 2.25 3.0 | 1.2 2.25 3.0 | 1.2 2.25 3.0 | V |
| V _{Hmin} (Note 7) | Minimum Hysteresis Voltage (Figure 5) | V _{OUT} = 0.1 V or V _{CC} − 0.1 V I _{OUT} ≤ 20 μA | 2.0 4.5 6.0 | 0.2 0.4 0.5 | 0.2 0.4 0.5 | 0.2 0.4 0.5 | V |
| V _{OH} | Minimum High-Level Output Voltage | V _{IN} ≤ V _{T-min} or V _{T+max} I _{OUT} ≤ 20 μA | 2.0 4.5 6.0 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | V |
| | | V _{IN} ≤ −V _{T-min} or V _{T+max} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA | 4.5 6.0 | 3.98 5.48 | 3.84 5.34 | 3.7 5.2 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{IN} ≥ V _{T+max} I _{OUT} ≤ 20 μA | 2.0 4.5 6.0 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V |
| | | V _{IN} ≥ V _{T+max} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA | 4.5 6.0 | 0.26 0.26 | 0.33 0.33 | 0.4 0.4 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = V _{CC} or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} = V _{CC} or GND I _{OUT} = 0 μA | 6.0 | 2.0 | 20 | 40 | μA |

7. V_{Hmin} > (V_{T+min}) − (V_{T-min}); V_{Hmax} = (V_{T+max}) + (V_{T-min}).

8. Information on typical parametric values can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6.0 \text{ ns}$)

| Symbol | Parameter | V_{CC} (V) | Guaranteed Limit | | | Unit |
|--------------------------|--|-------------------|------------------|-----------------|-----------------|------|
| | | | −55°C to 25°C | ≤ 85°C | ≤ 125°C | |
| t_{PLH} , t_{PHL} | Maximum Propagation Delay, Input A or B to Output Y (Figures 3 and 4) | 2.0 4.5 6.0 | 125 25 21 | 155 31 26 | 190 38 32 | ns |
| t_{TLH} , t_{THL} | Maximum Output Transition Time, Any Output (Figures 3 and 4) | 2.0 4.5 6.0 | 75 15 13 | 95 19 16 | 110 22 19 | ns |
| C_{in} | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |

9. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C _{PD} | Power Dissipation Capacitance (per Gate) (Note 10) | Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$ | | pF |
|-----------------|--|--|----|----|
| | | 24 | 24 | |

10. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

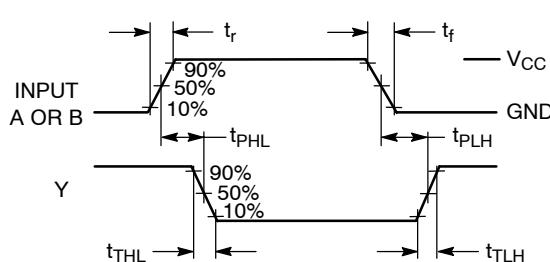
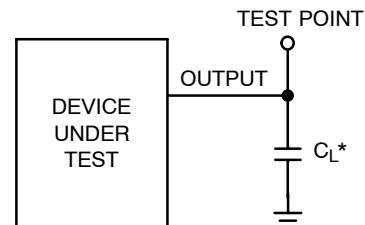


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

74HC132

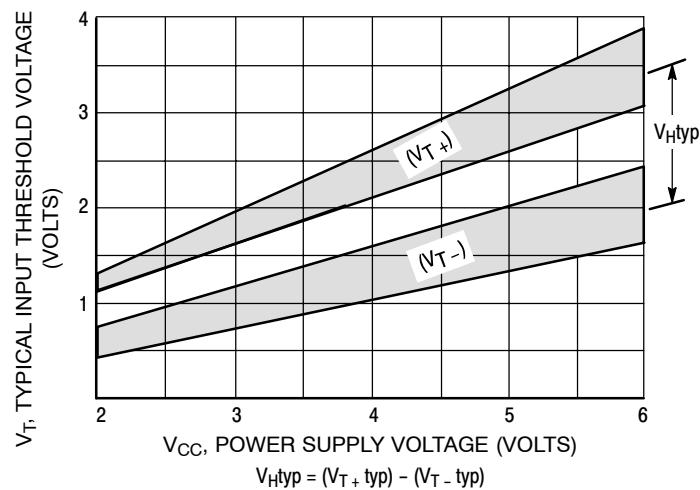


Figure 5. Typical Input Threshold, V_{T+} , V_{T-} Versus Power Supply Voltage

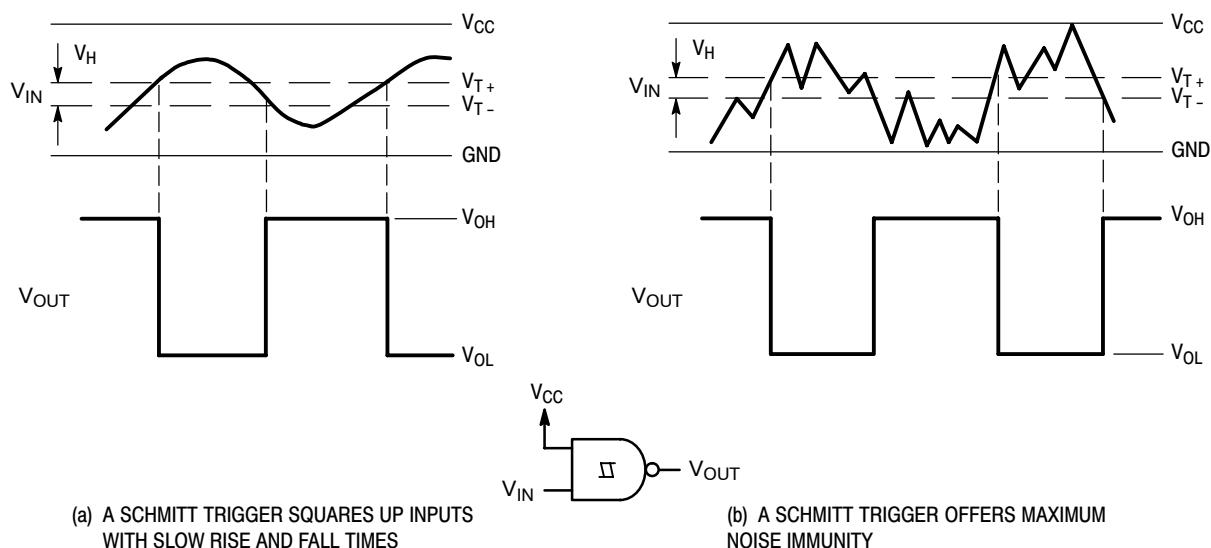
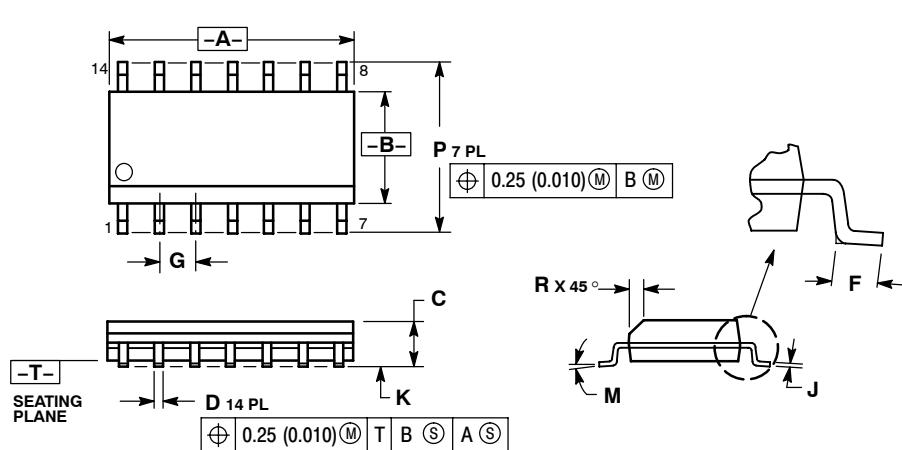


Figure 6. Typical Schmitt-Trigger Applications

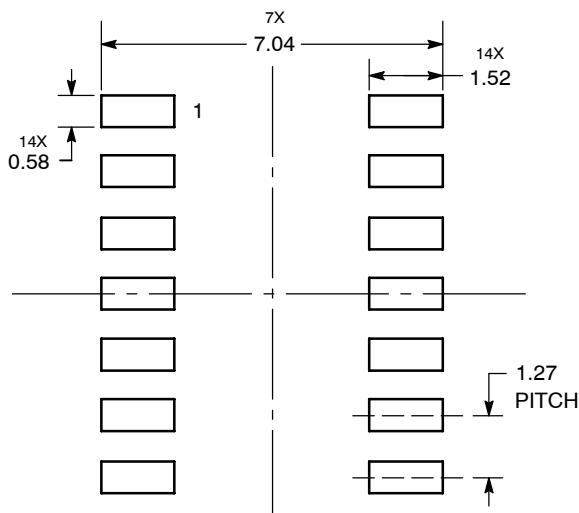
PACKAGE DIMENSIONS

SOIC-14
CASE 751A-03
ISSUE H



| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|--------|-------|
| | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 | BSC | 0.050 | BSC |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.018 |

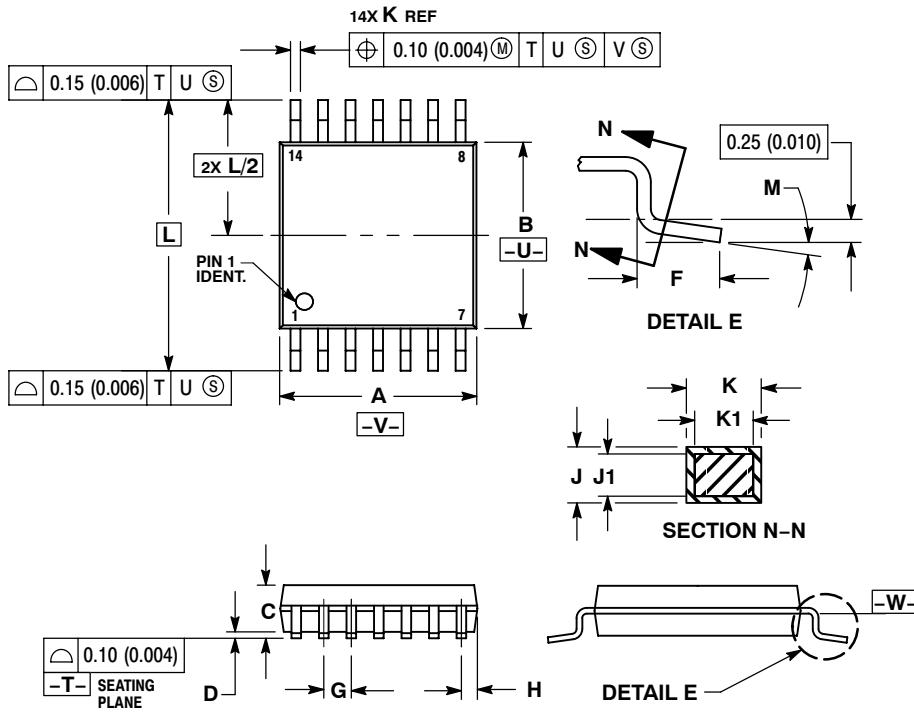
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

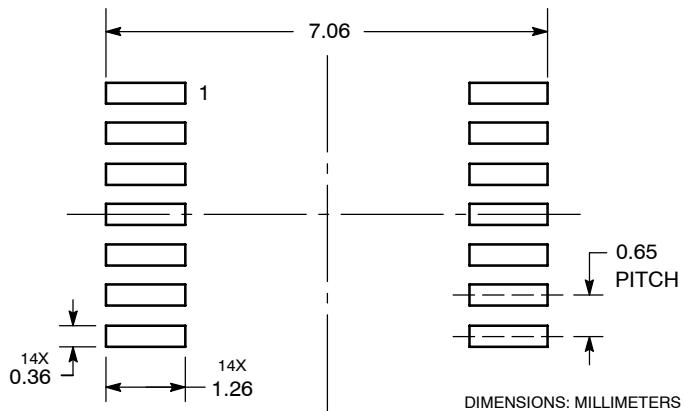
TSSOP-14
CASE 948G-01
ISSUE B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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